IT6801 Programming Guide

Ver 1.00

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Last Update Date: 2013/10/24

History

2013/10/24 initiate document.

Index

Chap 1 Term

MHL	**M**obile **H**igh-definition **L**ink
HDMI	High Definition Multimedia Interface
HPD	The MHL Link discovering to acknowledge a MHL sink connected.
Bank	There are more than 256 registers share the I^2C address 0x90, therefore the register in subaddress 0x0F[1:0] indicate the bank, where the bits are '00' the register bank is switched into bank 0; if reg0F[1:0] is '01', the register bank is switched to bank 1(which register represented as reg1XX), and if reg0F[1:0] is '10', the register bank is switched into bank 2 and the registers in the bank are represented as reg2XX.
RegXX	The registers with sub-address 0x**XX** of I^2C address 0x90 in bank **0**.
Reg1XX	The registers with sub-address 0x**XX** of I^2C address 0x90 in bank **1**.
Reg2XX	The registers with sub-address 0x**XX** of I^2C address 0x90 in bank **2**.
MHLyy	The MHL registers in I^2C address 0xE0 (which can be modified by Reg34 value) with sub-address 0x**yy**.
CECmm	The CEC registers in I^2C address 0xC0 (which can be modified by Reg86 value) with sub-address 0x**mm**.
EDIDnn	The EDID registers in I^2C address 0xA8 (which can be modified by Reg87 value) with sub-address 0x**nn**
Tx	MHL Transmitter
Rx	MHL Receiver
Packet	The packets carried in MHL data island period
Infoframe	The MHL packet with the infoframe format defined CEA861B/CEA861D/CEA861E
AVMute	The control bit status defined in the *General Control Packet* of MHL. When AVMute set is '1', MHL Rx should mute the video and audio output, otherwise if the AVMute clear is '1', the video and audio should be present.
Resquester	A MHL device which activate an MSC/DDC command to another device for updating or collecting some information
Responder	A MHL device which return data to or be updated data from the other device which activated an DDC or MSC command.

Chap 2 Introduction

General Description

The IT6801 is a signal port MHL/HDMI receiver which can operate in both HDMI1.4 and MHL2.0 dual mode, it is fully compatible with MHL2.0, HDMI 1.4a, HDMI 1.4a 3D and HDCP 1.4 and also backward compatible to DVI 1.0 specifications. The IT6801 with its Deep Color capability (up to 36-bit) ensures robust reception of high-quality uncompressed video content, along with state-of-the-art uncompressed and compressed digital audio content such as DTS-HD and Dolby TrueHD in digital televisions and projectors. The IT6801 also supports all the primary 3D formats which are compliant with the HDMI 1.4a 3D specification.

Aside from the various video output formats supported, the IT6801 also receives and provides 2 channels of I2S digital audio outputs, with sampling rate up to 192kHz and sample size up to 24 bits, facilitating direct connection to industry-standard low-cost audio DACs. Also, an S/PDIF output is provided to support up to compressed audio of 192kHz frame rate.

The High-Bit Rate (HBR) audio is also provided by the IT6801 in the S/PDIF output port. The S/PDIF interface highest possible HBR frame rate is supported at up to 768kHz.

Each IT6801 comes preprogrammed with an unique HDCP key, in compliance with the HDCP 1.4 standard so as to provide secure transmission of high-definition content. Users of the IT6801 need not purchase any HDCP keys or ROMs.

Chap 3 Initial

IT6801 initial can be separated into two parts. The first part is to initial HDMI/MHL configuration registers of IT6801. The second part is to initial MHLCBUS controlling registers of IT6801.

The registers in IT6801 are controlled by I2C protocol, via the PCSDA(pin24) and PCSCL(pin23) pins, and the main I2C address is 0x90 by PCADR (pin87) with low input, other the main I2C address is 0x92.

The MHL registers I2C address is configured in HDMI register (I2C address 0x90/0x92 part) offset 0x34, and the default address is 0xC0. To enable the access of MHL registers, HDMI Reg34[0] should set as '1'. In our providing firmware, we usually configure it as 0xE0.

34	Reg_P0_MHLPortAdr	7:1	I2C Slave Addresss for MHL block	R/W	1100000
	Reg_P0_MHLPortAdrEn	0	1: enable PC I2C access MHL block	R/W	0

The CEC registers I2C address is configured in Reg87, the default value is 0xC8, and the enable bit of CEC registers access is Reg86[0].

86	RegCECSlaveAdr	7:1	I2C Slave Address for CEC	R/W	1100100
		0	1: Enable access CEC block	R/W	0

The internal EDID RAM I2C address is configured in Reg87, the default value is 0xA8. To enable the internal EDID RAM access, the external EDID ROM DDC bus should be disconnected, then configure the EDID slave address as 0xA0 and set Reg87[0] as '1' to enable it.

87	RegEDIDSlaveAdr	7:1	I2C Slave Address for EDID	R/W	1010100
	RegEnEDIDSlaveAdr	0	1: Enable access EDID block	R/W	0

MHL 100 Microseconds Timer Calibration

IT6801 has internal ring oscillator, and it need calibration with the real time to adjust all the timing definition protocol as CEC and MHL CBUS communication.

For MHL CBUS wakeup procedure, IT6801 requires a dedicate 100 μs timer indicated in the MHL register:

Reg	Name	Bit	Definition	Type	Default
01	RegEnCBusDeGlitch	7	CBUS input de-glitch 0: disalbe, 1: enable	R/W	0
	RegOSCDivSel[2:0]	6:4	OSCCLK divide counter selection	R/W	100
	Reg100msTOAdj[1:0]	3:2	00: 100ms, 01: 99ms, 10: 101ms, 11: reserved	R/W	00
	RegEnCBusNack	1	Enable CBUS Nack bit protocol	R/W	0
	RegEn100msCnt	0	Enable 100ms calibration counter	R/W	0
02	Reg10usTimeInt[7:0]	7:0	10us time base integer number bit[7:0]	R/W	0xC8
03	Reg10usTimeInt[8]	7	10us time base integer number bit[8]	R/W	0
	Reg10usTimeFlt[6:0]	6:0	10us time base floating number	R/W	0000000
12	R100msTimeCnt[7:0]	7:0	100ms counter value	RO	
13	R100msTimeCnt[15:8]	7:0		RO	
14	R100msTimeCnt[23:16]	7:0		RO	

The values in the registers above should be referred by the internal ring oscillator of IT6801, thus it need an actual time period to calibrate the period in the MHL02/MHL03 registers. The procedure is described in follows:

- Get R100msTimeCnt (MHL14[7:0]|MHL13[7:0]|MHL12[7:0])

  1. MHL01 ← 0x41
  2. Delay 100ms

3. MHL01 ← 0x40

R100msTimeCnt = MHL14|MHL13|MHL12
To prevent the delay error range, consider to average of several times.

OSCCLK = R100msTimeCnt × 10 (in Hz)

- oscdiv

1. oscdiv = (int)(R100msTimeCnt+500000)/1000000
eg: If OCLK = 39MHz, R100msTimeCnt = 3.9MHz, oscdiv = R100msTimeCnt = 3, but 4 is better, therefore use (39+5)/10 = 4

2. MHL01[6:4] = oscdiv

- Set reference clock, depends on the power consumption and speed setting

54	RegEnAsynRst	7	1: Enable Asynchronous reset for OCLK	R/W	0
	RegMCLKSel	6:4	MCLK output clock multiple number 000: 128FS ; 001: 256FS ; 010: 384FS 011: 512FS ; 100: 640FS ; 101: 768FS 110: 894FS ; 111: 1024FS	R/W	001
	Reserved	3:2			
	RegRCLKFreqSel	1:0	RCLK frequency select 00: RINGCLK/2 ; 01: RINGCLK/4 10: RINGCLK/8 ; 11: RINGCLK/16	R/W	00

1. RegRCLKFreqSel = '01' OSCCLK/4

2. RCLK = OSCCLK/4

- Set RCLK parameter into MHL02/MHL03:

1. Reg10usTimerInt = int((RCLK/1000)/100) = MHL03[8]|MHL02[7:0]

2. Reg10usTimerFlt = int(128*(int(RCLK/1000) % 100) / 100) = MHL03[6:0] ;

3. After calculating the 10 us timing count, write them into MHL03 and MHL02.

Initial HDMI Register Setting

I2C address: 0x90

The following table is the setting sequence for each step. The Bit Clear Mask means the bit to update on each step, and the Bit Set Value means the updating part of each step.

HDMI Reg	Bit Clear Mask	Bit Set Value	Description
0x0F	0x03	0x00	Change Bank 0
0x10	0xFF	0x08	
0x10	0xFF	0x17	
0x11	0xFF	0x1F	
0x18	0xFF	0x1F	
0x12	0xFF	0xF8	
0x10	0xFF	0x10	
0x11	0xFF	0xA0	
0x18	0xFF	0xA0	
0x12	0xFF	0x00	
0x0F	0x03	0x01	Change Bank 1
0xC0	0x80	0x00	

0x0F	0x03	0x00	Change bank 0
0x17	0xC0	0x80	
0x1E	0xC0	0x00	
0x0E	0xFF	0xFF	
0x86	0xFF	0xC9	SW programmable I2C address of CEC
0x16	0x08	0x08	
0x1D	0x08	0x08	
0x2B	0x07	0x07	
0x31	0xFF	0x2C	
0x34	0xFF	0xE1	SW programmable I2C address of MHL
0x35	0x0C	0x01	
0x54	0x0C	0x09	RCLK Frequency select
0x6A	0xFF	0x81	Decide which kind of packet on General PKT
0x74	0xFF	0xA0	
0x50	0x1F	0x12	
0x65	0x0C	0x08	
0x7A	0x80	0x80	
0x85	0x02	0x02	
0xC0	0x03	0x00	
0x87	0xFF	0xA9	SW programmable I2C address of EDID
0x71	0x08	0x00	
0x37	0xFF	0x88	
0x4D	0xFF	0x88	
0x67	0x80	0x00	
0x7A	0x70	0x70	
0x7E	0x40	0x00	
0x52	0x20	0x20	
0x53	0xC0	0x40	
0x58	0xFF	0xAB	Video output driving strength
0x59	0xFF	0xAA	Audio output driving strength
0x0F	0x03	0x01	Change bank 1
0xBC	0xFF	0x06	
0xB5	0x03	0x03	
0xB6	0x07	0x00	
0xB1	0xFF	0x20	
0xB2	0xFF	0x01	
0x0F	0x03	0x00	Change bank 0
0x25	0xFF	0x1F	Default EQ Value
0x3D	0xFF	0x1F	Default EQ Value
0x27	0xFF	0x1F	Default EQ Value
0x28	0xFF	0x1F	Default EQ Value
0x29	0xFF	0x1F	Default EQ Value
0x3F	0xFF	0x1F	Default EQ Value
0x40	0xFF	0x1F	Default EQ Value
0x41	0xFF	0x1F	Default EQ Value
0x22	0xFF	0x00	
0x26	0xFF	0x00	
0x3A	0xFF	0x00	
0x3E	0xFF	0x00	
0x20	0x7F	0x3F	

0x38	0x7F	0x3F	

Initial MHL Register Setting

I2C address is 0xE0

MHL Reg	Bit Clear Mask	Bit Set Value	Description
0x0A	0xFF	0x00	
0x08	0xFF	0x00	
0x09	0xFF	0x00	
0x52	0xFF	0x00	
0x53	0xFF	0x80	
0x32	0xFF	0x0C	
0x81	0xFF	0x20	Device Capability: MHL 2.0 version
0x82	0xFF	0x31	Device Capability: PLIM and POW and Sink Type
0x83	0xFF	0x78	Device Capability: Adopter ID
0x84	0xFF	0x56	Device Capability: Adopter ID
0x8B	0xFF	0x68	Device Capability: Device ID
0x8C	0xFF	0x02	Device Capability: Device ID
0x28	0x01	0x00	
0x0F	0x20	0x20	
0x29	0x80	0x80	
0x39	0x80	0x80	
0x00	0x8F	0x01	
0x01	0x8C	0xC4	
0x0C	0x89	0x88	
0x36	0xFC	0xB7	
0x38	0x20	0xF8	
0x5C	0xFC	0x00	
0x66	0x03	0x01	
0x2A	0x01	0x01	
0x0F	0x10	0x00	

Chap 4 EDID RAM

IT6801 has 256 bytes RAM to support the EDID Function. The HDMI/MHL Source device can read EDID data only from IT6801 EDID RAM through the HDMI/MHL DDC bus for getting the Video and Audio capability of the HDMI/MHL Sink device.

EDID RAM Configuration

For access the EDID RAM of IT6801 need to configure the HDMI Reg87 and HDMI RegC0.

Reg	Register Name	Bit	Bit Description	Default
0xC0	Reserved	7		0
	RegEnMultiSeg	6	1: Enable multiple segment	0
	RegSoftEDIDRst	5	1: EDID reset	0
	RegAutoPwdEDID	4	1: auto powerdown EDID	0
	RegEDIDAdrSel	3	1: EDID address A2 ; 0: EDID address A0	0
	RegEnDetDDC	2	1: Enable monitor DDC detect start	1
	Reg_P1DisableShadow	1	1: disable Port 1 Internal EDID	1
	Reg_P0DisableShadow	0	1: disable Port 0 Internal EDID	1

Set HDMI RegC0=0x40 for Enable Internal EDID Shadow of IT6801.

Set HDMI RegC0=0x07 for Disable Internal EDID Shadow of IT6801.

Reg	Register Name	Bit	Bit Description	Default
0x87	RegEDIDSlaveAdr	7:1	I2C Slave Address for EDID	0x00
	RegEnEDIDSlaveAdr	0	1: Enable access EDID block	

Set HDMI Reg87=0xC9 for Enable EDID RAM Block and set I2C Slave address to 0xC8.

EDID RAM Update

After EDID RAM configuration by register 0x87, then we can update customer's EDID data to EDID RAM by I2C Bus. At last, we need to set EDID physical address and EDID check sum on IT6801 register for identify EDID of input port .

Reg	Register Name	Bit	Bit Description	Default
0xC1	Reg_VSDBAdr	7:0	VSDB PA offset of EDID	
0xC2	Reg_P0_AB	7:0	Physical address 1 of Port 0	
0xC3	Reg_P0_CD	7:0	Physical address 2 of Port 0	
0xC4	Reg_P0_B0Sum	7:0	Block 0 Check sum of Port 0	
0xC5	Reg_P0_B1Sum	7:0	Block 1 Check sum of Port 0	

For example, the following is an EDID sample, and VSDB *(refer to High-Definition Multimedia Interface Specification Version 1.4b, 8.3.2 HDMI Vendor-Specific Data Block, p150)* offset is in 0xA0, and the physical address location in the following EDID sample is in offset 0xA4, 0xA5. Then assign the physical address of each port in RegC2, RegC3, RegC8, RegC9, and update the checksum of the block 0 and block 1 of each port, then the different EDID will be represented in the same internal EDID RAM.

OFFSET	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
00	00	FF	FF	FF	FF	FF	FF	00	11	D2	05	00	00	00	00	00
10	24	14	01	03	80	46	28	78	0A	0D	C9	A0	57	47	98	27
20	12	48	4C	20	00	00	01	01	01	01	01	01	01	01	01	01
30	01	01	01	01	01	01	02	3A	80	18	71	38	2D	40	58	2C
40	45	00	DF	A4	21	00	00	1E	01	1D	80	18	71	1C	16	20
50	58	2C	25	00	DF	A4	21	00	00	9E	00	00	00	FC	00	53
60	6F	6E	79	20	41	54	43	0A	20	20	20	20	00	00	00	FD
70	00	3A	3E	0F	46	0F	00	0A	20	20	20	20	20	20	01	25
80	02	03	3B	71	53	94	13	05	03	04	11	10	1F	20	22	3C
90	3E	12	02	01	16	15	07	06	23	0F	7F	07	83	7F	00	00
A0	7A	03	0C	00	10	00	A8	2D	21	C0	10	01	41	01	12	20

B0	28	10	66	00	08	10	76	96	90	A0	B0	8C	0A	D0	8A	20
C0	E0	2D	10	10	3E	96	00	DF	A4	21	00	00	18	8C	0A	D0
D0	8A	20	E0	2D	10	10	3E	96	00	30	A4	21	00	00	18	8C
E0	0A	A0	14	51	F0	16	00	26	7C	43	00	30	A4	21	00	00
F0	98	00	00	00	00	00	00	00	00	00	00	00	00	00	00	D2

About the EDID RAM relate function. Please refer EDID Function Call on the IT6801 reference code.

As below function:

```
static void EnableEDIDupdata(void);
static void DisableEDIDupdata(void);
static void EDIDRAMInitial(unsigned char *pIT6801EDID);
static unsigned char Find_Phyaddress_Location(unsigned char *pEDID,unsigned char
Block_Number);
static void UpdateEDIDReg(unsigned char u8_VSDB_Addr, unsigned char CEC_AB, unsigned char
CEC_CD, unsigned char Block1_CheckSum);
```

Chap 5 Video Output

There is only one MHL/HDMI input port on IT6801. It can receive the MHL/HDMI/DVI input signal. And output 24 bit TTL with numerous formats, this chapter describe how to configure the video path and video output.

Video Output Flow

For HDMI/DVI input, IT6801 output video when it got a valid video input. The following steps are for getting the valid video output:

1. IT6801 should detect 5V in corresponding HDMI port
2. IT6801 gets valid SCDT (with SCDT status bit present and no SCDT off interrupt present).
3. Configure the video path of IT6801.
4. Turn off the video I/O and video data tri-state.

For MHL input from Input Port 0, following steps are for getting the valid video output:

1. Waiting CBUS discovery Done interrupt
2. IT6801 gets valid SCDT (with SCDT status bit present and no SCDT off interrupt present).
3. Configure the video path of IT6801.
4. Turn off the video I/O and video data tri-state.

Video Input Port Selection

51	RegPWDCSC	7	1: power down color space conversion logic	R/W	0
	RegHalfPCLKC	6	1: output PCLKO with half frequency.	R/W	0
	Reg_OutDDR	5	1: Enable data output at rising and falling edge of output clock (DDR mode)	R/W	0
	Reg_Half_CLK	4	1: Output half pixel clock	R/W	0
	RegDisPixRpt	3	1: disable pixel repeat	R/W	0
	Reg2x656CLK	2	1: output is CCIR656 mode	R/W	0
	RegEn_Debug	1	1: enable debug output to IO	R/W	0
	RegMainPortSel	0	Main Port selector 0: Port 0 MHL/HDMI	R/W	0

The IT6801 must to set '0' on HDMI Reg51[0].

The input video status are represented in the Reg0A~Reg0C, as following:

0A	P0_SCDT	7	Port 0 Video is stable	RO	
	P0_MHLMode	6	Port 0 MHL(1)/HDMI(0) mode '0': HDMI mode '1': MHL mode	RO	
	P0_IPLL_LOCK	5	Port 0 IPLL is locked	RO	
	P0_IPLL_HS	4	Port 0 IPLL clock is higher than 80MHz	RO	
	P0_RxCLK_Valid	3	Port 0 Rx clock is valid	RO	
	P0_RxCLK_Detect	2	Port 0 Rx clock detect	RO	
	P0_HDMI_Mode	1	Port 0 HDMI(1)/DVI(0) mode	RO	
	P0_PWR5V_Det	0	Port 0 power 5V detect	RO	
0C					
	P0_RxCLK_Stable	6	Port 0 clock is stabled	RO	
	MHL3DFreSeq	5	Receive MHL frame sequence 3D InfoFrame	RO	
	ARAM_bo_doneHQ	4	Audio RAM BIST Done	RO	
	reserved	3		RO	
	reserved	2		RO	
	reserved	1		RO	
	reserved	0		RO	

To check Reg0A[7] if it is '1' for assert video stable, After video input is stable, the output video can be configure.

Video Output Configuration

Video output signal type are configured by Reg51, Reg52 and Reg65, as the following tables:

51	RegPWDCSC	7	1: power down color space conversion logic	R/W	0
	RegHalfPCLKC	6	1: output PCLKO will be half frequency.	R/W	0
	Reg_OutDDR	5	1: Enable data output at rising and falling edge of output clock (DDR mode)	R/W	0
	Reg_Half_CLK	4	1: Output half pixel clock	R/W	0
	RegDisPixRpt	3	1: disable pixel repeat	R/W	0
	Reg2x656CLK	2	1: output is CCIR656 mode	R/W	0
	RegEn_Debug	1	1: enable debug output to IO	R/W	0
	RegMainPortSel	0	Main Port selector 0: Port 0	R/W	0
52	RegHCLKSel	7	HCLK source select when reg46h(6)=1	R/W	0
	RegEnSWHCLKSel	6	1: enable force HCLK source select	R/W	0
	RegDisVAutoMute	5	1: disable video auto mute	R/W	1
	RegTriSPDIF	4	1: Tri-state SPDIF IO	R/W	0
	RegTriI2SIO	3:0	Tristate Audio I2S0-I2S3 output buffer 1: Tri-state I2S[X] IO	R/W	0000
65	Reg_BTA1004Fmt	7	1: output BTA1004 format	R/W	0
	Reg_SyncEmb	6	1: output embeded sync	R/W	0
	Reg_OutColMod	5:4	Output color space 00: RGB444 , 01: YUV422 , 10: YUV444	R/W	00
	Reg_OutBit	3:2	Output color depth 00: 8bits, 01: 10bis, 10: 12bits	R/W	00
	Reg_CSCSel	1:0	00: bypass CSC 01: RGB to YUV 11: YUV to RGB	R/W	00

The combination are as following tables:

Color Space	Video Format	Bus Width	H/Vsync	Clocking	Setting
RGB	4:4:4	24/30/36	Seperate	1X	Reg51 = 0x00 Reg65[7:4] = '0000'
		12/15/18	Seperate	Dual-edged	Reg51 = 0x20 Reg65[7:4] = '0000'
		24/30/36	Seperate	0.5X, Dual-edged	Reg51 = 0x40 Reg65[7:4] = '0000'
YCbCr	4:4:4	24/30/36	Seperate	1X	Reg51 = 0x00 Reg65[7:4] = '0010'
		12/15/18	Seperate	Dual-edged	Reg51 = 0x20 Reg65[7:4] = '0010'
		24/30/36	Seperate	0.5X, Dual-edged	Reg51 = 0x40 Reg65[7:4] = '0010'
	4:2:2	16/20/24	Seperate	1X	Reg51 = 0x00 Reg65[7:4] = '0001'
			Seperate	0.5X, Dual-edged	Reg51 = 0x40 Reg65[7:4] = '0001'
			Embedded	1X	Reg51 = 0x00 Reg65[7:4] = '0101'
			Embedded	0.5X, Dual-edged	Reg51 = 0x40 Reg65[7:4] = '0101'
		8/10/12	Seperate	2X	Reg51 = 0x44 Reg65[7:4] = '0001'
			Seperate	1X, Dual-edged	Reg51 = 0x44 Reg65[7:4] = '0001'
			Embedded	2X	Reg51 = 0x44 Reg65[7:4] = '0101'
			Embedded	1X, Dual-edged	Reg51 = 0x44 Reg65[7:4] = '0101'
		BTA1004	Embedded	1X	Reg51 = 0x00 Reg65[7:4] = '1101'
			Embedded	0.5X, Dual-edged	Reg51 = 0x40 Reg65[7:4] = '1101'

Before enable video output (turning tri-state off), should reset *Reg_656FFRst* (Reg64[7] = '1' → '0'), then turn on the video output.

Color Space Matrix

Before enable color space convert, Reg51[7] should be '0'.

51	RegPWDCSC	7	1: power down color space conversion logic	R/W	0
	RegHalfPCLKC	6	1: output PCLKO will be half frequency.	R/W	0
	Reg_OutDDR	5	1: Enable data output at rising and falling edge of output clock (DDR mode)	R/W	0
	Reg_Half_CLK	4	1: Output half pixel clock	R/W	0
	RegDisPixRpt	3	1: disable pixel repeat	R/W	0
	Reg2x656CLK	2	1: output is CCIR656 mode	R/W	0
	RegEn_Debug	1	1: enable debug output to IO	R/W	0
	RegMainPortSel	0	Main Port selector 0: Port 0 ; 1: Port 1	R/W	0

Input color mode is in AVI Infoframe DB1[6:5] or in Reg71[1:0].

If the MHL data input is under MHL packed pixel mode, the input color will be YCbCr422.

71	Reserved	7:4			
	RegEnPPColMode	3	1: Input color mode YUV422 when PP mode	R/W	1
	Reg_ForceColMod	2	0: Input color mode auto detect 1: Force input color mode as bit[3:2] setting	R/W	0
	Reg_ColMod_Set	1:0	Input color mode set: 00: RGB mode ; 01: YUV422 mode 10: YUV444 mode	R/W	00

Output Color Space and Selection are in Reg65

65	Reg_BTA1004Fmt	7	1: output BTA1004 format	R/W	0
	Reg_SyncEmb	6	1: output embedded sync	R/W	0
	Reg_OutColMod	5:4	Output color space 00: RGB444 , 01: YUV422 , 10: YUV444	R/W	00
	Reg_OutBit	3:2	Output color depth 00: 8bits, 01: 10bis, 10: 12bits	R/W	00
	Reg_CSCSel	1:0	00: bypass CSC 10: RGB to YUV 11: YUV to RGB	R/W	00

Color space matrix are as following registers:

Color space conversion					
170	Reg_YOffset	7:0	Y blank level	R/W	0x10
171	Reg_COffset	7:0	C blank level	R/W	0x80
172	Reg_REGOffset	7:0	R/G/B blank level	R/W	0x00
173	Reg_Matrix11V[7:0]	7:0	Color space conversion matrix	R/W	0xB2
174	Reserved	7:6			
	Reg_Matrix11V[13:8]	5:0	Color space conversion matrix	R/W	000100
175	Reg_Matrix12V[7:0]	7:0	Color space conversion matrix	R/W	0x64
176	Reserved	7:6			
	Reg_Matrix12V[13:8]	5:0	Color space conversion matrix	R/W	000010
177	Reg_Matrix13V[7:0]	7:0	Color space conversion matrix	R/W	0xE9
178	Reserved	7:6			
	Reg_Matrix13V[13:8]	5:0	Color space conversion matrix	R/W	000000
179	Reg_Matrix21V[7:0]	7:0	Color space conversion matrix	R/W	0x93
17A	Reserved	7:6			
	Reg_Matrix21V[13:8]	5:0	Color space conversion matrix	R/W	011100
17B	Reg_Matrix22V[7:0]	7:0	Color space conversion matrix	R/W	0x16
17C	Reserved	7:6			
	Reg_Matrix22V[13:8]	5:0	Color space conversion matrix	R/W	000100
17D	Reg_Matrix23V[7:0]	7:0	Color space conversion matrix	R/W	0x56

17E	Reserved	7:6			
	Reg_Matrix23V[13:8]	5:0	Color space conversion matrix	R/W	011111
17F	Reg_Matrix31V[7:0]	7:0	Color space conversion matrix	R/W	0x49
180	Reserved	7:6			
	Reg_Matrix31V[13:8]	5:0	Color space conversion matrix	R/W	011101
181	Reg_Matrix32V[7:0]	7:0	Color space conversion matrix	R/W	0x9F
182	Reserved	7:6			
	Reg_Matrix32V[13:8]	5:0	Color space conversion matrix	R/W	011110
183	Reg_Matrix33V[7:0]	7:0	Color space conversion matrix	R/W	0x16
184	Reserved	7:6			
	Reg_Matrix33V[13:8]	5:0	Color space conversion matrix	R/W	000100

and the setting for color converting setting are:

Color space converting table		RGB to YUV				YUV to RGB			
		RGB to YUV 601		RGB to YUV 709		YUV to RGB 601		YUV to RGB 709	
	reg	16~ 235	0 ~ 255	16~ 235	0 ~ 255	16~ 235	0 ~ 255	16~ 235	0 ~ 255
Reg_CSCSel[1:0]	65[1:0]	10	10	10	10	11	11	11	11
Reg_YoffSet[7:0]	170	0x00	0x10	0x00	0x10	0x00	0x04	0x00	0x04
Reg_CoffSet[7:0]	171	0x80	0x80	0x80	0x80	0x00	0x00	0x00	0x00
Reg_RGBOffSet[7:0]	172	0x10	0x10	0x10	0x10	0x00	0xA7	0x00	0xA7
Reg_Matrix11V[13:0]	173	0xB2	0x09	0xB8	0XE4	0x00	0x4F	0x00	0x4F
	174	0x04	0x04	0x05	0x04	0x08	0x09	0x08	0x09
Reg_Matrix12V[13:0]	175	0x65	0x0E	0xB4	0x77	0x6B	0x81	0x55	0xBA
	176	0x02	0x02	0x01	0x01	0x3A	0x39	0x3C	0x3B
Reg_Matrix13V[13:0]	177	0xE9	0XC9	0x94	0x7F	0x50	0xDD	0x88	0x4B
	178	0x00	0x00	0x00	0x00	0x3D	0x3C	0x3E	0x3E
Reg_Matrix21V[13:0]	179	0x93	0x0F	0x4A	0XD0	0x00	0x4F	0x00	0x4F
	17A	0x3C	0x3D	0x3C	0x3C	0x08	0x09	0x08	0x09
Reg_Matrix22V[13:0]	17B	0x18	0x84	0x17	0x83	0xF5	0xC4	0x51	0x57
	17C	0x04	0x03	0x04	0x03	0x0A	0x0C	0x0C	0x0E
Reg_Matrix23V[13:0]	17D	0x55	0x6D	0x9F	0xAD	0x02	0x01	0x00	0x02
	17E	0x3F	0x3F	0x3F	0x3F	0x00	0x00	0x00	0x00
Reg_Matrix31V[13:0]	17F	0x49	0xAB	0xD9	0x4B	0x00	0x4F	0x00	0x4F
	180	0x3D	0x3D	0x3C	0x3D	0x08	0x09	0x08	0x09
Reg_Matrix32V[13:0]	181	0x9F	0xD1	0x10	0x32	0xFD	0xFD	0x00	0xFE
	182	0x3E	0x3E	0x3F	0x3F	0x3F	0x3F	0x00	0x3F
Reg_Matrix33V[13:0]	183	0x18	0x84	0x17	0x84	0xDA	0x1F	0x84	0xE8
	184	0x04	0x03	0x04	0x03	0x0D	0x10	0x0E	0x10

Video I/O and Video Data I/O Tristate

The following register control the video signal output:

Reg	Name	Bit	Description	Type	Default
53	RegVDGatting	7	Enable output data gating to zero when no Video display	R/W	0
	RegVIOSel	6	1: video IO enable depent on VIOenable 0: video IO eanble depent on VDIO1enable	R/W	0
	RegVDIOLLdisable	5	1: disable video IO QE0, QE1, QE12, QE13, QE24, QE25	R/W	0
	RegVDIOLHdisable	4	1: disable video IO QE2, QE3, QE14, QE15, QE26, QE27	R/W	0
	RegTriVDIO	3 2 1	1: enable tri-state Video IO QE35~QE24 1: enable tri-state Video IO QE23~QE12 1: enable tri-state Video IO QE11~QE0	R/W	0
	RegTriVIO	0	1: Tristate video control signal IO	R/W	0

RegTriVIO set tri-state of all video I/O TTL signal, such as H/V sync, DE, Video data (QE35~QE0).

If RegVIOSel is selected, the RegTriVDIO can just set tri-state to video data output but keep the video sync output; for 10bit/8bit signal output, the *RegVDIOLHdisable/RegVDIOLLdisable* can set tri-state to those low bit data to avoid noise under those pins are floating.

Event of Video Process

Those registers listed below are the event flags for the input video event:

Reg	Name	Bit	Description	Type	Default
05	P0_HDCPOff_Det	7	Port 0 HDCP off detect Interrupt	W1C	
	P0_ECCErrTrg	6	Port 0 ECC error Interrupt	W1C	
	P0_HDMIMode_Chg	5	Port 0 HDMI/DVI mode change Interrupt	W1C	
	P0_HDCP_Auth_Done	4	Port 0 HDCP authentication done Interrupt	W1C	
	P0_HDCP_Auth_Start	3	Port 0 HDCP authentication start Interrupt	W1C	
	P0_RxCLK_StbChg	2	Port 0 Rx Clock stable change Interrupt	W1C	
	P0_RxCLKOn_Det	1	Port 0 Rx Clock on detect Interrupt	W1C	
	P0_PWR5V_Chg	0	Port 0 power 5V state change Interrupt	W1C	
07	AudioFIFOError	7	Audio FIFO error Interrupt	W1C	
	AutoAudioMute	6	Audio Auto Mute Interrupt	W1C	
	PktLeftMute	5	AVMute clear is received Interrupt	W1C	
	PktSetMute	4	AVMute set is received Interrupt	W1C	
	TimerInt	3	Timer count to setting value Interrupt	W1C	
	VideoModeChg	2	Input Video Mode Change Interrupt	W1C	
	SCDTChg	1	Video Stable State Change Interrupt	W1C	
	MHLModeChg	0	MHL/HDMI mode change Interrupt	W1C	
08	NoGenPkt2_Rcv	7	No AVI packet is received	W1C	
	NoGenPkt_Rcv	6	No GenPkt is received	W1C	
	NoAud_Rcv	5	No Audio InfoFrame is received	W1C	
	NoAVI_Rcv	4	No AVI InfoFrame is received	W1C	
	CD_Det	3	Color Depth change Interrupt	W1C	
	GenPkt_Det	2	General packet detect Interrupt	W1C	
	ISRC2_Det	1	ISRC2 packet detect Interrupt	W1C	
	ISRC1_Det	0	ISRC1 packet detect Interrupt	W1C	
09	H2VSkewFail	7	Port 0 H2V FIFO Fail interrupt		
	P1_DeSkewErr	6	Port 1 deskew error interrupt	W1C	
	P0_DeSkewErr	5	Port 0 deskew error interrupt	W1C	
	NewAudioPkt_Det	4	New Audio Packet detect Interrupt	W1C	
	NewACPPkt_Det	3	New ACP Packet detect Interrupt	W1C	
	NewSPDPkt_Det	2	New SPD Packet detect Interrupt	W1C	
	NewMPEGPkt_Det	1	New MPEG Packet detect Interrupt	W1C	
	NewAVIPkt_Det	0	New AVI InfoFrame detect Interrupt	W1C	

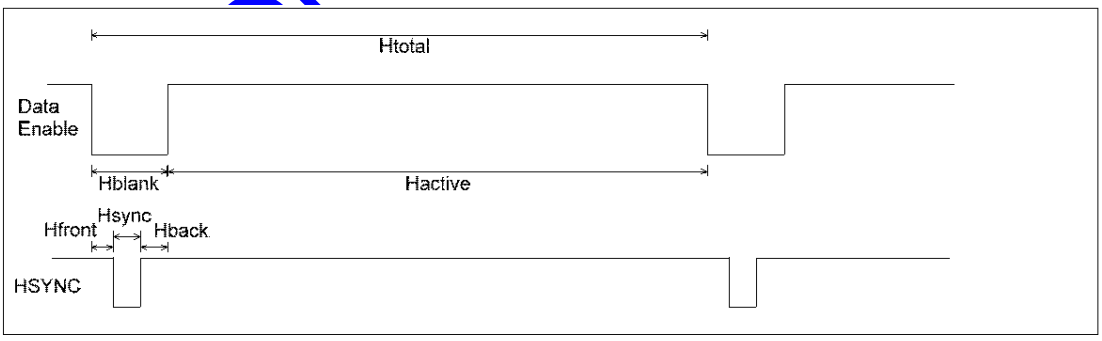
When an event occurs, firmware should process the event and write the corresponding bit with '1' to clear the bit.

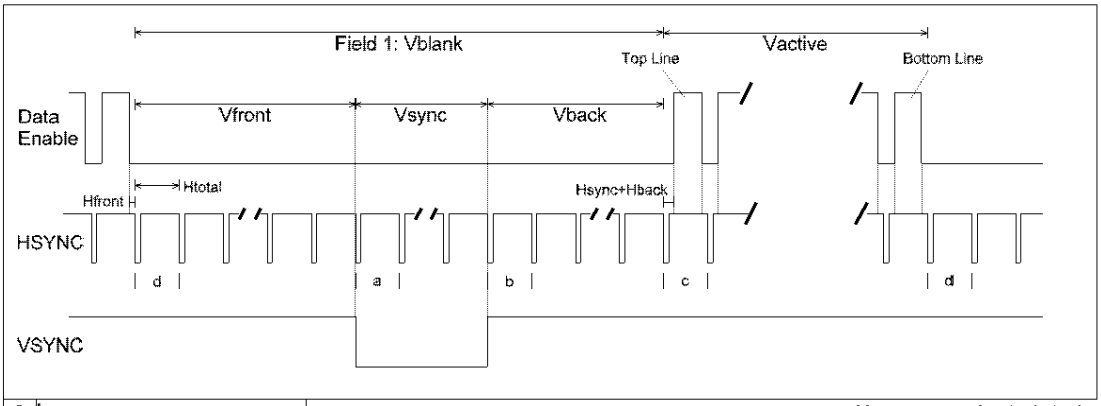
Video Input Status Readback

The following registers describe the input video parameter on the active input port:

99	GCP_CD_Active	7:4	Color depth decoder value 4: 24bits ; 5: 30bits ; 6: 36bits ; 7: 48bits	RO	
	PxVideoStable	3	Indicate if video signal is stable	RO	
	VidField	2	Video field number in interlaced mode	RO	
	VidInterlaceMode	1	Indicate video is in interlaced mode	RO	
	VidModeChg	0	Indicate if a video mode change occurs	RO	
9A	PIXCLKSpeed	7:0	PCLK = RCLK*255/PIXCLKSpeed	RO	
9C	VidHorTotal[7:0]	7:0	The total pixel count of one line[7:0]	RO	
9D	Reserved	7:6			
	VidHorTotal[13:8]	5:0	The total pixel count of one line[13:8]	RO	
9E	VidHorActive[7:0]	7:0	The active pixel count of one line[7:0]	RO	
9F	Reserved	7:6			
	VidHorActive[13:8]	5:0	The active pixel count of one line[13:8]	RO	
A0	VidHSyncWidth[7:0]	7:0	The width of Horizontal sync [7:0]	RO	
A1	VidHorFrontPorch[11:8]	7:4	The width of Horizontal sync front porch [11:8]	RO	
	Reserved	3:1			
	VidHSyncWidth[8]	0	The width of Horizontal sync [8]	RO	
A2	VidHorFrontPorch[7:0]	7:0	The width of Horizontal sync front porch [7:0]	RO	
A3	VidVerTotal[7:0]	7:0	The total line count of a field [7:0]	RO	
A4	VidVerActive[11:8]	7:4	The active line count of a field [11:8]	RO	
	VidVerTotal[11:8]	3:0	The total line count of a field [11:8]	RO	
A5	VidVerActive[7:0]	7:0	The active line count of a field [7:0]	RO	
A6	Reserved	7:5			
	VidVSyncWidth	4:0	The width of Vertical sync [4:0]	RO	
A7	Reserved	7:6			
	VidVerFrontPorch	5:0	The width of Vertical sync front porch	RO	
A8					
	P0_VSync_In_Pol	3	Port 0 Vertical sync input polarity	RO	
	P0_HSync_In_Pol	2	Port 0 Horizontal sync input polarity	RO	
	P0_HDCP_Dis_Flag	1	Port 0 HDCP disable Flag	RO	
	P0_AVMute	0	Port 0 is in AVMute state	RO	
A9	Reserved	7		RO	
	Reserved	6		RO	
	Reserved	4			
	Pix_Rep	3:0	Input video pixel repetition count Pixel repetition is Pix_Rep+1	RO	

The values in the table above represented the detected active input video timing while video stable. The parameter meaning as the following figure:





a	Ln
b	Ln+Vsync
c	Ln+Vsync+Vback
d	Ln+Vsync+Vback+Vactive

H parameters in pixel clocks
V parameters in lines
Letters a, b, c, … represent line numbers

HTotal[13:0] = Reg9D[5:0] | Reg9C[7:0]

HActive[13:0] = Reg9F[5:0] | Reg9E[7:0]

HSyncWidth[8:0] = RegA1[0] | RegA0[7:0]

HFrontPorch[11:0] = RegA1[7:4] | RegA2[7:0] (Notice the high nibble in the I2C address lower offset)

HBackPorch = HTotal – HActive – HFrontPorch – HSyncWidth

VTotal[11:0] = RegA4[3:0] | RegA3[7:0]

VActive[11:0] = RegA4[7:4] | RegA5[3:0]

VSyncWidth[4:0] = RegA6[4:0]

VFrontPorch[5:0] = RegA7[5:0]

VBackPorch = VTotal – VActive – VFrontPorch – VSyncWidth

Please notice the vertical parameters are of one field (half frame in interlaced mode). For interlaced mode, the actually frame parameter should be count as twice.

Chap 6 Audio Output

HDMI/MHL audio exists in the packages of data island, appended in the blank of video data. Therefore, audio could only exist with video playback. If the video is not ready, there is no audio. IT6801 support LCPM audio from 32KHz to 192KHz, 2 channels, compress audio with data rate up to 32bits*192KHz, High bit rate audio such as TrueHD or DTS-HD audio. There are 3 hardware pin combine the audio I2S and SPDIF signal. (Pin_41 for MUTE/MCLK, Pin_45 for WS/SPDIF , Pin_46 for SCK/MCLK) . If set Reg77[7:4]='1000' then audio output configure as I2S mode.(Pin_41 is MCLK, Pin_45 is WS, Pin_46 is SCK). If set Reg77[7:4]='0101' the audio output configure as S/PDDIF mode. (Pin_41 is MUTE, Pin_45 is SPDIF, Pin_46 is MCLK).

Audio Control Registers

Following table lists the control registers of audio used on IT6801.

Reg	Name	Bit	Description	Type	Default Value
74	Reg_I2SCEn	7	1: enable compressed (but non-HBR) audio output from I2S path	R/W	0
	RegForce_FS	6	Force Audio FS mode	R/W	0
	RegDis_False_DE	5	Disable false DE output	R/W	1
	RegAud_Info_Force	4	Force Audio setting from Aud info frame	R/W	0
	RegAVMute_Value	3	AVMute value when software AVMute is enable	R/W	0
	RegForce_AVMute	2	Software forced-AVMute mode	R/W	0
	RegDien	1	1: enable sdm dither	R/W	0
	RegDis_sdm	0	1: disable sdm	R/W	0
75	RegWS_Sel	7	1: invert channel A and channel B select	R/W	0
	RegI2S_Width	6:2	I2S word length, only effective in right justified mode; Maximum 24 bits	R/W	11000
	RegI2S_Mode	1:0	I2S output mode 00: I2S mode ; 01: right justified mode 10: left justified mode ; 11: undefined	R/W	00
76	RegI2S_CH3Sel	7:6	I2S channel 6 and channel 7 map: 00: map to input audio source 0 01: map to input audio source 1 10: map to input audio source 2 10: map to input audio source 3	R/W	11
	RegI2S_Ch2Sel	5:4	I2S channel 4 and channel 5 map: 00: map to input audio source 0 01: map to input audio source 1 10: map to input audio source 2 10: map to input audio source 3	R/W	10
	RegI2S_Ch1Sel	3:2	I2S channel 2 and channel 3 map: 00: map to input audio source 0 01: map to input audio source 1 10: map to input audio source 2 10: map to input audio source 3	R/W	01
	RegI2S_Ch0Sel	1:0	I2S channel 0 and channel 1 map: 00: map to input audio source 0 01: map to input audio source 1 10: map to input audio source 2 10: map to input audio source 3	R/W	00
77	RegAudIO_OutSel	7 6 7 4	For special output pin configure [7]: MUTE IO pin will output MCLKO [6]: SCK IO pin will output MCLKO [5]: I2S1 IO pin will output 3DR [4]: WS IO pin will output SPDIF	R/W	0000
	RegAudMode	3:2	Audio lock method select	R/W	00
	RegForce_CTS	1	Software force to set CTS value	R/W	0
	RegForce_CTSMode	0	Use CTS for audio FIFO adjustment	R/W	0

78	RegN_Set[7:0]	7:0	N [7:0] when ForceCTS	R/W	0x00
79	RegN_Set[15:8]	7:0	N[15:8] when ForceCTS	R/W	0x18
7A	RegBFrameSwap	7	1: enable audio B Frame Swap Interupt	R/W	1
	RegAud_cinc	6	1: decrease gain of integral path in digital path	R/W	1
	RegAud_cts_res	5:4	Decrease gain of propotional path in digital path	R/W	01
	RegN_Set[19:16]	3:0	N[19:16] when ForceCTS	R/W	0000
7B	Reserved	7:4			
	RegFS_Set	3:0	Software set sampling frequency 0000: 44.1KHz ; 0010: 48KHz 0011: 32KHz ; 1000: 88.2KHz 1010: 96KHz ; 1100: 176.4KHz ; 1110: 192KHz	R/W	0010
7C	RegHWMuteRate[7:0]	7:0	Hardware mute rate value [7:0]	R/W	0x20
7D	RegARAM_BIST_EN	7	1: enable Audio RAM BIST function	R/W	0
	RegHWForceMute	6	0: mute control by channel status 1: mute anyway	R/W	0
	RegHWAudMuteClrMode	5	FIFO mute clear	R/W	0
	RegHWMuteClr	4	Clear H/W mute	R/W	0
	RegHWMuteEn	3	H/W Mute enable	R/W	1
	RegHWMuteRate[10:8]	2:0	Hardware mute rate value [10:8]	R/W	000
7E	Reg_BiPhaseMode	7	1: enable SPDIF bi-phase mode	R/W	0
	Reg_HBRSel	6	1: HBR audio output to SPDIF 0: HBR audio output to I2S	R/W	0
	Reg_I2SOut_Fmt	5	1: output DSD audio when force I2Sout 0: output others audio when force I2Sout	R/W	0
	Reg_Force_I2SOut	4	1: Force I2S output format	R/W	0
	Reg_WAddWatch	3:2	Audio FIFO debug option	R/W	00
	Reg_HWAmpCtrl	1:0	Auido amplitude control 00: norma ; 01: 2X ; 10,11: 4X	R/W	00

Audio Input Status

The input audio status of active port is represented in RegAA:

AA	Audio_ON	7	Audio is ON	RO	
	HBRAudio	6	Audio type is High Bit Rate	RO	
	DSDAudio	5	Audio type is DSD	RO	
	Audio_Layout	4	Audio layout is 1 or 0	RO	
	Audio_CH_Valid		Audio channels valid Flag	RO	
		3	[3]: '1' of audio is avail in input audio source 3		
		2	[2]: '1' of audio is avail in input audio source 2		
		1	[1]: '1' of audio is avail in input audio source 1		
		0	[0]: '1' of audio is avail in input audio source 0		

If IT6801 received an input audio stream by audio sample packets, high bit rate audio packet (HBR), or one-bit audio packets (DSD), RegAA[7] will be '1'.

If the audio is in HBR packets, the RegAA[6] will be '1', otherwise if input audio is DSD audio, RegAA[5] will be '1', otherwise the audio is IEC60958 digital audio in audio sample packets.

Audio_CH_Valid register bits represent the input audio valid status. If the input is HBR or DSD audio, you can ignore it because HBR and DSD has their own layout definition.

IEC 60958 Audio Channel Status

The registers RegAB~RegAF represent the audio channel status under IEC60958, the bit definition as the following:

AB	Audio_CH_Status[7:0]	7:6	Channel Status Mode "00" Mode 0, *refer to IEC60958-3 5.2.2.*	RO
	Audio_CH_Status[5:3]	5:3	while bit[1] = '0', LPCM mode: 000: 2 audio channels without pre-emphasis 001: 2 audio channels with 50 us/15us pre-emphasis. otherwise: reserved	

			while bit[1] = '1', other than LPCM mode: 000: all are reserved	
	Audio_CH_Status[2]	2	'1': Software for which no copyright is asserted '0': Software for which copyright is asserted	
	Audio_CH_Status[1]	1	'1': Audio Sample word used for other purposes (Non-LPCM, compressed audio) '0': Audio Sample word represents linear PCM samples	
	Audio_CH_Status[0]	0	'0' Consmer use of channel status block	
AC	Audio_CH_Status[15:8] Catalog	7:0	Audio category code groups. Refer to IEC60958-3 5.3.2. channel status byte 2 (bit 15-8)	RO
AD	Audio_CH_Status[23:20] Channel Number	7:4	refer to IEC60958-3 p11 bit 23-20 single and dual channel operating modes are defined in IEC60958-1 Channel number of source 0 L-channel	RO
	Audio_CH_Status[19:16] Source Number	3:0	refer to IEC60958-3 p11 bit 16-19 Source number, 0~15, 0 means don't take number into account.	RO
AE	Audio_CH_Status[31:30]	7:6	reserved	RO
	Audio_CH_Status[29:28]	5:4	refer to IEC60958 p12 bit 29~28 [7:6]: Clock accuracy 00: Level II 01: Level I 10: Level III 11: Interface frame rate not matched to sampling frequency.	RO
	Audio_CH_Status[27:24] Sample FS	3:0	Sample frequency indicated in IEC60958-3 p11 bit 24~27. Sample frequency of software indicated 27..24 -------- 0000: 44.1 KHz 1000: 88.2 KHz 1100: 176.4 KHz 0110: 24 Khz 0010: 48Khz 1010: 96Khz 1110: 192KHz 0011: 32KHz 0001: sampling frequency not indicated. 1001: HBR	RO
AF	Audio_CH_Status[39:36] Original Sampling Frequency	7:4	Sample frequency indicated in IEC60958-3 p11 bit 24~27. Original Sampling Frequency 1111: 44.1 KHz 0111: 88.2 KHz 0011: 176.4 KHz 1001: 24 Khz 1101: 48Khz 0101: 96Khz 0001: 192KHz 1100: 32KHz 0000: sampling frequency not indicated. 0110: HBR	RO
	Audio_CH_Status[35:32] Sample Word Length	3:0	Audio sample word length 1101: 21 bits 1011: 24 bit 1001: 23 bit 0101: 22 bit 0011: 20 bit 0001: Word length not indicated 1100: 17 bit 1010: 20 bit 1000: 19 bit 0100: 18 bit 0010: 16 bit 0000: Word length not indicated	RO

By the information you can get the input audio if it is LPCM or compress audio, with the sample frequency.

Audio Output Configure

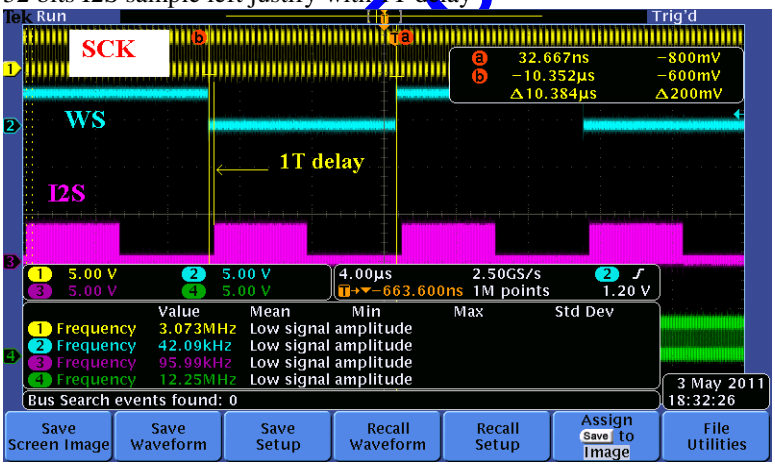
IT6801 can output I2S and SPDIF audio together, if one of the output source is not requirement, set the Reg52[4:0] bit to tri-state the output.

Reg	Name	Bit	Description	Type	Default Value
52	RegHCLKSel	7	HCLK source select when reg46h(6)=1	R/W	0
	RegEnSWHCLKSel	6	1: enable force HCLK source select	R/W	0
	RegDisVAutoMute	5	1: disable video auto mute	R/W	1
	RegTriSPDIF	4	1: Tri-state SPDIF IO	R/W	0
	RegTriI2SIO	3 2 1 0	Tristate Audio I2S0-I2S3 output buffer `1': Tri-state I2S source [3] IO output `1': Tri-state I2S source [2] IO output `1': Tri-state I2S source [1] IO output `1': Tri-state I2S source [0] IO output	R/W	0000

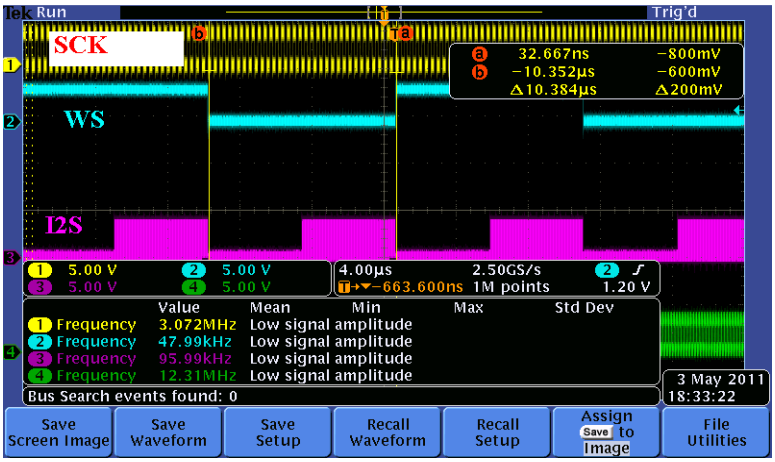
IT6801 only support three types of I2S format:

75	RegWS_Sel	7	0: WS high for right channel 1: WS low for right channel	R/W	0
	RegI2S_Width	6:2	I2S word length, only effective in right justified mode; Maximum 24 bits 11000b = 24 bits width 10000b = 16 bits widht	R/W	11000
	RegI2S_Mode	1:0	I2S output mode 00: 32bits I2S left justified with 1T delay; 01: 32bits I2S right justified mode 10: 32bits I2S left justified mode 0T delay; 11: reserved	R/W	00

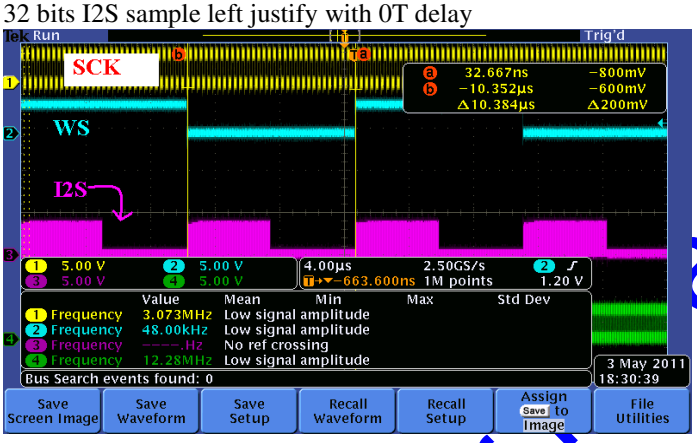
1. 32 bits I2S sample left justify with 1T delay



2. 32 bits I2S sample right justify



3. 32 bits I2S sample left justify with 0T delay



Reg75[1:0] controlled the output I2S mode.

HBR Output Selection

HBR audio carries the audio stream with much higher then 192KHz 2 channel SPDIF audio, therefore it is usually suggested output from I2S.

To output HBR from I2S[3:0] sources, Reg7E[6] ← '1'.

Error Handling

If the input audio has wrong sample frequency or anything unstable status, Reg07[7] and Reg07[6] interrupt will be raised. When detect the error, try to reset the Reg10[1] with writing '1' → '0' may solved this.

Chap 7 CBUS Message

Data On Link Layer are separated several channel with the packet format:

2 bit times	2 bits	1 bit	8 bits	1 bit	2 bit times
SYNC	Header	Control	Data or Command	Parity	ACK

Figure 7-2 Link Layer Packet Structure

For a field with more than one bit, the most significant bit of the field is sent first across CBUS, with each consecutive bit following, down to the least significant bit.

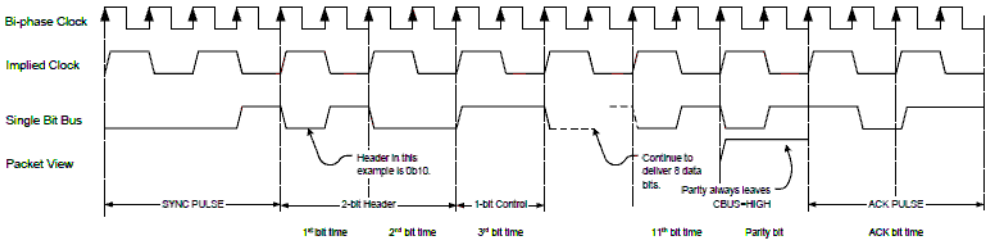


Figure 7-3 Link Layer Packet on the Control Bus

The CBUS is high when idle, due to the pull-up on the Source device.

And the header code encoding are the following table:

Header Bits	Description
00	DDC Packet
01	Vendor-specific packet
10	MHL Sideband Channel (MSC) packet
11	reserved

The control bit indicate the packet is control (command) or data.

Control Bit	Description
0	The following 8 bits are translation layer data
1	The following 8 bits are translation layer control

MSC Command

MHL Sideband Channel (MSC) packet are listed below:

Table 7-3. MSC Translation Layer Control Packets

Code	Control Packet	Description	Section	Notes
0x33	ACK	Command/Data byte acknowledged	7.3.1.1	1
0x34	NACK	Command/Data byte not acknowledged	7.3.1.2	1
0x35	ABORT	Transaction abort	7.3.1.3	1
0x60	WRITE_STAT	Write one byte to responder's status bytes.	7.4.3.8	2
	SET_INT	Write one or more interrupt bits in a byte.	7.4.3.9	2
0x61	READ_DEVCAP	Read one byte from responder's registers.	7.4.3.7	
0x62	GET_STATE	Read state from responder.	7.4.3.1	
0x63	GET_VENDOR_ID	Read vendor ID value from responder.	7.4.3.2	
0x64	SET_HPD	Set Hot Plug Detect in responder.	0	
0x65	CLR_HPD	Clear Hot Plug Detect in responder.	7.4.3.4	3
0x68	MSC_MSG	Send RCP or RAP code.	7.4.3.11	
0x69	GET_SC1_ERRORCODE	Get channel 1 command error code.		4
0x6A	GET_DDC_ERRORCODE	Get DDC channel command error code.	0	
0x6B	GET_MSC_ERRORCODE	Get MSC command error code.	7.4.3.6	
0x6C	WRITE_BURST	Write 1-16 bytes to responder's Scratchpad Registers.	7.4.3.10	
0x6D	GET_SC3_ERRORCODE	Get channel 3 command error code.		4
0x32	EOF	End of Frame.	7.4.3.10	1

IT6801 support the following MSC command with hardware or firmware control mode.

52	RegMSCHwMask[7:0]	7	WRITE_STAT/SET_INT hardware mask 0: handled by HW, 1: handle by FW	0
		6	READ_DEVCAP hardware mask 0: handled by HW, 1: handle by FW	0
		5	GET_MSC_ERRORCODE hardware mask 0: handled by HW, 1: handle by FW	0
		4	GET_DDC_ERRORCODE hardware mask 0: handled by HW, 1: handle by FW	0
		3	CLR_HPD hardware mask 0: handled by HW, 1: handle by FW	0
		2	SET_HPD hardware mask 0: handled by HW, 1: handle by FW	0
		1	GET_VENDOR_ID hardware mask 0: handled by HW, 1: handle by FW	0
		0	GET_STATE hardware mask 0: handled by HW, 1: handle by FW	0
53	RegMSCHwMask[15:8]	7	FW_MODE hardware mask 0: enable FW mode, 1: disable FW mode	1
		6		
		5		
		4		
		3		
		2		
		1	MSC_MSG hardware mask 0: handled by HW, 1: handle by FW	0
		0	WRITE_BURST hardware mask	0

			0: handled by HW, 1: handle by FW	

MSC provides register access through the MHL link, and offers four types of registers:

1. Capability Registers – readable across the link, inform each device about the opposite device's features.

2. Interrupt Registers – writeable across the link, inform a device about an event in the sending device, such as a change in link mode.

3. Status Register – writeable across the link, inform a device about the readiness of the sending device's register data.

4. Scratchpad Registers – writeable across the link, allows a device to send a message or a series of data bytes to the opposite device.

The registers are separates as the following table:

Resource Name	MSC Offset Range	Max. Size (bytes)	Req'd Size (bytes)	Size in CAP REG	Usage MHL CBUS	
					Access	Command
Capability Registers	0x00-0x0F	16	16	N/A	Read	READ_DEVCAP
Interrupt Registers	0x20-0x2F	16	4	0x0E[7:4]	Set Bits	SET_INT
Status Registers	0x30-0x3F	16	4	0x0E[3:0]	Write	WRITE_STAT
Scratchpad Registers	0x40-0x7F	64	16	0x0D	Write	WRITE_BURST

The MHL device capability registers of IT6801 are listed in the range (of MHL part)

MHL Device Register Space

Capability Register				
Reg	Name	Bit	Definition	Default
80	RegMHLCap00B	7:0	DEV_STATE[7:0]	0x00
81	RegMHLCap01B	7:4	MHL_VER_MAJOR[3:0]	0x2
		3:0	MHL_VER_MINOR[3:0]	0x0
82	RegMHLCap02B	7		000
		6:5	PLIM[1:0]	00
		4	POW	0
		3:0	DEV_TYPE[3:0]	0010
83	RegMHLCap03B	7:0	ADOPTER_ID_H[7:0]	0x00
84	RegMHLCap04B	7:0	ADOPTER_ID_L[7:0]	0x00
85	RegMHLCap05B	7:6		00
		5	SUPP_VGA	1
		4	SUPP_ISLANDS	1
		3	SUPP_PPIXEL	1
		2	SUPP_YCBCR422	1
		1	SUPP_YCBCR444	1
		0	SUPP_RGB444	1
86	RegMHLCap06B	7:2		000000
		1	AUD_8CH	1
		0	AUD_2CH	1
87	RegMHLCap07B	7	SUPP_VT	0
		6:4		000
		3	VT_GAME	0
		2	VT_CINEMA	0
		1	VT_PHOTO	0
		0	VT_GRAPHICS	0
88	RegMHLCap08B	7	LD_GUI	0
		6	LD_SPEAKE	0
		5	LD_RECORD	0

		4	LD_TUNER	0
		3	LD_MEDIA	0
		2	LD_AUDIO	1
		1	LD_VIDEO	1
		0	LD_DISPLAY	0
89	RegMHLCap09B	7:0	BANDWIDTH[7:0]	0x0F
8A	RegMHLCap10B	7:5		000
		4	UCP_RECV_SUPPORT	1
		3	UCP_SEND_SUPPORT	1
		2	SP_SUPPORT	1
		1	RAP_SUPPORT	1
		0	RCP_SUPPORT	1
8B	RegMHLCap11B	7:0	DEVICE_ID_H[7:0]	0x00
8C	RegMHLCap12B	7:0	DEVICE_ID_L[7:0]	0x00
8D	RegMHLCap13B	7:0	SCRATCHPAD_SIZE	0x10
8E	RegMHLCap14B	7:4	STAT_SIZE[3:0]	0x03
		3:0	INT_SIZE[3:0]	0x03
8F	RegMHLCap15B	7:0		0x00

The command can be read from MHL sink with *READ_DEVCAP* command.

MSC command provide the following device interrupt register, which allow a MHL device activate an interrupt to another MHL device, the interrupt registers on IT6801 listed below:

Interrupt Register				
A0	RegMHLInt00B	7:5	(Interrupt Status) Write '1' to clear this interrupt	000
		4	3D_REQ (Interrupt Status) Write '1' to clear this interrupt	0
		3	GNT_WRT (Interrupt Status) Write '1' to clear this interrupt	0
		2	REQ_WRT (Interrupt Status) Write '1' to clear this interrupt	0
		1	DSCR_CHG (Interrupt Status) Write '1' to clear this interrupt	0
		0	DCAP_CHG (Interrupt Status) Write '1' to clear this interrupt	0
A1	RegMHLInt01B	7:2	(Interrupt Status) Write '1' to clear this interrupt	0x00
		1	EDID_CHG (Interrupt Status) Write '1' to clear this interrupt	0
		0	(Interrupt Status) Write '1' to clear this interrupt	0
A2	RegMHLInt02B	7:0	(Interrupt Status) Write '1' to clear this interrupt	0x00
A3	RegMHLInt03B	7:0	(Interrupt Status) Write '1' to clear this interrupt	0x00

The MSC status register in IT6801 are listed below, which accept the update *WRITE_STATUS* command:

Status Register				
B0	RegMHLSts00B	7:1	Reserved	0x00
		0	DCAP_RDY (Read Only)	0
B1	RegMHLSts01B	7:5	Reserved	000
		4	MUTED (Read Only)	0
		3	PATH_EN (Read Only)	0
		2:0	CLK_MODE[2:0] (Read Only) 011: Normal 24-bit mode 010: PackedPixel mode others: reserved	011
B2	RegMHLSts02B	7:0	Reserved	0x00
B3	RegMHLSts03B	7:0	Reserved	0x00

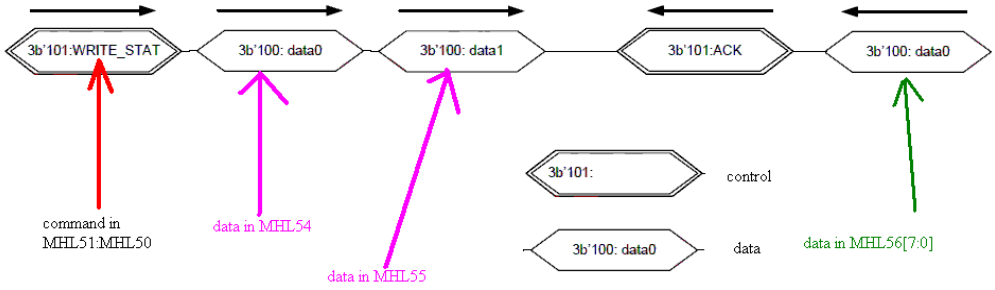
When sink update the status registers, it will activate an interrupt in MHL06[7:4].

Send An MSC Command

In IT6801, it implements the MSC command by hardware. Each command has a corresponding bit to trigger it, defined in the MHL50 and MHL51 as following:

Reg	Name	Bit	Definition	Default
50	RegMSCTxCmd[7:0]	7	WRITE_STAT/SET_INT Write '1' to trigger this MSC request	0
		6	READ_DEVCAP Write '1' to trigger this MSC request	0
		5	GET_MSC_ERRORCODE Write '1' to trigger this MSC request	0
		4	GET_DDC_ERRORCODE Write '1' to trigger this MSC request	0
		3	CLR_HPD (for MHL Sink only) Write '1' to trigger this MSC request	0
		2	SET_HPD (for MHL Sink only) Write '1' to trigger this MSC request	0
		1	GET_VENDOR_ID Write '1' to trigger this MSC request	0
		0	GET_STATE Write '1' to trigger this MSC request	0
51	RegMSCTxCmd[15:8]	7	FW_MODE Write '1' to trigger this FW request	0
		6		
		5		
		4		
		3		
		2		
		1	MSC_MSG Write '1' to trigger this MSC request	0
		0	WRITE_BURST Write '1' to trigger this MSC request	0

For each command required the following data, the data should be written into MHL54 for the first data and MHL55 for the following data, as following:



54	RegMSCTxValue0B[7:0]	7:0	Requester TX value byte 0	0x--
55	RegMSCTxValue1B[7:0]	7:0	Requester TX value byte 1	0x--

To send a command to requester, do with the following sequence:

1. Write the first data in MSC command into MHL54 (if necessary)
2. Write the second data in MSC command into MHL55 (if necessary)
3. Write the bit of command in MHL51:MHL50
4. Wait for MHL1C status if the MSC busy or check the MSC command fail interrupt.

1C		7:3		
	RMSCMSGBusy	2	RX MSG register is valid (Read Only)	-
	RCBusMSCBusy	1	CBUS MSC channel busy (Read Only)	-
	RCBusDDCBusy	0	CBUS DDC channel busy (Read Only)	-

If the MSC command with responder passed an data, as following figure:

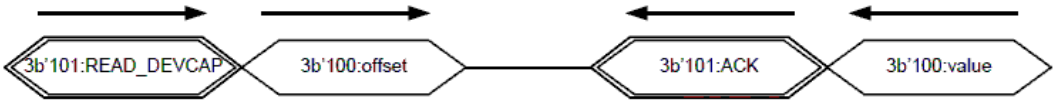


Figure 7-27 MSC Read Device Capability Command

The readback data will arrive after MSC channel not busy:

56	RMSCRxValue0B[7:0]	7:0	(Read Only) Requester RX value byte 0	0x--

WRITE_STAT/SET_INT

Follow the two diagrams, *SET_INT* and *WRITE_STAT* command are the same command code, and the same flow. These "two" commands just separated to the different destination offset. *SET_INT* command for update bit '1' into the device offset 0x20~0x2F for interrupt the responder, and *WRITE_STAT* command update one byte to the status register in the offset 0x30~0x3F.

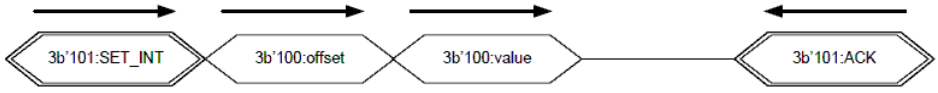
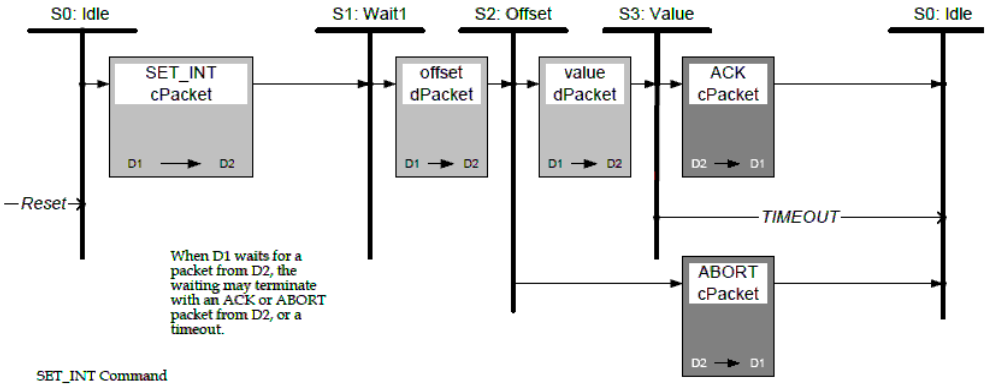


Figure 7-31 MSC Set Interrupt Command



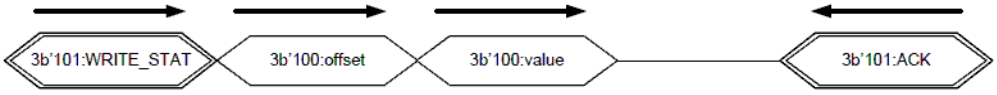
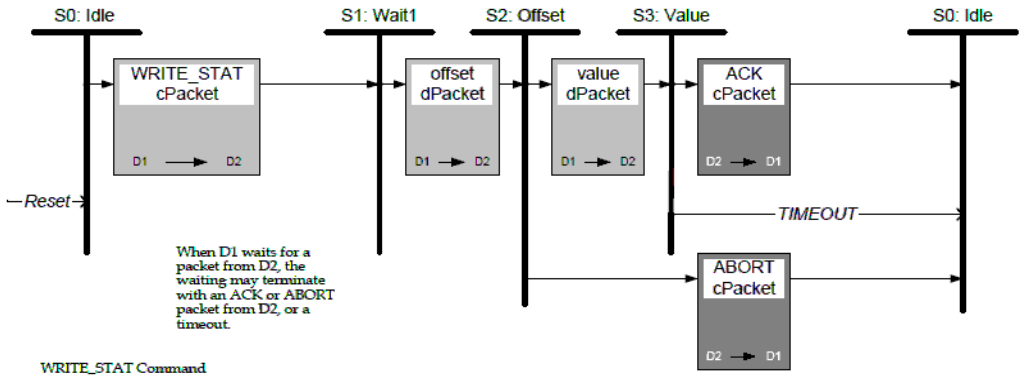


Figure 7-29 MSC Write Status Command



The command to activate an *SET_INT/WRITE_STAT* command on IT6801 is as follow:

1. MHL54 ← device space offset to update
2. MHL50 ← 0x80 // to trigger an *SET_INT/WRITE_STAT* command
3. Wait MHL1C[1] for '0' to check if it ready, or any fail interrupt in MHL05.

READ_DEVCAP

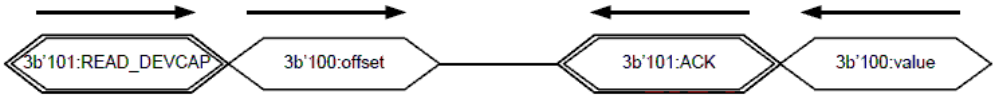


Figure 7-27 MSC Read Device Capability Command

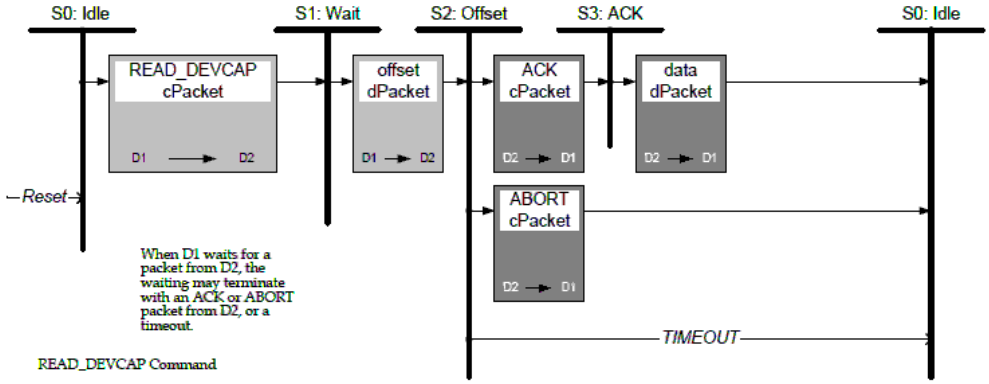


Figure 7-28 MSC READ_DEVCAP State Diagram

READ_DEVCAP command is to read the device space 0x00~0x0F from responder device. This command is used to read the device capability. This command should be activated after the status DCAP_RDY (MHLB0[0] = '1'), then the capability is available.

To issue a *READ_DEVCAP* command for one byte is the following sequence:

1. MHL54 ← offset to read
2. MHL50 ← 0x40 to read device capability
3. Wait for MHL1C[1] as '0' or fail. If MHL1C[1] is '0', means the data is ready.
4. If the read back data is ready, read the data from MHL56.

56	RMSCRxValue0B[7:0]	7:0	(Read Only) Requester RX value byte 0	0x--

GET_MSC_ERRORCODE

Figure 7-25 MSC GET_MSC_ERRORCODE Command

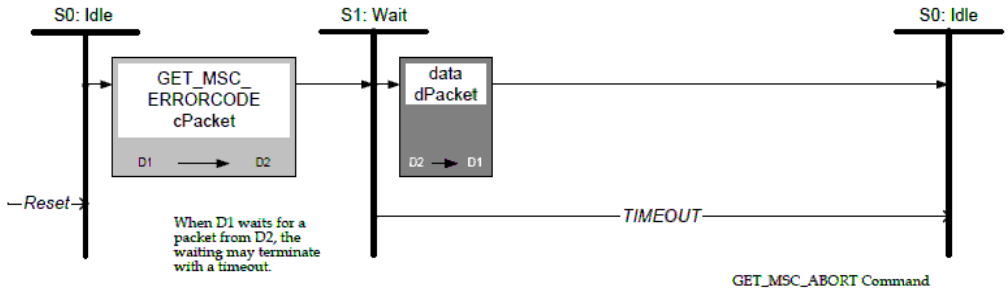


Figure 7-26 MSC GET_MSC_ERRORCODE State Diagram

This command is to read the MSC error code from responder.

1. MHL50 ← 0x20
2. Wait for MSC channel not busy or fail. If success ,
3. Get error code from MHL56.

GET_DDC_ERRORCODE

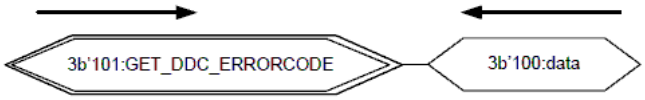


Figure 7-23 MSC GET_DDC_ERRORCODE Command

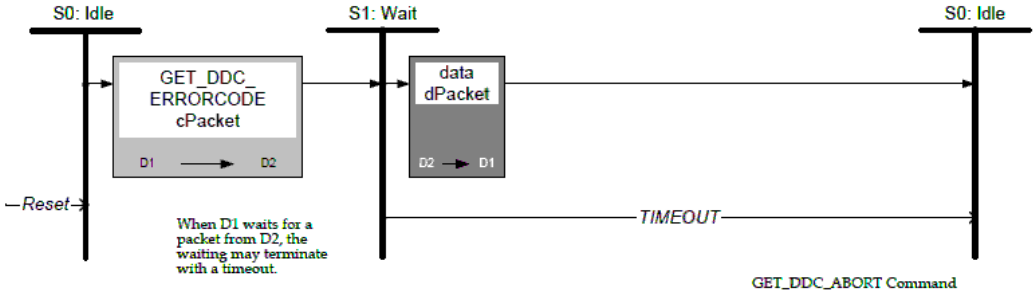


Figure 7-24 MSC GET_DDC_ERRORCODE State Diagram

This command is to read the DDC error code from responder.

1. MHL50 ← 0x10
2. Wait for MSC channel not busy or fail. If success,
3. Get error code from MHL56.

MSC_MSG

MSC_MSG command follows several command, such as

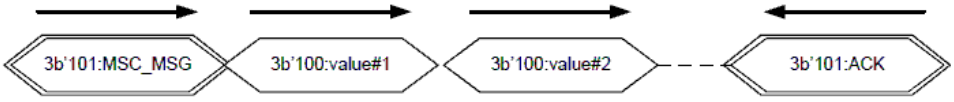


Figure 7-35 MSC MSG Command

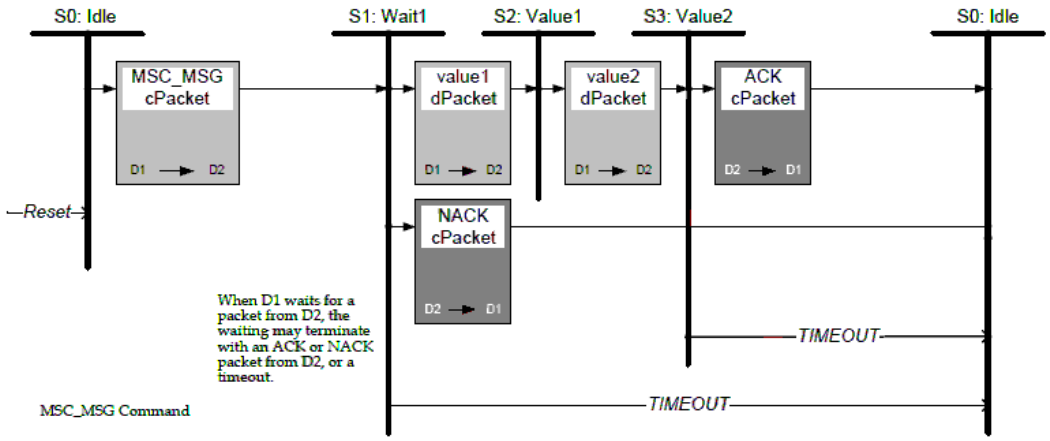


Figure 7-36 MSC MSC_MSG State Diagram

MSC_MSG command is used to transfer extension commands between two MHL devices, the first data of *MSC_MSG* command is the sub-command, and the second code are the op code. For each *MSC_MSG* command there is different protocol for each sub command.

To activate an *MSC_MSG* command on IT6801 is the follow sequence:

1. MHL51 ← 0x02
2. Wait for MSC channel not busy or fail. If success ,

The *MSC_MSG* sub commands are listed below:

Table 7-7. MSC Message Sub-commands

Command	Opcode	Description	Section
MSGE	0x02	MSC_MSG Error sub-command	7.4.3.12
RCP	0x10	Remote Control Protocol sub-command	7.7.1
RCPK	0x11	RCP Acknowledge sub-command	7.7.2
RCPE	0x12	RCP Error sub-command	7.7.3
RAP	0x20	Request Action Protocol sub-command	7.6.1
RAPK	0x21	RAP Acknowledge sub-command	7.6.2

During RCP/RAP protocol transition, there are several flow as the following diagram,

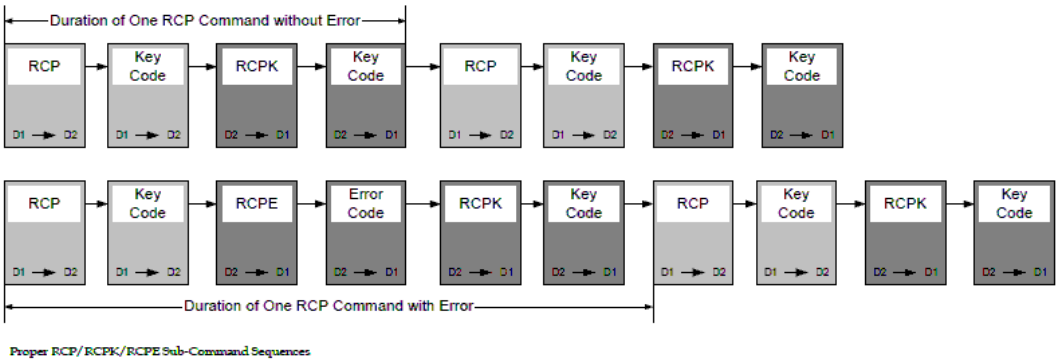


Figure 7-37 Proper MSC MSC_MSG Sub-command Sequencing

IT6801 also need to receive *MSC_MSG* command, when it need to activated a respond event, IT6801 us the command to activate a responding *MSC_MSG* command.

WRITE_BURST

MHL allow requester to write maximum up to 16 bytes into the scratch registers with *WRITE_BURST* command, with the following flow:

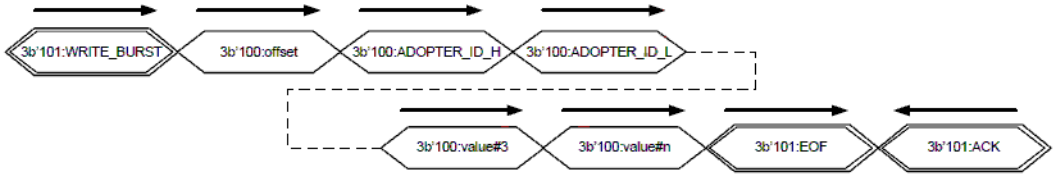


Figure 7-33 MSC Burst Write Command

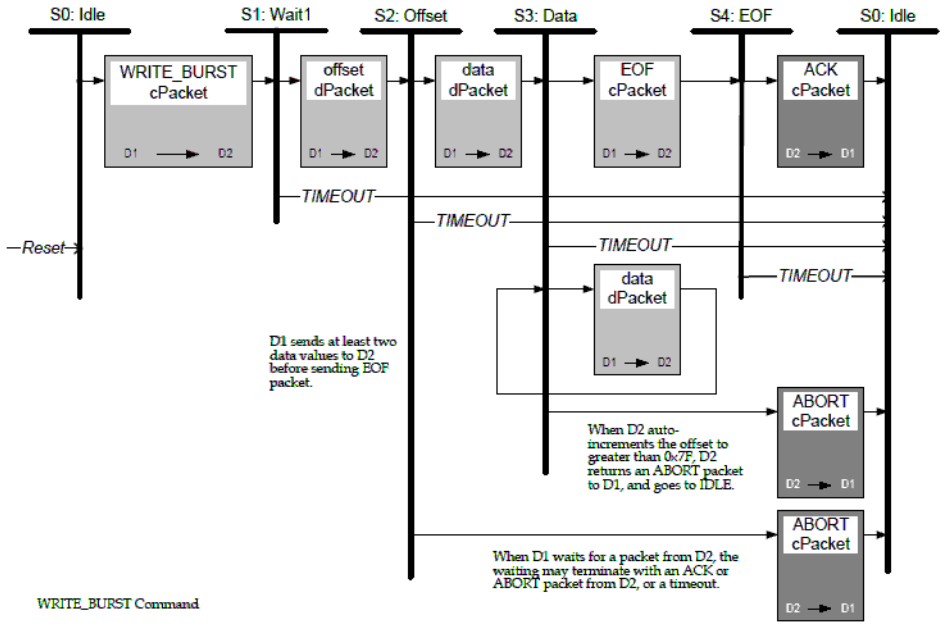


Figure 7-34 MSC WRITE_BURST State Diagram

Where the ADOPTER_ID is read from the responder device capability registers with *READ_DEVCAP* command, and the burst should by the sequence:

1. Use *SET_INT* command activate an *REQ_WRT interrupt (offset 0x20, bit[2])* to responder.
2. Wait for the MHL Interrupt *RegMHLInt00B[3]* (GNT_WRT) was activated to '1' by interrupt handler. When receive the interrupt, IT6801 can begin to activate an *WRITE_BURST* command.
3. Set MHL00[7] = '0'.
4. Write the *ADAPTOR_ID_H* and *ADAPTOR_ID_L* into the registers MHL5E and MHL5F.
5. *MHL5C[0] ← '1', to clear TX packet FIFO*.
6. Write *EACH* written data into MHL59. MHL59 is the scratch FIFO registers, write the data to update responder into the MHL59 in the transmitting order. Cannot over 16 bytes.
7. Write MHL51 ← 0x01 to activate an *WRITE_BURST* command.
8. After complete, activate an *SET_INT* with *DCSR_CHG* interrupt to the interrupt registers of responder.

Received an MSC Command

IT6801 implement the default interrupt for MSC command such as WRITE_STATE, or SET_INT, the status is corresponded in the interrupt status.

MSC_MSG Receiving

Refer the MHL04[4] interrupt status, when MHL04[4] is activated as '1', IT6801 received an *MSC_MSG* command. When this interrupt is '1', read the received *MSC_MSG* command in MHL60/MHL61:

60	RMSGRxValue0B[7:0]	7:0	(Read Only) MSC_MSG responder RX value byte 0	0x--
61	RMSGRxValue1B[7:0]	7:0	(Read Only) MSC_MSG responder RX value byte 1	0x--

After received the *MSC_MSG* command, then depends on the sub-command (in RMSGRxValue0B) and opcode (in RMSGRxValue1B) to process.

WRITE_BURST Receiving

When IT6801 as a responder of the MHL sink *MSC WRITE_BURST* command, it will receive an *REQ_WRT interrupt* in MHLA0[2]. When the system is ready to receive the burst written data, IT6801 should activate a *SET_INT* with *GNT_WRT (RegMHLInt00B[3])* bit to the MHL sink.

The MHL sink will activate a *WRITE_BURST* command to IT6801, and *EOF* with an *DSCR_CHG* interrupt in MHLA0[1]. MCU can read the written data from MHLC0~MHLCF with I^2C interface, and read the write count in MHL64[4:0].

64		7:5		
	RMSCRxScrPadNum[4:0]	4:0	(Read Only) Receive scratch pad byte number	0x--

Chap 8 CEC Handling

IT6801 CEC software functionality is separated into the following parts：

(1) Initial

(2) CECManager

-- IT6801_CECReceiver

-- IT6801_CECDecoder

-- IT6801_CECTransmitter

Initial

1. Set HDMI Reg0E[7]='1' for Enable IT6801 CEC Block.

2. Set HDMI Reg86=0xC1 for indicate IT6801 CEC I2C slave address to 0xC0.

3. Through I2C slave address 0xC0 to initial related register of IT6801 CEC for setup the CEC Timing control and Logical Address setting.

100 ms Timing control for CEC Bit timing calibration

1. Set CEC09[0]='1' to start 100ms counter by user MCU.

2. Set CEC09[0]='0' to stop 100ms counter

3. Read CEC47~CEC45 then divide 1000 for get 100us count value

4. Set 100us count value to CEC0C (REG_TIMER_UNIT)

(CEC0C default value is 0x59)

Logical Address setting

To Set CEC22 (CEC Logic Address) for identify CEC logical Address of IT6801 to receive and transfer belong to CEC command of IT6801.

CECManager

Responsible for CEC command handler, including the Receiver, Decoder, and Transmitter.

Receiver of CEC command

IT6801 according to CEC22 (CEC Logic Address) setting, to receive the respective CEC command, and through pin 16 (INT) interrupt generated to inform MCU interrupt routine that IT6801_CECReceiver will according to CEC4C (Interrupt Status) to do the action.

If CEC4C[4]='1' (RX_DONE_INT) then read CEC30~CEC42 (CEC Rx Buffer) to Queue of software by AddQ function.

Decoder of CEC command

1. Get CEC command from Queue that receive CEC command from CEC30 ~ CEC42(Rx Buffer).

2. According OP code to do the action.

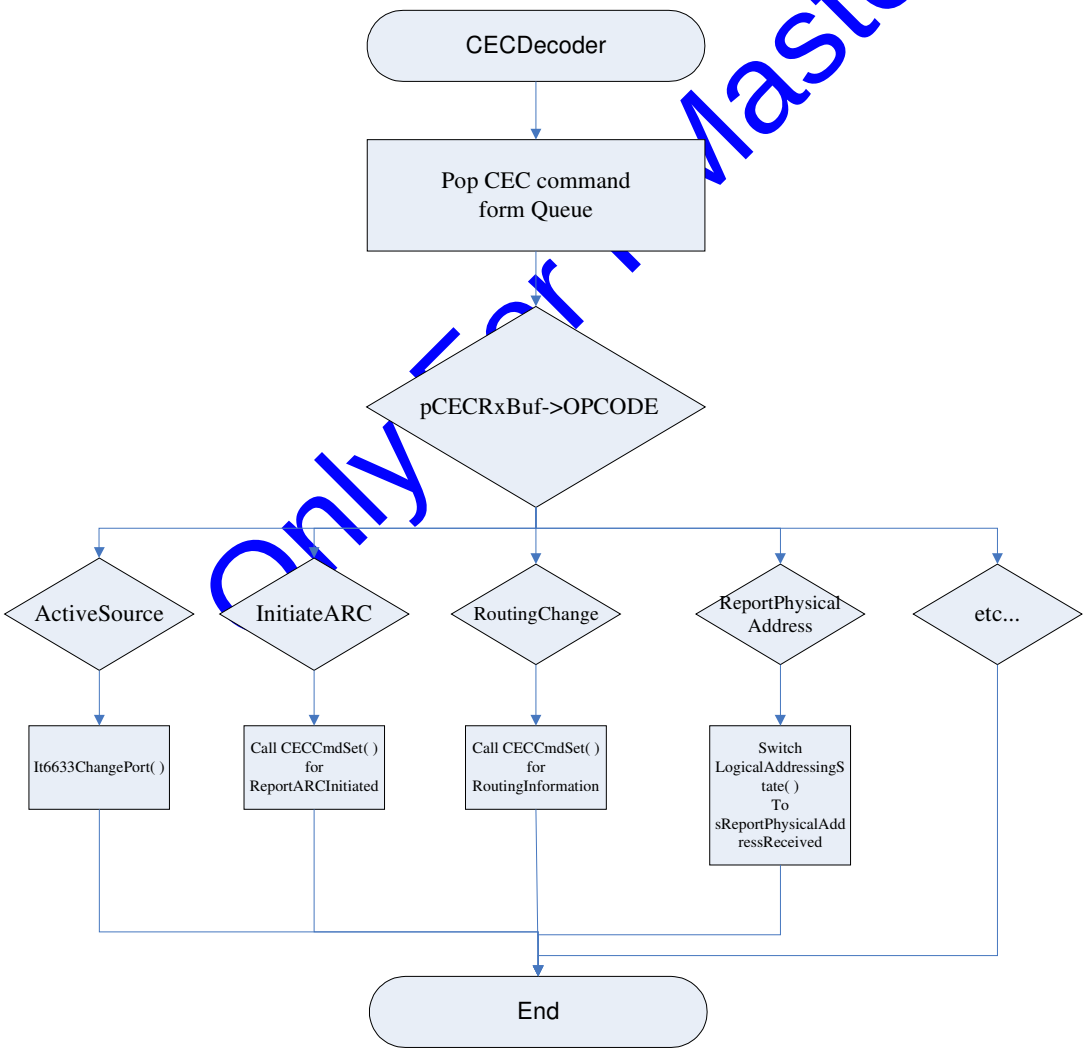
Example:

Active Source (OP code = 0x82),

➔ AVR and TV need to change HDMI port according to physical address of Active Source command.

Initiate ARC (OP code = 0xC0)

➔ IT6801 need to set CEC25[3]=1 (Enable S/PDIF output) and CEC25[1]=1 (Enable ARC Rx) then response command of Report ARC initiated to TV by switch_ARCState(sReportARCInitiated).



CEC command Transmission

1. Call *CECCmdSet()* to setup TxCmdBuf for transfer CEC command.

2. *IT6801_CECTransmitter()* will waiting for CEC44[6] ready to fire and CEC44[1] bus free then write CEC10 ~ CEC23 (CEC Tx Buffer) from TxCmdBuf to transfer CEC command.

Chap 9 Register List

HDMI Registers of IT6801

HDMI Registers I^2C address is 0x90 (PCADR = LOW) or 0x92 (PCADR = HIGH)

W1C：Write 1 Clear
W1P：Write 1 generate pulse
RO：Read Only
R/W：Read and Write

Reg	Register Name	Bit	Definition	Type	Default Value
Device Information					
00	VendorID[7:0]	7:0	Vendor ID Low Byte	RO	0x54
01	VendorID[15:8]	7:0	Vendor ID High Byte	RO	0x49
02	DeviceID[7:0]	7:0	Device ID Low Byte	RO	0x02
03	DeviceID[15:8]	7:0	Devicd ID High Byte	RO	0x68
04	RevID	7:0	Device Revision ID	RO	0xA0
Interrupt					
05	P0_HDCPOff_Det	7	Port 0 HDCP off detect Interrupt	W1C	
	P0_ECCErrTrg	6	Port 0 ECC error Interrupt	W1C	
	P0_HDMIMode_Chg	5	Port 0 HDMI/DVI mode change Interrupt	W1C	
	P0_HDCP_Auth_Done	4	Port 0 HDCP authentication done Interrupt	W1C	
	P0_HDCP_Auth_Start	3	Port 0 HDCP authentication start Interrupt	W1C	
	P0_RxCLK_StbChg	2	Port 0 Rx Clock stable change Interrupt	W1C	
	P0_RxCLKOn_Det	1	Port 0 Rx Clock on detect Interrupt	W1C	
	P0_PWR5V_Chg	0	Port 0 power 5V state change Interrupt	W1C	
06	P1_HDCPOff_Det	7	Port 1 HDCP off detect Interrupt	W1C	
	P1_ECCErrTrg	6	Port 1 ECC error Interrupt	W1C	
	P1_HDMIMode_Chg	5	Port 1 HDMI/DVI mode change Interrupt	W1C	
	P1_HDCP_Auth_Done	4	Port 1 HDCP authentication done Interrupt	W1C	
	P1_HDCP_Auth_Start	3	Port 1 HDCP authentication start Interrupt	W1C	
	P1_RxCLK_StbChgt	2	Port 1 Rx Clock stable change Interrupt	W1C	
	P1_RxCLKOn_Det	1	Port 1 Rx Clock on detect Interrupt	W1C	
	P1_PWR5V_Chg	0	Port 1 power 5V state change Interrupt	W1C	
07	AudioFIFOError	7	Audio FIFO error Interrupt	W1C	
	AutoAudioMute	6	Audio Auto Mute Interrupt	W1C	
	PktLeftMute	5	Left Mute Packet is received Interrupt	W1C	
	PktSetMute	4	Set Mute Packet is received Interrupt	W1C	
	TimerInt	3	Timer count to setting value Interrupt	W1C	
	VideoModeChg	2	Input Video Mode Change Interrupt	W1C	
	SCDTChg	1	Video Stable State Change Interrupt	W1C	
	MHLModeChg	0	MHL/HDMI mode change Interrupt	W1C	
08	NoGenPkt2_Rcv	7	No AVI packet is received	W1C	
	NoGenPkt_Rcv	6	No GenPkt is received	W1C	
	NoAud_Rcv	5	No Audio InfoFrame is received	W1C	
	NoAVI_Rcv	4	No AVI InfoFrame is received	W1C	
	CD_Det	3	Color Depth change Interrupt	W1C	
	GenPkt_Det	2	General packet detect Interrupt	W1C	
	ISRC2_Det	1	ISRC2 packet detect Interrupt	W1C	
	ISRC1_Det	0	ISRC1 packet detect Interrupt	W1C	
09	H2VSkewFail	7	Port 0 H2V FIFO Fail interrupt		
	P1_DeSkewErr	6	Port 1 deskew error interrupt	W1C	
	P0_DeSkewErr	5	Port 0 deskew error interrupt	W1C	
	NewAudioPkt_Det	4	New Audio Packet detect Interrupt	W1C	
	NewACPPkt_Det	3	New ACP Packet detect Interrupt	W1C	
	NewSPDPkt_Det	2	New SPD Packet detect Interrupt	W1C	
	NewMPEGPkt_Det	1	New MPEG Packet detect Interrupt	W1C	
	NewAVIPkt_Det	0	New AVI InfoFrame detect Interrupt	W1C	
Device internal status					
0A	P0_SCDT	7	Port 0 Video is stable	RO	
	P0_MHLMode	6	Port 0 MHL(1)/HDMI(0) mode	RO	

	P0_IPLL_LOCK	5	Port 0 IPLL is locked	RO	
	P0_IPLL_HS	4	Port 0 IPLL clock is higher than 80MHz	RO	
	P0_RxCLK_Valid	3	Port 0 Rx clock is valid	RO	
	P0_RxCLK_Detect	2	Port 0 Rx clock detect	RO	
	P0_HDMI_Mode	1	Port 0 HDMI(1)/DVI(0) mode	RO	
	P0_PWR5V_Det	0	Port 0 power 5V detect	RO	
0B	P1_SCDT	7	Video is stable	RO	
	P1_OLOCK	6	OPLL is locked	RO	
	P1_IPLL_LOCK	5	Port 1 IPLL is locked	RO	
	P1_IPLL_HS	4	Port 1 IPLL clock is higher than 80MHz	RO	
	P1_RxCLK_Valid	3	Port 1 Rx clock is valid	RO	
	P1_RxCLK_Detect	2	Port 1 Rx clock detect	RO	
	P1_HDMI_Mode	1	Port 1 HDMI(1)/DVI(0) mode	RO	
	P1_PWR5V_Det	0	Port 1 power 5V detect	RO	
0C	P1_RxCLK_Stable	7	Port 1 clock is stabled	RO	
	P0_RxCLK_Stable	6	Port 0 clock is stabled	RO	
	MHL3DFreSeq	5	Receive MHL frame sequence 3D InfoFrame	RO	
	ARAM_bo_doneHQ	4	Audio RAM BIST Done	RO	
	Reserved	3		RO	
	Reserved	2		RO	
	Reserved	1		RO	
	Reserved	0		RO	
Device Reset/Clock/PowerDown related register					
0D	Reserved	7:3			
	RegEnPIXCLKB2	2	1: Enable PIXCLKB for video detect	R/W	1
	RegEnBGRCLK	1	1: Enable RCLK for port 1 internal EDID I2C	R/W	1
	RegEnAGRCLK	0	1: Enable RCLK for port 0 internal EDID I2C	R/W	1
0E	RegEnNMRCLK	7	1: Enable RCLK for MHL NMRCLK domain	R/W	1
	RegEnGMRCLK	6	1: Enable RCLK for MHL GMRCLK domain	R/W	1
	RegEnGH3RCLK	5	1: Enable RCLK for port 1 frontend logic	R/W	1
	RegEnGH2RCLK	4	1: Enable RCLK for port 0 frontend logic	R/W	1
	RegEnGH1RCLK	3	1: Enable RCLK for backend logic	R/W	1
	RegEnNH2RCLK	2	1: Enable RCLK for Registers	R/W	1
	RegEnERCLK	1	1: Enable RCLK for internal EDID R/W	R/W	1
	RegEnCRCLK	0	1: Enable RCLK for CEC	R/W	0
0F	Reserved	7:2			
	Reg_Block_Sel	1:0	Register block select	R/W	00
10	RegPWDACLK	7	1: Power down Audio clock domain	R/W	0
	RegPWDPCLK	6	1: Power down Pixel clock domain	R/W	0
	RegEn_AutoAUDRst	5	1: Enable auto audio reset	R/W	0
	RegEn_AutoVDORst	4	1: Enable auto video reset	R/W	0
	RegRegRst	3	1: Register block reset	R/W	0
	RegEnIntRst	2	1: Interrupt logic reset	R/W	0
	RegAudRst	1	1: Audio logic reset	R/W	0
	RegVdoRst	0	1: Video logic reset	R/W	0
11	Reg_P0_EnCKRst	7	1: Enable Port 0 Auto reset when clock is not stable	R/W	0
	Reg_P0_EnHDCPRst	6	1: Enable Port 0 HDCP	R/W	0
	Reg_P0_EnAutoRst	5	1: Enable Port 0 Auto reset	R/W	0
	Reg_P0_EQRst	4	1: Port 0 EQ logic reset	R/W	0
	Reg_P0_DCLKRst	3	1: Port 0 CLKD5 domain logic reset	R/W	0
	Reg_P0_CDRDataRst	2	1: Port 0 CDR Data logic reset	R/W	0
	Reg_P0_HDCPRst	1	1: Port 0 HDCP logic reset	R/W	0
	Reg_P0_SWRst	0	1: Port 0 all logic reset	R/W	0
12	RegDisvRst	7	1: MHL discovery logic reset	R/W	0
	RegLinkRst	6	1: MHL link logic reset	R/W	0
	RegMSCRst	5	1: MHL MSC logic reset	R/W	0
	RegDDCRst	4	1: MHL DDC logic reset	R/W	0
	RegORst	3	1: MHL OCLK domain logic reset	R/W	0
	Reg_P0_IPLLRst	2	1: Port 0 IPLL reset	R/W	0
	Reg_P0_OPLLRst	1	1: Port 0 OPLL reset	R/W	0
	Reg_P0_APLLRst	0	1: Port 0 APLL reset	R/W	0
13	Reg_P0_OPLLPWD	7	1: Port 0 OPLL power down	R/W	0
	Reg_P0_IPLLPWD	6	1: Port 0 IPLL power down	R/W	0
	Reg_P0_IPLLPWDI	5	1: Port 0 IPLL current bias power down	R/W	0
	Reg_P0_APLLPWD	4	1: Port 0 APLL power down	R/W	0
	Reg_P0_PWDTOP	3	1: Port 0 all digital logic and APLL power down	R/W	0
	Reg_P0_BRST_RCVR	2	1: Port 0 AFE channel 0 decoder reset	R/W	0

	Reg_P0_GRST_RCVR	1	1: Port 0 AFE channel 1 decoder reset	R/W	0
	Reg_P0_RRST_RCVR	0	1: Port 0 AFE channel 2 decoder reset	R/W	0
14	Reg_P0_CLKPWDRTERM	7	1: Port 0 Clock differential pair termination power down	R/W	0
	Reg_P0_CH2PWDRTERM	6	1: Port 0 channel 2 differential pair termination power down	R/W	0
	Reg_P0_CH1PWDRTERM	5	1: Port 0 channel 1 differential pair termination power down	R/W	0
	Reg_P0_CH0PWDRTERM	4	1: Port 0 channel 0 differential pair termination power down	R/W	0
	Reg_P0_CH2PWD	3	1: Port 0 channel 2 differential pair power down	R/W	0
	Reg_P0_CH1PWD	2	1: Port 0 channel 1 differential pair power down	R/W	0
	Reg_P0_CH0PWD	1	1: Port 0 channel 0 differential pair power down	R/W	0
	Reg_P0_ETCPWD	0	1: Port 0 clock differential pair power down	R/W	0
15	Reg_P0_CH2CLKD5PWD	7	1: Port 0 channel 2 CLKD5 power down	R/W	0
	Reg_P0_CH1CLKD5PWD	6	1: Port 0 channel 1 CLKD5 power down	R/W	0
	Reg_P0_CH0CLKD5PWD	5	1: Port 0 channel 0 CLKD5 power down	R/W	0
	Reg_P0_CH2CLKD4PWD	4	1: Port 0 channel 2 CLKD4 power down	R/W	0
	Reg_P0_CH1CLKD4PWD	3	1: Port 0 channel 1 CLKD4 power down	R/W	0
	Reg_P0_CH0CLKD4PWD	2	1: Port 0 channel 0 CLKD4 power down	R/W	0
	Reg_P0_EQPWD	1	1: Port 0 AFE EQ power down	R/W	0
	Reg_P0_PWDAFEAll	0	1: Port 0 All AFEs power down	R/W	0
16	Reg_P0_EnAutoPwdBTERM	7	1: Enable Port 0 B Channel termination auto power down	R/W	1
	Reg_P0_EnAutoPwdTCLK	6	1: Enable Port 0 TCLK auto power down	R/W	0
	Reg_P0_EnAutoPwdTERM	5	1: Enable Port 0 termination auto power down	R/W	0
	Reg_P0_EnAutoPwdCDREQ	4	1: Enable Port 0 CDR EQ auto power down	R/W	0
	Reg_P0_EnAutoPwdCLKD5	3	1: Enable Port 0 CLKD5 auto power down	R/W	0
	Reg_P0_EnAutoPwdCLKD4	2	1: Enable Port 0 CLKD4 auto power down	R/W	0
	Reg_P0_EnRxAutoPwdPLL	1	1: Enable Port 0 PLL auto power down	R/W	0
	Reg_P0_EnRxAutoPwdAFE	0	1: Enable Port 0 RXAFE auto power down	R/W	0
17	Reg_P0_InvHCLK	7	1: Inverse Port 0 input HCLK	R/W	1
	Reg_P0_InvCLKD5I	6	1: Inverse Port 0 input CLKD5I	R/W	1
	Reg_P0_RDetClkHigh	5	1: IPLL in high speed mode when Reg17h(3)=1	R/W	0
	Reg_P0_RDetClkRdy	4	1: Input Clock Ready when Reg17h(3)=1	R/W	0
	Reg_P0_RSetCLK	3	1: SW force IPLL speed mode and Input clock ready	R/W	0
	Reg_P0_CKValidSel	2	Clock valid condition selector. 1: Clock detect ; 0: Clock valid	R/W	0
	Reg_P0_IgnClkRdyPwd	1	1: Ignore clock ready signal	R/W	0
	Reg_P0_DISMHLPWD	0	1: Disable MHL mode auto power down	R/W	0
18	Reg_P1_EnCKRst	7	1: Enable Port 1 Auto reset when clock is not stable	R/W	0
	Reg_P1_EnHDCPRst	6	1: Enable Port 1 HDCP	R/W	0
	Reg_P1_EnAutoRst	5	1: Enable Port 1 Auto reset	R/W	0
	Reg_P1_EQRst	4	1: Port 1 EQ logic reset	R/W	0
	Reg_P1_DCLKRst	3	1: Port 1 CLKD5 domain logic reset	R/W	0
	Reg_P1_CDRDataRst	2	1: Port 1 CDR Data logic reset	R/W	0
	Reg_P1_HDCPRst	1	1: Port 1 HDCP logic reset	R/W	0
	Reg_P1_SWRst	0	1: Port 1 all logic reset	R/W	0
19	Reserved	7:3			
	Reg_P1_IPLLRst	2	1: Port 1 IPLL reset	R/W	0
	Reserved	1:0			
1A	Reserved				
	Reg_P1_IPLLPWD	6	1: Port 1 IPLL power down	R/W	0
	Reg_P1_IPLLPWDI	5	1: Port 1 IPLL current bias power down	R/W	0
	Reserved	4			
	Reg_P1_PWDTOP	3	1: Port 1 all digital logic and APLL power down	R/W	0
	Reg_P1_BRST_RCVR	2	1: Port 1 AFE channel 0 decoder reset	R/W	0
	Reg_P1_GRST_RCVR	1	1: Port 1 AFE channel 1 decoder reset	R/W	0
	Reg_P1_RRST_RCVR	0	1: Port 1 AFE channel 2 decoder reset	R/W	0
1B	Reserved				
	Reg_P1_CH2PWDRTERM	6	1: Port 1 channel 2 differential pair termination power down	R/W	0
	Reg_P1_CH1PWDRTERM	5	1: Port 1 channel 1 differential pair termination power down	R/W	0
	Reg_P1_CH0PWDRTERM	4	1: Port 1 channel 0 differential pair termination power down	R/W	0
	Reg_P1_CH2PWD	3	1: Port 1 channel 2 differential pair power down	R/W	0
	Reg_P1_CH1PWD	2	1: Port 1 channel 1 differential pair power down	R/W	0

	Reg_P1_CH0PWD	1	1: Port 1 channel 0 differential pair power down	R/W	0
	Reg_P1_ETCPWD	0	1: Port 1 clock differential pair power down	R/W	0
1C	Reg_P1_CH2CLKD5PWD	7	1: Port 1 channel 2 CLKD5 power down	R/W	0
	Reg_P1_CH1CLKD5PWD	6	1: Port 1 channel 1 CLKD5 power down	R/W	0
	Reg_P1_CH0CLKD5PWD	5	1: Port 1 channel 0 CLKD5 power down	R/W	0
	Reg_P1_CH2CLKD4PWD	4	1: Port 1 channel 2 CLKD4 power down	R/W	0
	Reg_P1_CH1CLKD4PWD	3	1: Port 1 channel 1 CLKD4 power down	R/W	0
	Reg_P1_CH0CLKD4PWD	2	1: Port 1 channel 0 CLKD4 power down	R/W	0
	Reg_P1_EQPWD	1	1: Port 1 AFE EQ power down	R/W	0
	Reg_P1_PWDAFEAll	0	1: Port 1 All AFEs power down	R/W	0
1D	Reserved	7			
	Reg_P1_EnAutoPwdTCLK	6	1: Enable Port 0 TCLK auto power down	R/W	0
	Reg_P1_EnAutoPwdTERM	5	1: Enable Port 0 termination auto power down	R/W	0
	Reg_P1_EnAutoPwdCDREQ	4	1: Enable Port 0 CDR EQ auto power down	R/W	0
	Reg_P1_EnAutoPwdCLKD5	3	1: Enable Port 0 CLKD5 auto power down	R/W	0
	Reg_P1_EnAutoPwdCLKD4	2	1: Enable Port 0 CLKD4 auto power down	R/W	0
	Reg_P1_EnRxAutoPwdPLL	1	1: Enable Port 0 PLL auto power down	R/W	0
	Reg_P1_EnRxAutoPwdAFE	0	1: Enable Port 0 RXAFE auto power down	R/W	0
1E	Reg_P1_InvTMDSCLK	7	1: Inverse Port 1 input TMDSCLK	R/W	1
	Reg_P1_InvCLKD5I	6	1: Inverse Port 1 input CLKD5I	R/W	1
	Reg_P1_RDetClkHigh	5	1: IPLL in high speed mode when Reg1Eh(3)=1	R/W	0
	Reg_P1_RDetClkRdy	4	1: Input Clock Ready when Reg1Eh(3)=1	R/W	0
	Reg_P1_RSetCLK	3	1: SW force IPLL speed mode and Input clock ready	R/W	0
	Reg_P1_CKValidSel	2	Clock valid condition selector. 1: Clock detect ; 0: Clock valid	R/W	0
	Reg_P1_IgnClkRdyPwd	1	1: Ignore clock ready signal	R/W	0
	Reserved	0			
1F	Reserved	7			
	Reg_P1_GateWDOGCLK	6	1: gate Port 1 watchdog clock	R/W	0
	Reg_P1_GateTMDSCLK	5	1: gate Port 1 TMDS clock	R/W	0
	Reg_P1_GateEQCLK	4	1: gate Port 1 EQ clock	R/W	0
	Reg_P0_GateHCLK	3	1: gate Port 0 HCLK clock	R/W	0
	Reg_P0_GateWDOGCLK	2	1: gate Port 0 watchdog clock	R/W	0
	Reg_P0_GateTMDSCLK	1	1: gate Port 0 TMDS clock	R/W	0
	Reg_P0_GateEQCLK	0	1: gate Port 0 EQ clock	R/W	0

MHL/HDMI Front End Control

MHL/HDMI FrontEnd control					
20	Reserved	7			
	Reg_P0_EnEQFailRty	6	1: enable EQ retry when EQ failed	R/W	0
	Reg_P0_R_CS	5:4	R_CS initial value	R/W	00
	Reg_P0_G_CS	3:2	G_CS initial value	R/W	00
	Reg_P0_B_CS	1:0	B_CS initial value	R/W	00
21	Reg_P0_DFIFOCtrl[3:0]	7:4	De-serialize control register[3:0]	R/W	1001
	Reg_P0_BypassFIFO	3	1: bypass 10bit FIFO 0: normal	R/W	0
	Reg_P0_EnDatadbg_B	2	1: enable channel 0 data debug	R/W	0
	Reg_P0_EnDatadbg_G	1	1: enable channel 1 data debug	R/W	0
	Reg_P0_EnDatadbg_R	0	1: enable channel 2 data debug	R/W	0
22	Reg_P0_MDFE	7	0: Manual DFE calculation mode 1: auto DFE calculation mode	R/W	0
	Reg_P0_ENDFE	6	0: DFE is not active 1: DFE is active	R/W	0
	Reg_P0_AutoAMP	5	1: up/dn signal by AutoEQ is active 0: up/dn signal by AutoEQ is not active	R/W	0
	Reg_P0_AutoEQ	4	1: RS updated with AutoEQ 0: RS hold	R/W	0
	Reg_P0_AutoEQPWDB	3	1: AutoEQ is enabled 0: AutoEQ is power down	R/W	0
	Reg_P0_ACTRIG	2	Writing '1' to this bit will trigger one time AutoEQ calculation	R/W	0
	Reg_P0_CDRDbgsel	1:0	CDR debug selector	R/W	00
23	Reg_P0_G_FSD	7:4	FSD value of Ch1	R/W	0000
	Reg_P0_B_FSD	3:0	FSD value of Ch0	R/W	0000
24	Reserved	7			
	Reg_P0_MCHSEL	6:4	Channel selected to do EQ calculation in manual mode	R/W	000
	Reg_P0_R_FSD	3:0	FSD value of Ch2	R/W	0000
25	Reg_P0_FAMP	7	AutoEQ option	R/W	0
	Reg_P0_MAMP	6:0	Manually set value of REFAMP	R/W	0000000
26	Reg_P0_EnClkStb2TrgEQ	7	1: enable clock stable to trigger AUTOEQ	R/W	0
	Reg_P0_DisSymlock	6	1: disable symbol lock and bypass to output 0: enable symbol lock	R/W	0
	Reg_P0_OvWrRSCS	5	1: Manually set RS value 0: RS value decided by autoEQ	R/W	0
	Reg_P0_EnEQdbg	4	1: enable EQ debug	R/W	0
	Reg_P0_CTRUN	3	AutoEQ option	R/W	0
	Reg_P0_SelEQDbg	2:0	EQ debug selector	R/W	000
27	Reg_P0_UseBValue	7	1: all 3 channels use RS value of 0x27 when Reg_SetEQ='1' 0: RGB use individual RS values	R/W	0
	Reg_P0_B_RS	6:0	RS value of CH0 if Reg_SetEQ='1'	R/W	0000000
28	Reserved	7			
	Reg_P0_G_RS	6:0	RS value of CH1 if Reg_SetEQ='1'	R/W	0000000
29	Reserved	7			
	Reg_P0_R_RS	6:0	RS value of CH2 if Reg_SetEQ='1'	R/W	0000000
2A	Reserved	7:6			
	Reg_P0_HWByPassFIFO	5	1: Enable HW Bypass CLKD5 Data FIFO	R/W	1
	Reg_P0_EnPLLBufRst	4	1: Enable CLKD5 Data FIFO auto-reset	R/W	1
	Reg_P0_IPStableTime	3:2	1: IPLL stable time select 01: 50us ; 10: 100us ; others: 75us	R/W	00
	Reg_P0_EnCLKVldChk	1	1: Enable Check CLK_Valid when CLKD5 FIFO auto-reset is enabled.	R/W	1
	Reg_P0_EnIPLockChk	0	1: Enable Check IPLL_LOCK when CLKD5 FIFO auto-reset is enabled.	R/W	1
2B		7		R/W	0
		6:5		R/W	00
	Reg_P0_EnCtrlCrt	4	1: enable 1-bit auto-correction of certain control code errors.	R/W	0
	Reg_P0_EnTERC4Crt	3	1: enable 1-bit auto-correction of certain TERC4 code errors.	R/W	0
	Reg_P0_filtalign	2	0: Channel skew edge changes once if any DE position change observed.	R/W	0

			1: Channel skew edge changeds only if 2 identical DE position change observed.		
	Reg_P0_deskewdown	1	0: the signal deskew_done is always asserted after DE observed unless reset. 1: the signal deskew_done is deasserted if symbol lock is de-asserted.	R/W	0
	Reg_P0_FixTek3D	0	0: Rx FSM data island trailing guard-band always ends after 2T. 1: Rx FSM data island trailing guard-band ends only if blank starts.	R/W	0
2C	Reserved	7:6			
	Reg_P0_DEDisp0	5		R/W	0
	Reg_P0_EnLockDisp	4	1: enable disparity-lock when doing video code comparison	R/W	0
	Reg_P0_ENVdoComp	3	1: enable video code-err comparison	R/W	0
	Reg_P0_FiltDE	2	1: deglitch 1T blank period 0: no deglitch	R/W	0
	Reg_P0_Terc_Check	1	1: enable TERC check	R/W	1
	Reg_P0_TimeOut_En	0	1: Enabled so main state go to lost after 4096T not seeing DE;	R/W	1
2D	Reg_P0_I2CFiltTap	7	DDC I2C filter tap	R/W	0
	Reg_P0_I2CFiltType	6	DDC I2C filter type	R/W	0
	Reg_P0_I2CDeglitch	5	DDC I2C deglitch	R/W	1
	Reg_P0_FastHDCPMode	4	HDCP Bcap's FAST bit (Bcaps[4]) setting	R/W	0
	Reg_P0_HDCP_A0Pin	3	1: Select 0x76 as DDC address. (default is 0x74)	R/W	0
	Reg_P0_HDCP_En	2	1: Enable HDCP	R/W	1
	Reg_P0_HDMIModeOVWT	1	1: Enable HDMI/DVI mode over-write	R/W	0
	Reg_P0_HDMIMode	0	1: HDMI/DVI mode value when reg2BH(1)=1	R/W	0
2E	Reg_P0_RdROM_Offset	7:0	Offset when reading HDCP key ROM	R/W	0x00
2F	Reserved	7			
	Reg_P0_MasterSel	6	1: PC ; 0: HDCP	R/W	0
	Reg_P0_RdROM_Header	5	Read rom header selector 1: E2 ; 0: E0	R/W	0
	Reg_P0_RdROM_ReqByte	4:0	Read rom request length	R/W	00000
30	Reserved	7:6			
	Reg_P0_EnHDCPOff	5	1: enable HDCP OFF function, if continuous 16 fields not receive enable descryption, then auth_state change to un-auth.	R/W	0
	Reg_P0_En_PwrOn_RdBKSV	4	1: Enable reading BKSV on power-on	R/W	1
	Reg_P0_SelAVMute	3	1: EESS_avmute will always mute	R/W	0
	Reg_P0_ROMBIST	2	1: enable ROMBIST	R/W	0
	Reg_P0_HDCP_StableCnt	1:0	Will influence the interrupt auth_done. If not"00", auth_done only raised when some vsyncs pass without reauth seen.	R/W	00
31	Reg_P0_HDCPCtrl 7: Enable repeater 6: KSV ready 5: Enable feature 1.1 4: Enable Fast authentication	7:4	Enable repeater function Set KSV ready when IT6536 is repeater Enable HDCP 1.1 feature Enable Fast authentication	R/W	0011
	Reg_P0_BCap7B	3	HDCP BCap bit 7 value	R/W	1
	Reg_P0_UpdRiSel	2	1: Ri value always update 0: Ri value update only when deskew done	R/W	0
	Reg_P0_HoldCntNum	1:0	SCL hold time counter value	R/W	01
32	Reserved	7			
	Reg_P0_DisBCH	6	1: disable BCH correction	R/W	0
	Reg_P0_Swap_RB	5	1: swap input channel 0 and channel 2	R/W	0
	Reg_P0_Swap_Pol	4	1: swap input 10bit word's polarity	R/W	0
	Reg_P0_PCI2CHoldT	3:0	PC interface I2C hold time setting	R/W	0010
33	Reserved	7:5			
	Reg_P0_EnH2VAutoRst	4	1: enable H2VFIFO auto reset	R/W	1
	Reg_P0_H2VFIFORst	3	1: H2VFIFO reset	R/W	0
	Reg_P0_EnH2VCheck	2	1: enable H2V blank check	R/W	1
	Reg_P0_ModeSel	1	H2V data mode select when reg31h(0)=1 1: MHL mode ; 0: HDMI mode	R/W	0
	Reg_P0_ForceMode	0	1: Force H2V data mode	R/W	0
34	Reg_P0_MHLPortAdr	7:1	I2C Slave Addresss for MHL block	R/W	1100000
	Reg_P0_MHLPortAdrEn	0	1: enable PC I2C access MHL block	R/W	0

35	Reserved	7:5			
	Reg_P0_EnClkDiffMin	4	1: the minimum delta value will be 2	R/W	0
	Reg_P0_RCLKDeltaSel	3:2	Watchdog PCLK Delta value select 00: 1%; 01: 2%; 10: 3%; 11:5%	R/W	00
	Reg_P0_UseIPLOCK	1	1: Watchdog will monitor IPLL Lock signal	R/W	1
	Reg_P0_EnUpdAvg	0	1: Watchdog will use average value for PCLK sample	R/W	1
36	Reserved	7:6			
	Reg_P0_WCLKHighNum	5:0	PxCK_4DOG high speed threshold	R/W	011001
37	Reg_P0_WCLKValidNum	7:0	PxCK_4DOG valid threshold	R/W	0x80

Back End Common Control (For Output)

BackEnd Common control					
50	RegEnPortChgRst	7		R/W	1
	RegEnAWCLKDly	6	1: Enable ARAMWCLK delay 1ns	R/W	0
	RegPCLKBInv	5	1: Invert internal PIXCLKB	R/W	1
	RegDCLKInv	4	1: Invert output DCLK	R/W	1
	RegPCLKBDly	3:2	Fine tune internal PIXCLKB clock delay (1ns for 1 step)	R/W	00
	RegDCLKDly	1:0	Fine tune output DCLK delay (1ns for 1 step)	R/W	00
51	RegPWDCSC	7	1: power down color space conversion logic	R/W	0
	RegHalfPCLKC	6	1: output PCLKO will be half frequency.	R/W	0
	Reg_OutDDR	5	1: Enable data output at rising and falling edge of output clock (DDR mode)	R/W	0
	Reg_Half_CLK	4	1: Output half pixel clock	R/W	0
	RegDisPixRpt	3	1: disable pixel repeat	R/W	0
	Reg2x656CLK	2	1: output is CCIR656 mode	R/W	0
	RegEn_Debug	1	1: enable debug output to IO	R/W	0
	RegMainPortSel	0	Main Port selector 0: Port 0 ; 1: Port 1	R/W	0
52	RegHCLKSel	7	HCLK source select when reg46h(6)=1	R/W	0
	RegEnSWHCLKSel	6	1: enable force HCLK source select	R/W	0
	RegDisVAutoMute	5	1: disable video auto mute	R/W	1
	RegTriSPDIF	4	1: Tri-state SPDIF IO	R/W	0
	RegTriI2SIO	3:0	Tristate Audio I2S0-I2S3 output buffer 1: Tri-state I2S[X] IO	R/W	0000
65	Reg_BTA1004Fmt	7	1: output BTA1004 format	R/W	0
	Reg_SyncEmb	6	1: output embeded sync	R/W	0
	Reg_OutColMod	5:4	Output color space 00: RGB444 , 01: YUV422 , 10: YUV444	R/W	00
	Reg_OutBit	3:2	Output color depth 00: 8bits, 01: 10bits, 10: 12bits	R/W	00
	Reg_CSCSel	1:0	00: bypass CSC 01: RGB to YUV 11: YUV to RGB	R/W	00

Color Space	Video Format	Bus Width	H/Vsync	Clocking	Setting
RGB	4:4:4	24/30/36	Seperate	1X	Reg51 = 0x00 Reg65[7:4] = '0000'
		12/15/18	Seperate	Dual-edged	Reg51 = 0x20 Reg65[7:4] = '0000'
		24/30/36	Seperate	0.5X, Dual-edged	Reg51 = 0x40 Reg65[7:4] = '0000'
YCbCr	4:4:4	24/30/36	Seperate	1X	Reg51 = 0x00 Reg65[7:4] = '0010'
		12/15/18	Seperate	Dual-edged	Reg51 = 0x20 Reg65[7:4] = '0010'
		24/30/36	Seperate	0.5X, Dual-edged	Reg51 = 0x40 Reg65[7:4] = '0010'
	4:2:2	16/20/24	Seperate	1X	Reg51 = 0x00 Reg65[7:4] = '0001'
			Seperate	0.5X, Dual-edged	Reg51 = 0x40 Reg65[7:4] = '0001'
			Embedded	1X	Reg51 = 0x00 Reg65[7:4] = '0101'
			Embedded	0.5X, Dual-edged	Reg51 = 0x40 Reg65[7:4] = '0101'
		8/10/12	Seperate	2X	Reg51 = 0x44 Reg65[7:4] = '0001'
			Seperate	1X, Dual-edged	Reg51 = 0x44 Reg65[7:4] = '0001'
			Embedded	2X	Reg51 = 0x44 Reg65[7:4] = '0101'
			Embedded	1X, Dual-edged	Reg51 = 0x44

					Reg65[7:4] = '0101'
		BTA1004	Embedded	1X	Reg51 = 0x00 Reg65[7:4] = '1101'
			Embedded	0.5X, Dual-edged	Reg51 = 0x40 Reg65[7:4] = '1101'

Before enable video output (turning tri-state off), should reset *Reg_656FFRst* (Reg64[7] = '1' → '0'), then turn on the video output.

53	RegVDGatting	7	Enable output data gating to zero when no Video display	R/W	0
	RegVIOSel	6	1: video IO enable depent on VIOenable 0: video IO eanble depent on VDIO1enable	R/W	0
	RegVDIOLLdisable	5	1: disable video IO QE0, QE1, QE12, QE13, QE24, QE25	R/W	0
	RegVDIOLHdisable	4	1: disable video IO QE2, QE3, QE14, QE15, QE26, QE27	R/W	0
	RegTriVDIO	3:1	1: enable tri-state Video IO	R/W	0
	RegTriVIO	0	1: Tristate video control signal IO	R/W	0
54	RegEnAsynRst	7	1: Enable Asynchronous reset for OCLK	R/W	0
	RegMCLKSel	6:4	MCLK output clock multiple number 000: 128FS ; 001: 256FS ; 010: 384FS 011: 512FS ; 100: 640FS ; 101: 768FS 110: 894FS ; 111: 1024FS	R/W	001
	Reserved	3:2			
	RegRCLKFreqSel	1:0	RCLK frequency select 00: RINGCLK/2 ; 01: RINGCLK/4 10: RINGCLK/8 ; 11: RINGCLK/16	R/W	00
55	Reserved	7:3			
	RegVidOutDly	2:0	When set, output video data will dealy 1ns. RegVidOutDly[0] : QE[11:0] RegVidOutDly[1] : QE[23:12] RegVidOutDly[2] : QE[35:24]	R/W	000
58	Reg_VIO_Slew	7	Separate driving strength on Video clock and data Slew rate: 0:Fast, 1:Slow Driving strength: When 1.8V: 00: 1.25mA, 01: 2.5mA, 10: 3.75mA, 11: 5mA When 3.3V: 00: 2.5mA, 01: 5mA, 10: 7.5mA, 11: 10mA	R/W	1
	Reserved	6			
	Reg_VIO_ST	5:4		R/W	00
	Reg_VCLK_Slew	3		R/W	1
	Reserved	2			
	Reg_VCLK_ST	1:0		R/W	01
59	Reg_AIO_Slew	7	Separate driving strength on Audio clock and data Slew rate: 0:Fast ; 1:Slow Driving strength: When 1.8V: 00: 1.25mA, 01: 2.5mA, 10: 3.75mA, 11: 5mA When 3.3V: 00: 2.5mA, 01: 5mA, 10: 7.5mA, 11: 10mA	R/W	1
	Reserved	6			
	Reg_AIO_ST	5:4		R/W	00
	Reg_MCLK_Slew	3		R/W	1
	Reserved	2			
	Reg_MCLK_ST	1:0		R/W	01
5A	Reg_PCSDA_Slew	7	Slew rate of command I2C pins 0: Fast ; 1: Slow	R/W	1
	Reserved	6			
	Reg_PCSDA_ST	5:4	Current strength of command I2C pins 00: 2.5mA, 01: 5mA, 10: 7.5mA, 11: 10mA	R/W	10
	Reg_DDCSDA_Slew	3	Slew rate of HDCP I2C pins 0: Fast ; 1: Slow	R/W	1
	Reserved	2			
	Reg_DDCSDA_ST	1:0	Current strength of HDCP I2C pins 00: 2.5mA, 01: 5mA, 10: 7.5mA, 11: 10mA	R/W	10
5B	Reg_CDSENSE_SMT	7	CDSENSE IO schmitt-trigger setting	R/W	1
	RegPS_CntlValue	6	ENVBUS output value when reg5Bh[5:4]=10	R/W	0
	RegPS_CntlMode	5:4	00: ENVBUS IO will output inversed renvbus 01: ENVBUS IO will output renvbus 10: ENVBUS IO will output RegPS_CntlValue 11: ENVBUS IO will output inversed renvbus	R/W	00
	Reg_MISC_Slew	3	MISC IO Slew Rate setting	R/W	1
	Reserved	2			
	Reg_MISC_ST	1:0	MISC IO Strength setting	R/W	01
5D	RegIntMask[7:0]	7:0	Interrupt mask for Reg0x05h	R/W	0xFF
5E	RegIntMask[15:8]	7:0	Interrupt mask for Reg0x06h	R/W	0xFF
5F	RegIntMask[23:16]	7:0	Interrupt mask for Reg0x07h	R/W	0xFF
60	RegIntMask[31:24]	7:0	Interrupt mask for Reg0x08h	R/W	0xFF

61	RegIntMask[39:32]	7:0	Interrupt mask for Reg0x09h	R/W	0xFF
62	Reserved	7:2			
	RegIntMask[41:40]	1:0	Interrupt mask for Reg0xD0h	R/W	11
63	Reserved	7:6			
	RegEnIntOut	5	1: Enable Interrupt IO output	R/W	0
	RegEnCBusInt	4	1: Enable MHL CBus Interrupt	R/W	1
	RegEnSetInt	3	1: Enable MHL Set Interrupt	R/W	1
	RegEnHDMIInt	2	1: Enable HDMI interrupt	R/W	1
	RegIntrOutType	1	Interupt pin output type 1: open drain 0: push pull	R/W	1
	RegIntPol	0	Interrupt pin output polarity 1: low active 0: high active	R/W	1
64	Reg_656FFRst	7	1: reset video FIFO's pointer	R/W	0
	Reg_EnAVMuteRst	6	1: enable reset video FIFO when detect avmute	R/W	0
	Reg_ChgSyncPol	5	1: Output Sync's polarity setting by reg54h[7:6]	R/W	0
	Reg_ChSwap	4	1: swap output channel0 and channel2 when output mode is yuv422	R/W	0
	Reg_RBSwap	3	1: swap output channel0 and channel2 when output mode is yuv444 or rgb444 swap Cb and Cr when yuv422	R/W	0
	Reg_LMSwap	2	MSB/LSB swap	R/W	0
	Reg_VSyncPol	1	VSync output polarity	R/W	0
	Reg_HSyncPol	0	HSync output polarity	R/W	0
65	Reg_BTA1004Fmt	7	1: output BTA1004 format	R/W	0
	Reg_SyncEmb	6	1: output embeded sync	R/W	0
	Reg_OutColMod	5:4	Output color space 00: RGB444 , 01: YUV422 , 10: YUV444	R/W	00
	Reg_OutBit	3:2	Output color depth 00: 8bits, 01: 10bis, 10: 12bits	R/W	00
	Reg_CSCSel	1:0	00: bypass CSC 01: RGB to YUV 11: YUV to RGB	R/W	00
66	RegEn3DFreSeq	7	Re-generate DE when receive MHL frame sequential 3D 1: enable ; 0: disable	R/W	0
	RegEnHW3DFreSeq	6	Auto enable re-generate DE function when receive MHL frame sequential 3D VIC 1: enable ; 0: disable	R/W	1
	Reg_3DFldPol	5	field polarity in 3D mode	R/W	0
	Reg_DE3DFrame	4	1: 3D frame-packet mode to sequence mode	R/W	0
	RegEnSyncOut	3	1: enable HSync & VSync output	R/W	1
	Reg_YCSwap	2	1: channel YC Swapping	R/W	0
	RegSTBMode	1:0	Video stable condition selector 01: clock stable ; 10: H stable ; others: V stable	R/W	00
67	RegAutoCSCSel	7	1: Enable HW CSCSel	R/W	1
	Reg_CSCOffset_Signed	6		R/W	0
	Reg_CSCOffset_YSign	5		R/W	0
	Reg_CSCOffset_CRSign	4		R/W	0
	Reg_CSCOffset_CBSign	3		R/W	0
	Reg_DNFreeGo	2	1: Enable Dither's Fcnt function	R/W	0
	Reg_EnDither	1	1: Enable Dither function	R/W	0
	Reg_EnUdFilt	0	1: Enable Color Up/Dn Filter	R/W	0
68	Reg_CBOffset	7:0		R/W	0x00
69	Reg_PktRec_Type_H	7:0	Decide which kind of packet to be recorded on General PKT registers	R/W	0x0A
6A	Reg_PktRec_Type	7:0	Decide which kind of packet to be fully recorded on General PKT register	R/W	0x83
6B	Reg_ACP_Rec_Type	7:0	The packet type will be recoded to ACP register	R/W	0x04
6C	Reg_ISRC1_Rec_Type	7:0	The packet type will be recoded to ISRC1 register	R/W	0x05
6D	Reg_ISRC2_Rec_Type	7:0	The packet type will be recoded to ISRC2 register	R/W	0x06
6E	Reg_PktSetClr	7:6	Packet set clear	R/W	00
	RegPktFlag_Ctrl 5: ACP 4: General 3: SPD 2: Audio 1: MPEG	5:0	0: interrupt only when first receiving or a new value is updated. 1: interrupt each time a packet is received.	R/W	000000

	0: AVI				
6F	Reserved	7:6			
	Reg_GenPkt_HL	5	GenPkt register latch data selector	R/W	0
	Reg_ISRC2_HL	4	ISRC2 registers latch data selector	R/W	0
	Reg_NewPkt_Sel 3: ISRC2 2: ISRC1 1: ACP 0: General Packet	3:0	1: latch unsupport packet data 0: latch normal data	R/W	0000
70	CLR_FramePkt_Err	7	Clear the error register asserted by packets that is received not in a manner directed by spec	R/W	0
	Reg_ForceLayout	6	1: force layout value	R/W	0
	Reg_LayoutNum	5	Layout value setting when Reg_ForceLayout=1	R/W	0
	Reg_ForceCH	4	1: force channel number	R/W	0
	Reg_CHNum	3:0	Channel number setting when Reg_ForceCh=1	R/W	0000
71	Reserved	7:4			
	RegEnPPColMode	3	1: Input color mode YUV422 when PP mode	R/W	1
	Reg_ForceColMod	2	0: Input color mode auto detect 1: Force input color mode as bit[3:2] setting	R/W	0
	Reg_ColMod_Set	1:0	Input color mode set: 00: RGB mode ; 01: YUV422 mode 10: YUV444 mode	R/W	00
72	RegDebugSel	7:0	Debug port select	R/W	00000000
73	Reserved	7:3			
	RegEnFixKey	3	1: hdcp key from internal 0: hdcp key from SIPROM	R/W	0
	RegEnSiPROM	2	1: sip relative registers write enable	R/W	0
	Reg_SiPROMSel	1	0: default block (block 0) 1: backup block (block 1)	R/W	0
	Reg_SiPRASel	0	SiPROM read address selection 0: from HDCP module 1: from Reg_SiPA[9:0] or ExtSiP_A[9:0]	R/W	0

Audio Control Registers

Audio Control					
74	Reg_I2SCEn	7	1: enable compressed but non-HBR audio output from I2S path	R/W	0
	RegForce_FS	6	Force Audio FS mode	R/W	0
	RegDis_False_DE	5	Disable false DE output	R/W	1
	RegAud_Info_Force	4	Force Audio setting from Aud info frame	R/W	0
	RegAVMute_Value	3	AVMute value when software AVMute is enable	R/W	0
	RegForce_AVMute	2	Software forced-AVMute mode	R/W	0
	RegDien	1	1: enable sdm dither	R/W	0
	RegDis_sdm	0	1: disable sdm	R/W	0
75	RegWS_Sel	7	1: invert channel A and channel B select	R/W	0
	RegI2S_Width	6:2	I2S word length, only effective in right justified mode; Maximum 24 bits	R/W	11000
	RegI2S_Mode	1:0	I2S output mode 00: I2S mode ; 01: right justified mode 10: left justified mode ; 11: undefined	R/W	00
76	RegI2S_CH3Sel	7:6	I2S channel 6 and channel 7 map: 00: map to channel 0 and channel 1 01: map to channel 2 and channel 3 10: map to channel 4 and channel 5 11: map to channel 6 and channel 7	R/W	11
	RegI2S_Ch2Sel	5:4	I2S channel 4 and channel 5 map: 00: map to channel 0 and channel 1 01: map to channel 2 and channel 3 10: map to channel 4 and channel 5 11: map to channel 6 and channel 7	R/W	10
	RegI2S_Ch1Sel	3:2	I2S channel 2 and channel 3 map: 00: map to channel 0 and channel 1 01: map to channel 2 and channel 3 10: map to channel 4 and channel 5 11: map to channel 6 and channel 7	R/W	01
	RegI2S_Ch0Sel	1:0	I2S channel 0 and channel 1 map: 00: map to channel 0 and channel 1 01: map to channel 2 and channel 3 10: map to channel 4 and channel 5 11: map to channel 6 and channel 7	R/W	00
77	RegAudIO_OutSel	7:4	[3]: MUTE IO pin will output MCLKO [2]: SCK IO pin will output MCLKO [1]: I2S1 IO pin will output 3DR [0]: WS IO pin will output SPDIF	R/W	0000
	RegAudMode	3:2	Audio lock method select	R/W	00
	RegForce_CTS	1	Software force to set CTS value	R/W	0
	RegForce_CTSMode	0	Use CTS for audio FIFO adjustment	R/W	0
78	RegN_Set[7:0]	7:0	N [7:0] when ForceCTS	R/W	0x00
79	RegN_Set[15:8]	7:0	N[15:8] when ForceCTS	R/W	0x18
7A	RegBFrameSwap	7	1: enable audio B Frame Swap Interupt	R/W	1
	RegAud_cinc	6	1: decrease gain of integral path in digital path	R/W	1
	RegAud_cts_res	5:4	Decrease gain of propotional path in digital path	R/W	01
	RegN_Set[19:16]	3:0	N[19:16] when ForceCTS	R/W	0000
7B	Reserved	7:4			
	RegFS_Set	3:0	Software set sampling frequency 0000: 44.1KHz ; 0010: 48KHz 0011: 32KHz ; 1000: 88.2KHz 1010: 96KHz ; 1100: 176.4KHz ; 1110: 192KHz	R/W	0010
7C	RegHWMuteRate[7:0]	7:0	Hardware mute rate value [7:0]	R/W	0x20
7D	RegARAM_BIST_EN	7	1: enable Audio RAM BIST function	R/W	0
	RegHWForceMute	6	0: mute control by channel status 1: mute anyway	R/W	0
	RegHWAudMuteClrMode	5	FIFO mute clear	R/W	0
	RegHWMuteClr	4	Clear H/W mute	R/W	0
	RegHWMuteEn	3	H/W Mute enable	R/W	1
	RegHWMuteRate[10:8]	2:0	Hardware mute rate value [10:8]	R/W	000
7E	Reg_BiPhaseMode	7	1: enable SPDIF bi-phase mode	R/W	0
	Reg_HBRSel	6	1: HBR audio output to SPDIF 0: HBR audio output to I2S	R/W	0
	Reg_I2SOut_Fmt	5	1: output DSD audio when force I2Sout	R/W	0

			0: output others audio when force I2Sout		
	Reg_Force_I2SOut	4	1: Force I2S output format	R/W	0
	Reg_WAddWatch	3:2	Audio FIFO debug option	R/W	00
	Reg_HWAmpCtrl	1:0	Auido amplitude control 00: norma ; 01: 2X ; 10,11: 4X	R/W	00
Audio N/CTS read back					
2BE	N[19:12]	7:0	Audio N parameter decoder value [19:12]	RO	
2BF	N[11:4]	7:0	Audio N parameter decoder value [11:4]	RO	
2C0	CTS[3:0]	7:4	Audio CTS parameter decoder value [3:0]	RO	
	N[3:0]	3:0	Audio N parameter decoder value [3:0]	RO	
2C1	CTS[19:12]	7:0	Audio CTS parameter decoder value [19:12]	RO	
2C2	CTS[11:4]	7:0	Audio CTS parameter decoder value [11:4]	RO	

I²C control

I²C Control					
7F	Reserved	7:3			
	RegCmd_FiltTap	2	PC I2C filter tap	R/W	0
	RegCmd_FiltType	1	PC I2C filter type	R/W	0
	RegCmd_Deglitch	0	PC I2C deglitch	R/W	1
80	Reserved	7:5			
	Reg_En_MuteCD	4	1: enable CD_conv mute	R/W	0
	Reg_RstCD	3	1: Reset CD_conv module	R/W	0
	Reg_EnAutoRstCD	2	1: enable CD auto reset	R/W	0
	Reg_DisDefRst	1		R/W	0
	Reg_En_DefPhase	0	1: Enable GCP default_phase setting	R/W	1
81	Reserved	7			
	Reg_P1_KeepErr	6	1: keep error status and counter when clock change to not valid	R/W	0
	Reg_P0_KeepErr	5	1: keep error status and counter when clock change to not valid	R/W	0
	Reg_P1_HoldECCErr	4	1: receive correct pkt will not decrease eccerrcnt	R/W	0
	Reg_P0_HoldECCErr	3	1: receive correct pkt will not decrease eccerrcnt	R/W	0
	RegBCHThresh	2:0	Threshold to raise BCHError interrupt	R/W	100
82	Reg_PktType_Mask[7:0]	7:0	Received packet type mask[7:0]	R/W	0xFF
83	Reserved	7:4			
	Reg_PktType_Mask[11:8]	3:0	Received packet type mask[11:8]	R/W	1111
84	RegEnTimer	7	Enable timer	W1P	
	RegTimerCntSet	6:0	Timer period setting	R/W	0000000
85	Reserved	7:6			
	RegEn3DROut	5	1: enable output 3DR signal	R/W	0
	Reg3DRPol	4	1: Polarity for 3DR signal	R/W	0
	RegEnDEMon	3	1: Enable DE monitor	R/W	1
	RegEnSyncMon	2	1: Enable H/V Sync monitor	R/W	1
	RegAVMuteSel	1	1: gating avmute in video detect module	R/W	0
	RegFNumSel	0	Select video detect stable frame number 0: 2 1: 3	R/W	0
86	RegCECSlaveAdr	7:0	I2C Slave Address for CEC	R/W	0xC8
87	RegEDIDSlaveAdr	7:1	I2C Slave Address for EDID	R/W	1010100
	RegEnEDIDSlaveAdr	0	1: Enable access EDID block	R/W	0
Device internal Status ReadBack					
91	P0_TMDSCLKSpeed	7:0	TMDSCLK = RCLK*256/ TMDSCLKSpeed	RO	
92	P1_TMDSCLKSpeed	7:0	TMDSCLK = RCLK*256/ TMDSCLKSpeed	RO	
93	P0_HDCP_Auth_State	7:4	Show the HDCP authentication status	RO	
	P0_HDCP_AdvCipher	3	HDCP Ainfo's ENABLE_1.1_FEATURES bit	RO	
	P0_HDCP_EESS	2	1: HDCP operates in EESS mode	RO	
	P0_HDCP_KeyRd_Fail_Flag	1	1: Read key from OTP was failed	RO	
	P0_HDCP_On_Flag	0	1: Encrytion on going	RO	
94	P0_HDCP_Status 7: Pj ever read 6: V'H4 ever read 5: Ri ever read 4: R0 ever read 3: AKSV ever written 2: An ever written 1: BKSV ever read 0: HDCP port ever read	7:0	Bit[3:0] are cleared only by reset Bit[7:4] are cleared by re-authentication and reset	RO	
95	P1_HDCP_Auth_State	7:4	Show the HDCP authentication status	RO	
	P1_HDCP_AdvCipher	3	HDCP Ainfo's ENABLE_1.1_FEATURES bit	RO	
	P1_HDCP_EESS	2	1: HDCP operates in EESS mode	RO	
	P1_HDCP_KeyRd_Fail_Flag	1	1: Read key from OTP was failed	RO	
	P1_HDCP_On_Flag	0	1: Encrytion on going	RO	
96	P1_HDCP_Status 7: Pj ever read 6: V'H4 ever read 5: Ri ever read 4: R0 ever read 3: AKSV ever written 2: An ever written	7:0	Bit[3:0] are cleared only by reset Bit[7:4] are cleared by re-authentication and reset	RO	

	1: BKSV ever read 0: HDCP port ever read				
97	P1_OPLL_HS	7	Port 1 OPLL in High Speed	RO	
	P0_OPLL_HS	6	Port 0 OPLL in High Speed	RO	
	P1_HDCP_Ri_Rec	5	Indicate HDCP TX had readback Ri, when write will be clear to 0	W1C	
	P0_HDCP_Ri_Rec	4	Indicate HDCP TX had readback Ri, when write will be clear to 0	W1C	
	FramePkt_Err 3: GMP error 2: GCP error 1: Audio infoframe pkt error 0: AVI infoframe pkt error	3:0	Error Means it's ever transmitted but vanished in at least a certain period	RO	
98	RHDMIIntGroup[3:0]	7:4	Indicate Interrupt occur in which group	RO	
	RCECIntSts	3	CEC interrupt status	RO	
	RHDMIInt	2	HDMI interrupt status	RO	
	RCBusIntSts	1	MHL CBus interrupt status	RO	
	RSetIntSts	0	MHL Set interrupt status	RO	
99	GCP_CD_Active	7:4	Color depth decoder value 4: 24bits ; 5: 30bits ; 6: 36bits ; 7: 48bits	RO	
	PxVideoStable	3	Indicate if video signal is stable	RO	
	VidField	2	Video field number in interlaced mode	RO	
	VidInterlaceMode	1	Indicate video is in interlaced mode	RO	
	VidModeChg	0	Indicate if a video mode change occurs	RO	
9A	PIXCLKSpeed	7:0	PIXCLK = RCLK*255/ PIXCLKSpeed	RO	
9C	VidHorTotal[7:0]		The total pixel count of one line[7:0]	RO	
9D	Reserved	7:6			
	VidHorTotal[13:8]	5:0	The total pixel count of one line[13:8]	RO	
9E	VidHorActive[7:0]	7:0	The active pixel count of one line[7:0]	RO	
9F	Reserved	7:6			
	VidHorActive[13:8]	5:0	The active pixel count of one line[13:8]	RO	
A0	VidHSyncWidth[7:0]	7:0	The width of HSync [7:0]	RO	
A1	VidHorFrontPorch[11:8]	7:4	The width of HSync front porch [11:8]	RO	
	Reserved	3:1			
	VidHSyncWidth[8]	0	The width of HSync [8]	RO	
A2	VidHorFrontPorch[7:0]	7:0	The width of HSync front porch [7:0]	RO	
A3	VidVerTotal[7:0]	7:0	The total line count of a field [7:0]	RO	
A4	VidVerActive[11:8]	7:4	The active line count of a field [11:8]	RO	
	VidVerTotal[11:8]	3:0	The total line count of a field [11:8]	RO	
A5	VidVerActive[7:0]	7:0	The active line count of a field [7:0]	RO	
A6	Reserved	7:5			
	VidVSyncWidth	4:0	The width of VSync [4:0]	RO	
A7	Reserved	7:6			
	VidVerFrontPorch	5:0	The width of VSync front porch	RO	
A8	P1_VSync_In_Pol	7	Port 1 VSync input polarity	RO	
	P1_HSync_In_Pol	6	Port 1 HSync input polarity	RO	
	P1_HDCP_Dis_Flag	5	Port 1 HDCP disable Flag	RO	
	P1_AVMute	4	Port 1 is in AVMute state	RO	
	P0_VSync_In_Pol	3	Port 0 VSync input polarity	RO	
	P0_HSync_In_Pol	2	Port 0 HSync input polarity	RO	
	P0_HDCP_Dis_Flag	1	Port 0 HDCP disable Flag	RO	
	P0_AVMute	0	Port 0 is in AVMute state	RO	
A9	P1_RDecFail	7	Port 1 SIPROM decode failed	RO	
	P0_RDecFail	6	Port 0 SIPROM decode failed	RO	
	Reserved	5:4			
	Pix_Rep	3:0	Video input status 0000: no repetition ; 0001: pixel sent 2 times 0011: pixel sent 4 times	RO	
AA	Audio_ON	7	Audio is ON	RO	
	HBRAudio	6	Audio type is High Bit Rate	RO	
	DSDAudio	5	Audio type is DSD	RO	
	Audio_Layout	4	Audio layout is 1 or 0	RO	
	Audio_CH_Valid	3:0	Audio channels valid Flag	RO	
AB	Audio_CH_Status[7:0]	7:0	Audio Channel status decoder value[7:0]	RO	
AC	Audio_CH_Status[15:8]	7:0	Audio Channel status decoder value[15:8]	RO	
AD	Audio_CH_Status[23:16]	7:0	Audio Channel status decoder value[23:16]	RO	
AE	Audio_CH_Status[31:24]	7:0	Audio Channel status decoder value[31:24]	RO	

AF	Audio_CH_Status[39:32]	7:0	Audio Channel status decoder value[39:32]	RO	
B0	Pkt_Type_R[7:0]	7:0	Received packet type low byte Pkt_type is cleared each time it's read	RO	
B1	Reserved	7:4			
	Pkt_Type_R[11:8]	3:0	Received packet type high byte	RO	
B2	P0_Receive_Err	7:0	[7]: 2-bit BCH error is detected and packet is discarded. [6]: 1-bit BCH error is detected and packet is discarded. [5:4]: A decode error is detected on channel 2 [3:2]: A decode error is detected on channel 1 [1:0]: A decode error is detected on channel 0	W1C	
B3	P0_Video_Err	7:5	Video code error	W1C	
	P0_AFE_RegDbg	4:0	AFE dubug signal read back 4: phase lock 3: audio pll lock 2:0: SDET_Normal	RO	
B4	P0_Code_Err	7:0	Error counter of code error	W1C	
B5	P0_Pkt_Err	7:0	Packet data error counter	W1C	
B6	P0_ErrCrt	7:0	[7:6]: reserved [5:3]: TercErrCrt for CH2 to CH0 [2:0]: CtrErrCrt for CH2 to CH0	W1C	
B7	P1_Receive_Err	7:0	[7]: 2-bit BCH error is detected and packet is discarded. [6]: 1-bit BCH error is detected and packet is discarded. [5:4]: A decode error is detected on channel 2 [3:2]: A decode error is detected on channel 1 [1:0]: A decode error is detected on channel 0	W1C	
B8	P1_Video_Err	7:5	Video code error	W1C	
	P1_AFE_RegDbg	4:0	AFE dubug signal read back 4: phase lock 3: audio pll lock 2:0: SDET_Normal	RO	
B9	P1_Code_Err	7:0	Error counter of code error	W1C	
BA	P1_Pkt_Err	7:0	Packet data error counter	W1C	
BB	P1_CrtErr	7:0	[7:6]: reserved [5:3]: TercErrCrt for CH2 to CH0 [2:0]: CtrErrCrt for CH2 to CH0	W1C	

Internal EDID Control Registers

Internal EDID Register					
C0	Reserved	7			
	RegEnMultiSeg	6	1: Enable multiple segment	R/W	0
	RegSoftEDIDRst	5	1: EDID reset	R/W	0
	RegAutoPwdEDID	4	1: auto powerdown EDID	R/W	0
	RegEDIDAdrSel	3	1: EDID address A2 ; 0: EDID address A0	R/W	0
	RegEnDetDDC	2	1: Enable monitor DDC detect start	R/W	1
	Reg_P1DisableShadow	1	1: disable Port 1 Internal EDID	R/W	1
	Reg_P0DisableShadow	0	1: disable Port 0 Internal EDID	R/W	1
C1	Reg_VSDBAdr	7:0	VSDB Offset	R/W	n.a.
C2	Reg_P0_AB	7:0	Port 0 EDID's AB value	R/W	n.a.
C3	Reg_P0_CD	7:0	Port 0 EDID's CD value	R/W	n.a.
C4	Reg_P0_B0Sum	7:0	Port 0 EDID block 1's checksum value	R/W	n.a.
C5	Reg_P0_B1Sum	7:0	Port 0 EDID block2's checksum value	R/W	n.a.
C6	Reg_P1_AB	7:0	Port 1 EDID's AB value	R/W	n.a.
C7	Reg_P1_CD	7:0	Port 1 EDID's CD value	R/W	n.a.
C8	Reg_P1_B0Sum	7:0	Port 1 EDID block 1's checksum value	R/W	n.a.
C9	Reg_P1_B1Sum	7:0	Port 1 EDID block2's checksum value	R/W	n.a.
D0	P1_EQFailInt	7	Port 1 auto EQ Fail Interrupt	W1C	
	P1_EQDoneInt	6	Port 1 auto EQ Done Interrupt	W1C	
	P0_EQFailInt	5	Port 0 auto EQ Fail Interrupt	W1C	
	P0_EQDoneInt	4	Port 0 auto EQ Done Interrupt	W1C	
	P1_RxCLKChg_Det	3	Port 1 Rx Clock change detect Interrupt	W1C	
	P0_RxCLKChg_Det	2	Port 0 Rx Clock change detect Interrupt	W1C	
	P1_AutoEQUpd	1	Port 1 Auto EQ Update	W1C	
	P0_AutoEQUpd	0	Port 0 Auto EQ Update	W1C	
D1	P1_RDetDDCAct	7	1: Port 1 DDC active ; 0: Port 1 DDC Idle	RO	
	P0_RDetDDCAct	6	1: Port 0 DDC active ; 0: Port 0 DDC Idle	RO	
	RIntGroup	5:0	Interrupt group reg05h, reg09h, regD0h	RO	
D2	Reserved	7:1			
	VidAbnormalSts	0	Video Abnormal Interrupt	W1C	

HDCP Value

HDCP related register					
110	P0_BSTATUS[7:0]	7:0	Port 0 HDCP BStatus[7:0]	R/W	0x00
111	Reserved	7:4			
	P0_BSTATUS[11:8]	3:0	Port 0 HDCP BStatus[11:8]	R/W	0000
112	P1_BSTATUS[7:0]	7:0	Port 1 HDCP BStatus[7:0]	R/W	0x00
113	Reserved	7:4			
	P1_BSTATUS[11:8]	3:0	Port 1 HDCP BStatus[11:8]	R/W	0000
114	SHA1_H0[7:0]	7:0	HDCP SHA1_H0[7:0]	R.W	n.a.
115	SHA1_H0[15:8]	7:0	HDCP SHA1_H0[15:8]	R.W	n.a.
116	SHA1_H0[23:16]	7:0	HDCP SHA1_H0[23:16]	R.W	n.a.
117	SHA1_H0[31:24]	7:0	HDCP SHA1_H0[31:24]	R.W	n.a.
118	SHA1_H1[7:0]	7:0	HDCP SHA1_H1[7:0]	R.W	n.a.
119	SHA1_H1[15:8]	7:0	HDCP SHA1_H1[15:8]	R.W	n.a.
11A	SHA1_H1[23:16]	7:0	HDCP SHA1_H1[23:16]	R.W	n.a.
11B	SHA1_H1[31:24]	7:0	HDCP SHA1_H1[31:24]	R.W	n.a.
11C	SHA1_H2[7:0]	7:0	HDCP SHA1_H2[7:0]	R.W	n.a.
11D	SHA1_H2[15:8]	7:0	HDCP SHA1_H2[15:8]	R.W	n.a.
11E	SHA1_H2[23:16]	7:0	HDCP SHA1_H2[23:16]	R.W	n.a.
11F	SHA1_H2[31:24]	7:0	HDCP SHA1_H2[31:24]	R.W	n.a.
120	SHA1_H3[7:0]	7:0	HDCP SHA1_H3[7:0]	R.W	n.a.
121	SHA1_H3[15:8]	7:0	HDCP SHA1_H3[15:8]	R.W	n.a.
122	SHA1_H3[23:16]	7:0	HDCP SHA1_H3[23:16]	R.W	n.a.
123	SHA1_H3[31:24]	7:0	HDCP SHA1_H3[31:24]	R.W	n.a.
124	SHA1_H4[7:0]	7:0	HDCP SHA1_H4[7:0]	R.W	n.a.
125	SHA1_H4[15:8]	7:0	HDCP SHA1_H4[15:8]	R.W	n.a.
126	SHA1_H4[23:16]	7:0	HDCP SHA1_H4[23:16]	R.W	n.a.
127	SHA1_H4[31:24]	7:0	HDCP SHA1_H4[31:24]	R.W	n.a.
128	DS_KSV0[7:0]	7:0	HDCP KSVFIFO0[7:0]	R/W	n.a.
129	DS_KSV0[15:8]	7:0	HDCP KSVFIFO0[15:8]	R/W	n.a.
12A	DS_KSV0[23:16]	7:0	HDCP KSVFIFO0[23:16]	R/W	n.a.
12B	DS_KSV0[31:24]	7:0	HDCP KSVFIFO0[31:24]	R/W	n.a.
12C	DS_KSV0[39:32]	7:0	HDCP KSVFIFO0[39:32]	R/W	n.a.
12D	DS_KSV1[7:0]	7:0	HDCP KSVFIFO1[7:0]	R/W	n.a.
12E	DS_KSV1[15:8]	7:0	HDCP KSVFIFO1[15:8]	R/W	n.a.
12F	DS_KSV1[23:16]	7:0	HDCP KSVFIFO1[23:16]	R/W	n.a.
130	DS_KSV1[31:24]	7:0	HDCP KSVFIFO1[31:24]	R/W	n.a.
131	DS_KSV1[39:32]	7:0	HDCP KSVFIFO1[39:32]	R/W	n.a.
132	DS_KSV2[7:0]	7:0	HDCP KSVFIFO2[7:0]	R/W	n.a.
133	DS_KSV2[15:8]	7:0	HDCP KSVFIFO2[15:8]	R/W	n.a.
134	DS_KSV2[23:16]	7:0	HDCP KSVFIFO2[23:16]	R/W	n.a.
135	DS_KSV2[31:24]	7:0	HDCP KSVFIFO2[31:24]	R/W	n.a.
136	DS_KSV2[39:32]	7:0	HDCP KSVFIFO2[39:32]	R/W	n.a.
137	DS_KSV3[7:0]	7:0	HDCP KSVFIFO3[7:0]	R/W	n.a.
138	DS_KSV3[15:8]	7:0	HDCP KSVFIFO3[15:8]	R/W	n.a.
139	DS_KSV3[23:16]	7:0	HDCP KSVFIFO3[23:16]	R/W	n.a.
13A	DS_KSV3[31:24]	7:0	HDCP KSVFIFO3[31:24]	R/W	n.a.
13B	DS_KSV3[39:32]	7:0	HDCP KSVFIFO3[39:32]	R/W	n.a.
13C	DS_KSV4[7:0]	7:0	HDCP KSVFIFO4[7:0]	R/W	n.a.
13D	DS_KSV4[15:8]	7:0	HDCP KSVFIFO4[15:8]	R/W	n.a.
13E	DS_KSV4[23:16]	7:0	HDCP KSVFIFO4[23:16]	R/W	n.a.
13F	DS_KSV4[31:24]	7:0	HDCP KSVFIFO4[31:24]	R/W	n.a.
140	DS_KSV4[39:32]	7:0	HDCP KSVFIFO4[39:32]	R/W	n.a.
141	DS_KSV5[7:0]	7:0	HDCP KSVFIFO5[7:0]	R/W	n.a.
142	DS_KSV5[15:8]	7:0	HDCP KSVFIFO5[15:8]	R/W	n.a.
143	DS_KSV5[23:16]	7:0	HDCP KSVFIFO5[23:16]	R/W	n.a.
144	DS_KSV5[31:24]	7:0	HDCP KSVFIFO5[31:24]	R/W	n.a.
145	DS_KSV5[39:32]	7:0	HDCP KSVFIFO5[39:32]	R/W	n.a.
146	DS_KSV6[7:0]	7:0	HDCP KSVFIFO6[7:0]	R/W	n.a.
147	DS_KSV6[15:8]	7:0	HDCP KSVFIFO6[15:8]	R/W	n.a.
148	DS_KSV6[23:16]	7:0	HDCP KSVFIFO6[23:16]	R/W	n.a.
149	DS_KSV6[31:24]	7:0	HDCP KSVFIFO6[31:24]	R/W	n.a.
14A	DS_KSV6[39:32]	7:0	HDCP KSVFIFO6[39:32]	R/W	n.a.
14B	DS_KSV7[7:0]	7:0	HDCP KSVFIFO7[7:0]	R/W	n.a.
14C	DS_KSV7[15:8]	7:0	HDCP KSVFIFO7[15:8]	R/W	n.a.

14D	DS_KSV7[23:16]	7:0	HDCP KSVFIFO7[23:16]	R/W	n.a.
14E	DS_KSV7[31:24]	7:0	HDCP KSVFIFO7[31:24]	R/W	n.a.
14F	DS_KSV7[39:32]	7:0	HDCP KSVFIFO7[39:32]	R/W	n.a.

Color Space Convert

Before enable color space convert, Reg51[7] should be '0'.

51	**RegPWDCSC**	**7**	**1: power down color space conversion logic**	**R/W**	**0**
	RegHalfPCLKC	6	1: output PCLKO will be half frequency.	R/W	0
	Reg_OutDDR	5	1: Enable data output at rising and falling edge of output clock (DDR mode)	R/W	0
	Reg_Half_CLK	4	1: Output half pixel clock	R/W	0
	RegDisPixRpt	3	1: disable pixel repeat	R/W	0
	Reg2x656CLK	2	1: output is CCIR656 mode	R/W	0
	RegEn_Debug	1	1: enable debug output to IO	R/W	0
	RegMainPortSel	0	Main Port selector 0: Port 0 ; 1: Port 1	R/W	0

Input color mode is in AVI Infoframe DB1[6:5] or in Reg71[1:0].

If in MHL packed pixel mode, the input color will be YCbCr422.

71	Reserved	7:4			
	RegEnPPColMode	3	1: Input color mode YUV422 when PP mode	R/W	1
	Reg_ForceColMod	2	0: Input color mode auto detect 1: Force input color mode as bit[3:2] setting	R/W	0
	Reg_ColMod_Set	1:0	Input color mode set: 00: RGB mode ; 01: YUV422 mode 10: YUV444 mode	R/W	00

Output Color Space and Selection are in Reg65

65	Reg_BTA1004Fmt	7	1: output BTA1004 format	R/W	0
	Reg_SyncEmb	6	1: output embeded sync	R/W	0
	Reg_OutColMod	5:4	Output color space 00: RGB444 , 01: YUV422 , 10: YUV444	R/W	00
	Reg_OutBit	3:2	Output color depth 00: 8bits, 01: 10bis, 10: 12bits	R/W	00
	Reg_CSCSel	1:0	00: bypass CSC 10: RGB to YUV 11: YUV to RGB	R/W	00

Color space conversion					
170	Reg_YOffset	7:0	Y blank level	R/W	0x10
171	Reg_COffset	7:0	C blank level	R/W	0x80
172	Reg_REGOffset	7:0	R/G/B blank level	R/W	0x00
173	Reg_Matrix11V[7:0]	7:0	Color space conversion matrix	R/W	0xB2
174	Reserved	7:6			
	Reg_Matrix11V[13:8]	5:0	Color space conversion matrix	R/W	000100
175	Reg_Matrix12V[7:0]	7:0	Color space conversion matrix	R/W	0x64
176	Reserved	7:6			
	Reg_Matrix12V[13:8]	5:0	Color space conversion matrix	R/W	000010
177	Reg_Matrix13V[7:0]	7:0	Color space conversion matrix	R/W	0xE9
178	Reserved	7:6			
	Reg_Matrix13V[13:8]	5:0	Color space conversion matrix	R/W	000000
179	Reg_Matrix21V[7:0]	7:0	Color space conversion matrix	R/W	0x93
17A	Reserved	7:6			
	Reg_Matrix21V[13:8]	5:0	Color space conversion matrix	R/W	011100
17B	Reg_Matrix22V[7:0]	7:0	Color space conversion matrix	R/W	0x16

17C	Reserved	7:6			
	Reg_Matrix22V[13:8]	5:0	Color space conversion matrix	R/W	000100
17D	Reg_Matrix23V[7:0]	7:0	Color space conversion matrix	R/W	0x56
17E	Reserved	7:6			
	Reg_Matrix23V[13:8]	5:0	Color space conversion matrix	R/W	011111
17F	Reg_Matrix31V[7:0]	7:0	Color space conversion matrix	R/W	0x49
180	Reserved	7:6			
	Reg_Matrix31V[13:8]	5:0	Color space conversion matrix	R/W	011101
181	Reg_Matrix32V[7:0]	7:0	Color space conversion matrix	R/W	0x9F
182	Reserved	7:6			
	Reg_Matrix32V[13:8]	5:0	Color space conversion matrix	R/W	011110
183	Reg_Matrix33V[7:0]	7:0	Color space conversion matrix	R/W	0x16
184	Reserved	7:6			
	Reg_Matrix33V[13:8]	5:0	Color space conversion matrix	R/W	000100

Internal Pattern Generator					
188	Reg_PGVMD	7:6	Pattern generater vertical mode	R/W	00
	Reg_PGHMD	5:4	Pattern generater horizontal mode	R/W	00
	Reg_PGVRep2	3	Pattern generater vertical repeat	R/W	0
	Reg_PGHRep2	2	Pattern generater horizontal repeat	R/W	0
	Reg_PGFreeGo	1		R/W	0
	Reg_PGEn	0	Enable Pattern generater	R/W	0
189	Reserved	7:6			
	Reg_PGSelB	5:4	Pattern generater B channel outupt select	R/W	00
	Reg_PGSelG	3:2	Pattern generater G channel outupt select	R/W	00
	Reg_PGSelR	1:0	Pattern generater R channel outupt select	R/W	00
18A	Reg_PGColR	7:0	Pattern generater R colorvalue	R/W	0x00
18B	Reg_PGColG	7:0	Pattern generater G color value	R/W	0x00
18C	Reg_PGColB	7:0	Pattern generater B color value	R/W	0x00
18D	Reg_PGColBlank	7:0	Pattern generater C blank value	R/W	0x00
18E	Reg_PGColBlankY	7:0	Pattern generater Y blank value	R/W	0x00
18F	Reg_PGHActSt[7:0]	7:0	Pattern generater H active start [7:0]	R/W	0x89
190	Reg_PGHActEd[3:0]	7:4	Pattern generater H active end [3:0]	R/W	0x9
	Reg_PGHActSt[11:8]	3:0	Pattern generater H active start [11:8]	R/W	0x0
191	Reg_PGHActEd[11:4]	7:0	Pattern generater H active end [11:4]	R/W	0x35
192	Reg_PGVActSt[7:0]	7:0	Pattern generater V active start [7:0]	R/W	0x23
193	Reg_PGVActEd[3:0]	7:4	Pattern generater V active end [3:0]	R/W	0x3
	Reg_PGVActSt[11:8]	3:0	Pattern generater V active start [11:8]	R/W	0x0
194	Reg_PGVActEd[11:4]	7:0	Pattern generater V active end [11:4]	R/W	0x20
195	Reg_PGVActSt2nd[7:0]	7:0	Pattern generater V active start 2nd [7:0]	R/W	0xFF
196	Reg_PGVActEd2nd[3:0]	7:4	Pattern generater V active end 2nd [3:0]	R/W	0xF
	Reg_PGVActSt2nd[11:8]	3:0	Pattern generater V active start 2nd [11:8]	R/W	0x7
197	Reg_PGVActEd2nd[11:4]	7:0	Pattern generater V active end 2nd [11:4]	R/W	0x7F
198	Reg_PGHTotal[7:0]	7:0	Pattern generater H total [7:0]	R/W	0x59
199	Reg_PGHSyncSt[3:0]	7:4	Pattern generater H sync start [3:0]	R/W	0xF
	Reg_PGHTotal[11:8]	3:0	Pattern generater H total [11:8]	R/W	0x3
19A	Reg_PGHSyncSt[11:4]	7:0	Pattern generater H sync start [11:4]	R/W	0x00
19B	Reg_PGHSyncEd[7:0]	7:0	Pattern generater H sync end [7:0]	R/W	0x4D
19C	Reg_PGVTotal[3:0]	7:4	Pattern generater V total [3:0]	R/W	0xC
	Reserved	3:2			
	Reg_PGSyncEmb	1	Pattern generater sync embeded output	R/W	0
	Reg_PGHSyncEd[8]	0	Pattern generater H sync end [8]	R/W	0
19D	Reg_PGVTotal[11:4]	7:0	Pattern generater V total [11:4]	R/W	0x20
19E	Reg_PGVSyncSt[7:0]	7:0	Pattern generater V sync start [7:0]	R/W	0x0C
19F	Reg_PGVSyncEd[3:0]	7:4	Pattern generater V sync end [3:0]	R/W	0x5
	Reg_PGVSyncSt[11:8]	3:0	Pattern generater V sync start [11:8]	R/W	0x2
1A0	Reg_PGCHInc	7:0	Pattern generater H increase value	R/W	0x10
1A1	Reg_PGCVInc	7:0	Pattern generater V increase value	R/W	0x10
1A8	RegOtpCtrl	7:0	Selected encryption word	R/W	0x2A
1A9	RegOtpXor	7:0	Selected encryption word	R/W	0xA5

AFE Control

Port 0 AFE control					
1B0	Reserved	7			
	Reg_P0_ForceCBus	6	1: CBUS signals follow registers 0: CBUS signals follow HW	R/W	0
	Reg_P0_CBusEnR100K	5	1: Enable CBUS 100K ohm resistor in register mode	R/W	0
	Reg_P0_CBusEnR1K	4	1: Enable CBUS 1K ohm resistor in register mode	R/W	0
	Reg_P0_CBusOut	3	CBUS output in register mode	R/W	0
	Reg_P0_CBusOE	2	CBUS output enable in register mode	R/W	0
	Reg_P0_HPDOut	1	HPD output enable in register mode	R/W	0
	Reg_P0_HPDOE	0	HPD output enable in register mode	R/W	0
1B1	Reg_P0_OPLL_GAIN	7	1: increase VCO gain	R/W	1
	Reg_P0_OPLL_OVWT	6	Similar to IPLL_OVWT, for OPLL, just there is no gain bit in OPLL register	R/W	0
	Reg_P0_IPLL_OVWT	5	0: GAIN, EC1 and ER0 are decided by watchdog GAIN=0;EC1=1;ER0=1 when CLK<=100M GAIN=1;EC1=0;ER0=0 when CLK>100M 1: by software overwirte	R/W	0
	Reg_P0_OPLL_ER1	4	1: increase filter resistance	R/W	0
	Reg_P0_OPLL_DEI	3	1: decrease iprpll pump current	R/W	0
	Reg_P0_OPLL_ENI	2	1: increase pump current	R/W	0
	Reg_P0_OPLL_EC1	1	1: increase vco capacitance	R/W	0
	Reg_P0_OPLL_ER0	0	1: increase filter resistance	R/W	0
1B2	Reg_P0_IPLL_ENI1	7	1: increase iprpll charge pump current	R/W	0
	Reg_P0_IPLL_ENI0B	6	0: increase iprpll charge pump current	R/W	0
	Reg_P0_IPLL_ER1	5	1: increase filter resistance value	R/W	0
	Reg_P0_IPLL_ENVC	4	1: increase filter capacitance	R/W	0
	Reg_P0_IPLL_DEI	3	1: decrease iprpll pump current	R/W	0
	Reg_P0_IPLL_GAIN	2	1: increase VCO speed	R/W	1
	Reg_P0_IPLL_DEK	1	1: reduce KVCO	R/W	0
	Reg_P0_IPLL_ER0	0	1: increase filter resistance	R/W	0
1B3	Reg_P0_ANA_DBG	7	1: enable analog debug port	R/W	0
	Reg_P0_OPLL_Bypass	6	1: bypass OPLL, OPCLK is directly from REFCLK	R/W	0
	Reg_P0_VOSEL	5:4	Output voltage selection for debug 00: phase select output of channel 0 (B) 01: phase select output of channel 1 (G) 10: phase select output of channel 2 (R) 11: fixed voltage (DVDD12 when P0_pwdc_etc=L, DVSS when P1_pwdc_etc=L)	R/W	00
	Reg_P0_AFB	3:0	2bit duration feedback Reg_AFB[3]=1 is valid bit	R/W	0000
1B4	Reg_P0_VSEL	7:6	Reference voltage source selection 00: 1.0V, 01: 0.95V, 10: 0.9V, 11: 0.85V	R/W	10
	Reg_P0_OPLL_ENVC	5	1: increase filter capacitance	R/W	0
	Reg_P0_IPLL_ENPRED	4	1: enable div4 prescaler	R/W	0
	Reg_P0_IPLLENI	3	1: Increase current of AFE ck_amp	R/W	0
	Reg_P0_TERM_DIN	2:0	Resistor control for termination calibration	R/W	100
1B5	Reg_P0_CKAMPENI	7	1: Increase current of AFE ck_amp, phitp, ckfs.	R/W	0
	Reg_P0_CKITPENI	6	1: Increase AFE phitp current	R/W	0
	Reg_P0_CKFSENI	5	1: Increase AFE ckfs current	R/W	0
	Reg_P0_PHSELEN	4	1: enable new phase selector algorithm	R/W	1
	Reg_P0_2BCDR	3	1: the output buffer of EAR[7:0] and LAT[7:0] will be gatted to L in order to save power consumption	R/W	1
	Reg_P0_PSELMUX	2	0: select the algorithm which used in elder version in cat6023 etc 1: select the new algorithm	R/W	1
	Reg_P0_PHERR_GAIN	1:0	Input register for the gain of phase change. The larger value means the large changed phase step	R/W	01
1B6	Reg_P0_SEL_PXCK	7		R/W	0
	Reg_P0_AFE_VCMSEL	6:5	Setting reference voltage of EQ 00: common-mode, 01: 1.0V,	R/W	00

			10: 0.95V, 11: 0.9V		
	Reg_P0_XTAL_PWDB	4	0: Power down Xtal oscillator	R/W	1
	Reg_P0_CSEL	3	1: increase filter resistance when pixel clock < 80MHz 0: when pixel clock > 80MHz	R/W	0
	Reg_P0_ENHYS	2:0	The input registers which to enable the differential pair mismatch of AMP_CLK_HDMI011 to avoid the malfunction caused by the noise. The larger value means the more clock amplifier differential pair mismatch. *MHL mode suggest to set '000'* *HDMI mode, suggest to set '011'*	R/W	011
1B7	Reg_P0_ENRB	7	0: NR option is enabled 1: NR option is disabled	R/W	0
	Reserved	6			
	Reg_P0_RING1	5	Ring oscillator option	R/W	0
	Reg_P0_RING0	4	Ring oscillator option	R/W	0
	Reg_P0_RINGSLOW	3	1: slower ring oscillator output clock 0: normal	R/W	0
	Reg_P0_RINGFAST	2	1: faster ring oscillator output clock 0: normal	R/W	0
	Reg_P0_PwdRGLR18BMode	1:0	00: when not in MHL mode, then Reg_18VPWD = '1'. Others: Reg_18VPWD = Reg_P0_PwdRGLR18BMode[0].	R/W	00
1B8	Reg_P0_HWENHYS	7	1: enable hw enhys setting 000 when mhlmode='1' else reg1B8h[2:0]	R/W	1
	Reg_P0_PWD_EQ	6	1: power down AFE EQ logic	R/W	0
	Reg_P0_AFEBackup	5:2	AFE backup register	R/W	0000
	P0_CKD5RST	1	1: a write '1' to this bit will align channel 0/1/2 CKD5 Clock signal.	R/W	0
	Reg_P0_ENCKD5RST	0	0: channel 0,1,2's CKD5 clock will not be aligned by CKD5RST signal 1: channel 0,1,2's CKD5 clock will be aligned by CKD5RST signal	R/W	0
1B9	Reg_P0_POL	7		R/W	0
	Reg_P0_S1CB	6	C value option of all channel	R/W	0
	Reserved	5:0			
1BA	Reserved	7:6			
	Reg_P0_HPDPD	5	HPD pull down signal	R/W	0
	Reg_P0_HPDSMT	4	1: enable HPD schmitt trigger	R/W	0
	Reg_P0_HPD_SLEW	3	HPD I/O slew rate control 0: fast 1: slow	R/W	1
	Reserved	2			
	Reg_P0_HPD_ST1	1	HPD I/O driving strength[1]	R/W	1
	Reg_P0_HPD_ST0	0	HPD I/O driving strength[0]	R/W	0
1BB	Reserved	7:6			
	Reg_P0_CBUSPD	5	CBUS pull down signal	R/W	0
	Reg_P0_CBUSSMT	4	1: enable CBUS schmitt trigger	R/W	0
	Reg_P0_CBUS_SLEW	3	CBUS I/O slew rate control 0: fast 1: slow	R/W	1
	Reserved	2			
	Reg_P0_CBUS_ST1	1	CBUS I/O driving strength[1]	R/W	1
	Reg_P0_CBUS_ST0	0	CBUS I/O driving strength[0]	R/W	0
1BC	Reg_DEQ	7:5	Reg_DEQ[0]=1 : EnDESI Reg_DEQ[1]=1 : EnDESC Reg_DEQ[2]=1 : EnLink2RS	R/W	111
	Reg_CKSEN	4		R/W	0
	Reg_SEL_DBG_PORT	3		R/W	0
	Reg_P0_APLL_ENI2A	2	Option for charge pump current with different EC1. 1: EC1=1; 0: EC1=0	R/W	1
	Reg_P0_APLL_EC1	1	The option for VCO gain	R/W	1
	Reg_P0_APLL_ENIA	0	Option for charge pump current.	R/W	0

			1: for 1.5I; 0: for I		
1BD	Reg_P0_B_FORCEPH	7	1: enable force channel 0 phase	R/W	0
	Reg_P0_B_PSEL	6:0	Channel 0 phase value	R/W	0000000
1BE	Reg_P0_G_FORCEPH	7	1: enable force channel 1 phase	R/W	0
	Reg_P0_G_PSEL	6:0	Channel 1 phase value	R/W	0000000
1BF	Reg_P0_R_FORCEPH	7	1: enable force channel 2 phase	R/W	0
	Reg_P0_R_PSEL	6:0	Channel 2 phase value	R/W	0000000
1C0	Reg_PWSB_LV	7		R/W	1
	Reg_CBUSR100K2	6		R/W	0
	Reg_CBUSR100K1	5		R/W	0
	Reg_CBUSR100K0	4		R/W	0
	Reg_CBUSR1K1	3		R/W	0
	Reg_CBUSR1K0	2		R/W	0
	Reg_V18V1	1		R/W	0
	Reg_V18V0	0		R/W	0

AFECTRL logic status readback

Port 0 / Port 1 AFECTRL logic status readback					
1D0	Reserved	7			
	P0_Rec_AMPTimeOut	6	Timeout	RO	
	P0_R_AMP2Valid	5	Calculation of Ch2 clock2 valid	RO	
	P0_R_AMP1Valid	4	Calculation of Ch2 clock1 valid	RO	
	P0_G_AMP2Valid	3	Calculation of Ch1 clock2 valid	RO	
	P0_G_AMP1Valid	2	Calculation of Ch1 clock1 valid	RO	
	P0_B_AMP2Valid	1	Calculation of Ch0 clock2 valid	RO	
	P0_B_AMP1Valid	0	Calculation of Ch0 clock1 valid	RO	
1D1	P0_Rec_MATCHCOUNT	7:0	Recorded number of match count	RO	
1D2	Reserved	7			
	P0_Rec_AMP16VAR	6:0	Recorded number of 16 Amp average value	RO	
1D3	Reserved	7			
	P0_Rec_AMPCOUNT	6:0	Recorded number of Amp value	RO	
1D4	Reserved	7:6			
	P0_Dbg_AUTOState	5:0	State of AutoEQ, for debug	RO	
1D5	P0_Rec_B_CS	7	AutoEQ calculated B_CS value	RO	
	P0_Rec_B_RS	6:0	AutoEQ calculated B_RS value	RO	
1D6	P0_Rec_G_CS	7	AutoEQ calculated G_CS value	RO	
	P0_Rec_G_RS	6:0	AutoEQ calculated G_RS value	RO	
1D7	P0_Rec_R_CS	7	AutoEQ calculated R_CS value	RO	
	P0_Rec_R_RS	6:0	AutoEQ calculated R_RS value	RO	
1D8	Reserved	7			
	P1_Rec_AMPTimeOut	6	Timeout	RO	
	P1_R_AMP2Valid	5	Calculation of Ch2 clock2 valid	RO	
	P1_R_AMP1Valid	4	Calculation of Ch2 clock1 valid	RO	
	P1_G_AMP2Valid	3	Calculation of Ch1 clock2 valid	RO	
	P1_G_AMP1Valid	2	Calculation of Ch1 clock1 valid	RO	
	P1_B_AMP2Valid	1	Calculation of Ch0 clock2 valid	RO	
	P1_B_AMP1Valid	0	Calculation of Ch0 clock1 valid	RO	
1D9	P1_Rec_MATCHCOUNT	7:0	Recorded number of match count	RO	
1DA	Reserved	7			
	P1_Rec_AMP16VAR	6:0	Recorded number of 16 Amp average value	RO	
1DB	Reserved	7			
	P1_Rec_AMPCOUNT	6:0	Recorded number of Amp value	RO	
1DC	Reserved	7:6			
	P1_Dbg_AUTOState	5:0	State of AutoEQ, for debug	RO	
1DD	P1_Rec_B_CS	7	AutoEQ calculated B_CS value	RO	
	P1_Rec_B_RS	6:0	AutoEQ calculated B_RS value	RO	
1DE	P1_Rec_G_CS	7	AutoEQ calculated G_CS value	RO	
	P1_Rec_G_RS	6:0	AutoEQ calculated G_RS value	RO	
1DF	P1_Rec_R_CS	7	AutoEQ calculated R_CS value	RO	
	P1_Rec_R_RS	6:0	AutoEQ calculated R_RS value	RO	
Audio RAM BIST Fault result					
1E0	ARAM_bo_FaultHQ	7	1: Audio RAM BIST fault	RO	
	ARAM_D6FaultStauHQ	6:0	1: Audio RAM BIST fault status	RO	
BackUp register					
1FE	Reg_Backup0	7:0	Backup register	R/W	0x00
1FF	Reg_Backup1	7:0	Backup register	R/W	0xFF

Infoframe

Info Frame recode					
210	SRC_Ver	7:0	SPD infoFrame Version	RO	
211	SRC_PB25	7:0	SPK infoFrame Data Byte 25	RO	
212	AVI_Length	7:0	AVI infoFrame Length	RO	
213	AVI_Version	7:0	AVI infoFrame Version	RO	
214	AVI_PB0	7:0	AVI infoFrame Data Byte 0	RO	
215	AVI_PB1	7:0	AVI infoFrame Data Byte 1	RO	
216	AVI_PB2	7:0	AVI infoFrame Data Byte 2	RO	
217	AVI_PB3	7:0	AVI infoFrame Data Byte 3	RO	
218	AVI_PB4	7:0	AVI infoFrame Data Byte 4	RO	
219	AVI_PB5	7:0	AVI infoFrame Data Byte 5	RO	
21A	AVI_PB6	7:0	AVI infoFrame Data Byte 6	RO	
21B	AVI_PB7	7:0	AVI infoFrame Data Byte 7	RO	
21C	AVI_PB8	7:0	AVI infoFrame Data Byte 8	RO	
21D	AVI_PB9	7:0	AVI infoFrame Data Byte 9	RO	
21E	AVI_PB10	7:0	AVI infoFrame Data Byte 10	RO	
21F	AVI_PB11	7:0	AVI infoFrame Data Byte 11	RO	
220	AVI_PB12	7:0	AVI infoFrame Data Byte 12	RO	
221	AVI_PB13	7:0	AVI infoFrame Data Byte 13	RO	
222	AVI_PB14	7:0	AVI infoFrame Data Byte 14	RO	
223	AVI_PB15	7:0	AVI infoFrame Data Byte 15	RO	
224	GenPkt_HB0	7:0	General Packet Header Byte 0	RO	
225	GenPkt_HB1	7:0	General Packet Header Byte 1	RO	
226	GenPkt_HB2	7:0	General Packet Header Byte 2	RO	
227	GenPkt_PB0	7:0	General Packet Data Byte 0	RO	
228	GenPkt_PB1	7:0	General Packet Data Byte 1	RO	
229	GenPkt_PB2	7:0	General Packet Data Byte 2	RO	
22A	GenPkt_PB3	7:0	General Packet Data Byte 3	RO	
22B	GenPkt_PB4	7:0	General Packet Data Byte 4	RO	
22C	GenPkt_PB5	7:0	General Packet Data Byte 5	RO	
22D	GenPkt_PB6	7:0	General Packet Data Byte 6	RO	
22E	GenPkt_PB7	7:0	General Packet Data Byte 7	RO	
22F	GenPkt_PB8	7:0	General Packet Data Byte 8	RO	
230	GenPkt_PB9	7:0	General Packet Data Byte 9	RO	
231	GenPkt_PB10	7:0	General Packet Data Byte 10	RO	
232	GenPkt_PB11	7:0	General Packet Data Byte 11	RO	
233	GenPkt_PB12	7:0	General Packet Data Byte 12	RO	
234	GenPkt_PB13	7:0	General Packet Data Byte 13	RO	
235	GenPkt_PB14	7:0	General Packet Data Byte 14	RO	
236	GenPkt_PB15	7:0	General Packet Data Byte 15	RO	
237	GenPkt_PB16	7:0	General Packet Data Byte 16	RO	
238	GenPkt_PB17	7:0	General Packet Data Byte 17	RO	
239	GenPkt_PB18	7:0	General Packet Data Byte 18	RO	
23A	GenPkt_PB19	7:0	General Packet Data Byte 19	RO	
23B	GenPkt_PB20	7:0	General Packet Data Byte 20	RO	
23C	GenPkt_PB21	7:0	General Packet Data Byte 21	RO	
23D	GenPkt_PB22	7:0	General Packet Data Byte 22	RO	
23E	GenPkt_PB23	7:0	General Packet Data Byte 23	RO	
23F	GenPkt_PB24	7:0	General Packet Data Byte 24	RO	
240	GenPkt_PB25	7:0	General Packet Data Byte 25	RO	
241	GenPkt_PB26	7:0	General Packet Data Byte 26	RO	
242	GenPkt_PB27	7:0	General Packet Data Byte 27	RO	
243	Audio_Version	7:0	Audio infoFrame Version	RO	
244	Audio_PB0	7:0	Audio infoFrame Data Byte 0	RO	
245	Audio_PB1	7:0	Audio infoFrame Data Byte 1	RO	
246	Audio_PB2	7:0	Audio infoFrame Data Byte 2	RO	
247	Audio_PB3	7:0	Audio infoFrame Data Byte 3	RO	
248	Audio_PB4	7:0	Audio infoFrame Data Byte 4	RO	
249	Audio_PB5	7:0	Audio infoFrame Data Byte 5	RO	
24A	Audio_Length	7:0	Audio infoFrame Length	RO	
24B	MPEG_Version	7:0	MPEG infoFrame Version	RO	
24C	MPEG_Length	7:0	MPEG infoFrame Length	RO	
24D	MPEG_PB0	7:0	MPEG infoFrame Data Byte 0	RO	
24E	MPEG_PB1	7:0	MPEG infoFrame Data Byte 1	RO	

24F	MPEG_PB2	7:0	MPEG infoFrame Data Byte 2	RO	
250	MPEG_PB3	7:0	MPEG infoFrame Data Byte 3	RO	
251	MPEG_PB4	7:0	MPEG infoFrame Data Byte 4	RO	
252	MPEG_PB5	7:0	MPEG infoFrame Data Byte 5	RO	
253	ACP_HB0	7:0	ACP packet Header Byte 0	RO	
254	ACP_Type	7:0	ACP packet Header Byte 1	RO	
255	ACP_HB2	7:0	ACP packet Header Byte 2	RO	
256	ACP_PB0	7:0	ACP packet Data Byte 0	RO	
257	ACP_PB1	7:0	ACP packet Data Byte 1	RO	
258	ACP_PB2	7:0	ACP packet Data Byte 2	RO	
259	ACP_PB3	7:0	ACP packet Data Byte 3	RO	
25A	ACP_PB4	7:0	ACP packet Data Byte 4	RO	
25B	ACP_PB5	7:0	ACP packet Data Byte 5	RO	
25C	ACP_PB6	7:0	ACP packet Data Byte 6	RO	
25D	ACP_PB7	7:0	ACP packet Data Byte 7	RO	
25E	ACP_PB8	7:0	ACP packet Data Byte 8	RO	
25F	ACP_PB9	7:0	ACP packet Data Byte 9	RO	
260	ACP_PB10	7:0	ACP packet Data Byte 10	RO	
261	ACP_PB11	7:0	ACP packet Data Byte 11	RO	
262	ACP_PB12	7:0	ACP packet Data Byte 12	RO	
263	ACP_PB13	7:0	ACP packet Data Byte 13	RO	
264	ACP_PB14	7:0	ACP packet Data Byte 14	RO	
265	ACP_PB15	7:0	ACP packet Data Byte 15	RO	
266	ACP_PB16	7:0	ACP packet Data Byte 16	RO	
267	ACP_PB17	7:0	ACP packet Data Byte 17	RO	
268	ACP_PB18	7:0	ACP packet Data Byte 18	RO	
269	ACP_PB19	7:0	ACP packet Data Byte 19	RO	
26A	ACP_PB20	7:0	ACP packet Data Byte 20	RO	
26B	ACP_PB21	7:0	ACP packet Data Byte 21	RO	
26C	ACP_PB22	7:0	ACP packet Data Byte 22	RO	
26D	ACP_PB23	7:0	ACP packet Data Byte 23	RO	
26E	ACP_PB24	7:0	ACP packet Data Byte 24	RO	
26F	ACP_PB25	7:0	ACP packet Data Byte 25	RO	
270	ACP_PB26	7:0	ACP packet Data Byte 26	RO	
271	ACP_PB27	7:0	ACP packet Data Byte 27	RO	
272	ISRC1_HB0	7:0	ISRC1 packet Header Byte 0	RO	
273	ISRC1_HB1	7:0	ISRC1 packet Header Byte 1	RO	
274	ISRC1_HB2	7:0	ISRC1 packet Header Byte 2	RO	
275	ISRC1_PB0	7:0	ISRC1 packet Data Byte 0	RO	
276	ISRC1_PB1	7:0	ISRC1 packet Data Byte 1	RO	
277	ISRC1_PB2	7:0	ISRC1 packet Data Byte 2	RO	
278	ISRC1_PB3	7:0	ISRC1 packet Data Byte 3	RO	
279	ISRC1_PB4	7:0	ISRC1 packet Data Byte 4	RO	
27A	ISRC1_PB5	7:0	ISRC1 packet Data Byte 5	RO	
27B	ISRC1_PB6	7:0	ISRC1 packet Data Byte 6	RO	
27C	ISRC1_PB7	7:0	ISRC1 packet Data Byte 7	RO	
27D	ISRC1_PB8	7:0	ISRC1 packet Data Byte 8	RO	
27E	ISRC1_PB9	7:0	ISRC1 packet Data Byte 9	RO	
27F	ISRC1_PB10	7:0	ISRC1 packet Data Byte 10	RO	
280	ISRC1_PB11	7:0	ISRC1 packet Data Byte 11	RO	
281	ISRC1_PB12	7:0	ISRC1 packet Data Byte 12	RO	
282	ISRC1_PB13	7:0	ISRC1 packet Data Byte 13	RO	
283	ISRC1_PB14	7:0	ISRC1 packet Data Byte 14	RO	
284	ISRC1_PB15	7:0	ISRC1 packet Data Byte 15	RO	
285	ISRC2_HB0	7:0	ISRC2 packet Header Byte 0	RO	
286	ISRC2_HB1	7:0	ISRC2 packet Header Byte 1	RO	
287	ISRC2_HB2	7:0	ISRC2 packet Header Byte 2	RO	
288	ISRC2_PB0	7:0	ISRC2 packet Data Byte 0	RO	
289	ISRC2_PB1	7:0	ISRC2 packet Data Byte 1	RO	
28A	ISRC2_PB2	7:0	ISRC2 packet Data Byte 2	RO	
28B	ISRC2_PB3	7:0	ISRC2 packet Data Byte 3	RO	
28C	ISRC2_PB4	7:0	ISRC2 packet Data Byte 4	RO	
28D	ISRC2_PB5	7:0	ISRC2 packet Data Byte 5	RO	
28E	ISRC2_PB6	7:0	ISRC2 packet Data Byte 6	RO	
28F	ISRC2_PB7	7:0	ISRC2 packet Data Byte 7	RO	
290	ISRC2_PB8	7:0	ISRC2 packet Data Byte 8	RO	
291	Vendor_Ver		Vendor Specific InfoFrame version	RO	

292	Vendor_Length		Vendor Specific InfoFrame length	RO	
293	Vendor_PB0		Vendor Specific InfoFrame Data Byte 0	RO	
294	Vendor_PB1		Vendor Specific InfoFrame Data Byte 1	RO	
295	Vendor_PB2		Vendor Specific InfoFrame Data Byte 2	RO	
296	Vendor_PB3		Vendor Specific InfoFrame Data Byte 3	RO	
297	Vendor_PB4		Vendor Specific InfoFrame Data Byte 4	RO	
298	Vendor_PB5		Vendor Specific InfoFrame Data Byte 5	RO	
299	Vendor_PB6		Vendor Specific InfoFrame Data Byte 6	RO	

HDCP AKSV/BKSV/Mi read back					
29A	P0_AkSV[7:0]	7:0	HDCP AKSV ReadBack [7:0]	RO	
29B	P0_AKSV[15:8]	7:0	HDCP AKSV ReadBack [15:8]	RO	
29C	P0_AKSV[23:16]	7:0	HDCP AKSV ReadBack [23:16]	RO	
29D	P0_AKSV[31:24]	7:0	HDCP AKSV ReadBack [31:24]	RO	
29E	P0_AKSV[39:32]	7:0	HDCP AKSV ReadBack [39:32]	RO	
29F	P0_BKSV[7:0]	7:0	HDCP BKSV value readback [7:0]	RO	
2A0	P0_BKSV[15:8]	7:0	HDCP BKSV value readback [15:8]	RO	
2A1	P0_BKSV[23:16]	7:0	HDCP BKSV value readback [23:16]	RO	
2A2	P0_BKSV[31:24]	7:0	HDCP BKSV value readback [31:24]	RO	
2A3	P0_BKSV[39:32]	7:0	HDCP BKSV value readback [39:32]	RO	
2A4	P0_M0[7:0]	7:0	HDCP Mi value readback [7:0]	RO	
2A5	P0_M0[15:8]	7:0	HDCP Mi value readback [15:8]	RO	
2A6	P0_M0[23:16]	7:0	HDCP Mi value readback [23:16]	RO	
2A7	P0_M0[31:24]	7:0	HDCP Mi value readback [31:24]	RO	
2A8	P0_M0[39:32]	7:0	HDCP Mi value readback [39:32]	RO	
2A9	P0_M0[47:40]	7:0	HDCP Mi value readback [47:40]	RO	
2AA	P0_M0[55:48]	7:0	HDCP Mi value readback [55:48]	RO	
2AB	P0_M0[63:56]	7:0	HDCP Mi value readback [63:56]	RO	
2AC	P1_AkSV[7:0]	7:0	HDCP AKSV ReadBack [7:0]	RO	
2AD	P1_AKSV[15:8]	7:0	HDCP AKSV ReadBack [15:8]	RO	
2AE	P1_AKSV[23:16]	7:0	HDCP AKSV ReadBack [23:16]	RO	
2AF	P1_AKSV[31:24]	7:0	HDCP AKSV ReadBack [31:24]	RO	
2B0	P1_AKSV[39:32]	7:0	HDCP AKSV ReadBack [39:32]	RO	
2B1	P1_BKSV[7:0]	7:0	HDCP BKSV value readback [7:0]	RO	
2B2	P1_BKSV[15:8]	7:0	HDCP BKSV value readback [15:8]	RO	
2B3	P1_BKSV[23:16]	7:0	HDCP BKSV value readback [23:16]	RO	
2B4	P1_BKSV[31:24]	7:0	HDCP BKSV value readback [31:24]	RO	
2B5	P1_BKSV[39:32]	7:0	HDCP BKSV value readback [39:32]	RO	
2B6	P1_M0[7:0]	7:0	HDCP Mi value readback [7:0]	RO	
2B7	P1_M0[15:8]	7:0	HDCP Mi value readback [15:8]	RO	
2B8	P1_M0[23:16]	7:0	HDCP Mi value readback [23:16]	RO	
2B9	P1_M0[31:24]	7:0	HDCP Mi value readback [31:24]	RO	
2BA	P1_M0[39:32]	7:0	HDCP Mi value readback [39:32]	RO	
2BB	P1_M0[47:40]	7:0	HDCP Mi value readback [47:40]	RO	
2BC	P1_M0[55:48]	7:0	HDCP Mi value readback [55:48]	RO	
2BD	P1_M0[63:56]	7:0	HDCP Mi value readback [63:56]	RO	
Audio N/CTS read back					
2BE	N[19:12]	7:0	Audio N parameter decoder value [19:12]	RO	
2BF	N[11:4]	7:0	Audio N parameter decoder value [11:4]	RO	
2C0	CTS[3:0]	7:4	Audio CTS parameter decoder value [3:0]	RO	
	N[3:0]	3:0	Audio N parameter decoder value [3:0]	RO	
2C1	CTS[19:12]	7:0	Audio CTS parameter decoder value [19:12]	RO	
2C2	CTS[11:4]	7:0	Audio CTS parameter decoder value [11:4]	RO	

MHL Control Registers of IT6801

MHL Registers Address are defined in HDMI register 0x34

34	Reg_P0_MHLPortAdr	7:1	I2C Slave Addresss for MHL block	R/W	1100000
	Reg_P0_MHLPortAdrEn	0	1: enable PC I2C access MHL block	R/W	0

W1C：Write 1 Clear
W1P：Write 1 generate pulse
RO：Read Only
R/W：Read and Write

MHL Registers in I2C slave address of IT6801 MHL

Reg	Name	Bit	Definition	Type	Default
00	RegEnCBusDbgMode	7	CBUS TX/RX queue debug mode 0: disable, 1: enable	R/W	0
	Reserved	6:4			
	RegEnCBusDbgCtrl[3:0]	3	1: Enable Reserved packet debug	R/W	0
		2	1: Enable MSC packet debug	R/W	0
		1	1: Enable Vendor-specific packet debug	R/W	0
		0	1: Enable DDC packet debug	R/W	0
01	RegEnCBusDeGlitch	7	CBUS input de-glitch 0: disalbe, 1: enable	R/W	0
	RegOSCDivSel[2:0]	6:4	OSCCLK divide counter selection	R/W	100
	Reg100msTOAdj[1:0]	3:2	00: 100ms, 01: 99ms, 10: 101ms, 11: reserved	R/W	00
	RegEnCBusNack	1	Enable CBUS Nack bit protocol	R/W	0
	RegEn100msCnt	0	Enable 100ms calibration counter	R/W	0
02	Reg10usTimeInt[7:0]	7:0	10us time base integer number bit[7:0]	R/W	0xC8
03	Reg10usTimeInt[8]	7	10us time base integer number bit[8]	R/W	0
	Reg10usTimeFlt[6:0]	6:0	10us time base floating number	R/W	0000000
04	RCBusDDCHangInt	7	CBUS DDC I2C BUS Hang interrupt Write '1' to clear this interrupt	W1C	
	RCBusWrBurstInt	6	MSC channel receive WRITE_BURST interrupt Write '1' to clear this interrupt	W1C	
	RCBusWrStatInt	5	MSC channel receive WRITE_STAT interrupt Write '1' to clear this interrupt	W1C	
	RCBusMSCRxMSGInt	4	MSC channel receive MSC_MSG interrupt Write '1' to clear this interrupt	W1C	
	RCBusRxPktFailInt	3	CBUS Link Layer receive a packet fail interrupt Write '1' to clear this interrupt	W1C	
	RCBusRxPktDoneInt	2	CBUS Link Layer receive a packet done interrupt Write '1' to clear this interrupt	W1C	
	RCBusTxPktFailInt	1	CBUS Link Layer send a packet fail interrupt Write '1' to clear this interrupt	W1C	
	RCBusTxPktDoneInt	0	CBUS Link Layer send a packet done interrupt Write '1' to clear this interrupt	W1C	
05	RCBusDDCRpdFailInt	7	CBUS DDC channel responder fail interrupt Write '1' to clear this interrupt	W1C	
	RCBusDDCRpdDoneInt	6	CBUS DDC channel responder done interrupt Write '1' to clear this interrupt	W1C	
	Reserved	5			
	RCLKModeChgInt	4	RegMHLSts01B[2:0] change interrupt Write '1' to clear this interrupt	W1C	
	RCBusMSCRpdFailInt	3	CBUS MSC channel responder fail interrupt Write '1' to clear this interrupt	W1C	
	RCBusMSCRpdDoneInt	2	CBUS MSC channel responder done interrupt Write '1' to clear this interrupt	W1C	
	RCBusMSCReqFailInt	1	CBUS MSC channel requester fail interrupt Write '1' to clear this interrupt	W1C	
	RCBusMSCReqDoneInt	0	CBUS MSC channel requester done interrupt Write '1' to clear this interrupt	W1C	
06	RVBusChgInt	7	VBUS detection status change interrupt Write '1' to clear this interrupt	W1C	
	RDCapRdyChgInt	6	RegMHLSts00B[0] change interrupt	W1C	

			Write '1' to clear this interrupt		
	RmuteChgInt	5	RegMHLSts01B[4] change interrupt Write '1' to clear this interrupt	W1C	
	RPathEnChgInt	4	RegMHLSts01B[3] change interrupt Write '1' to clear this interrupt	W1C	
	RCBusDisvFailInt	3	CBUS discovery process fail interrupt Write '1' to clear this interrupt	W1C	
	RCBusDisvDoneInt	2	CBUS discovery process done interrupt Write '1' to clear this interrupt	W1C	
	RWakeUpFailInt	1	CBUS discovery wakeup fail interrupt Write '1' to clear this interrupt	W1C	
	RWakeUpInt	0	CBUS disvovery wakeup interrupt Write '1' to clear this interrupt	W1C	
08	RDDCBusHangMask	7	Interrupt Mask 0: Enable the corresponding interrupt 1: Disalbe the corresponding interrupt		
	RCBusWrBurstMask	6		R/W	1
	RCBusWrStatMask	5		R/W	1
	RCBusMSCRxMSGMask	4		R/W	1
	RCBusRxPktFailMask	3		R/W	1
	RCBusRxPktDoneMask	2		R/W	1
	RCBusTxPktFailMask	1		R/W	1
	RCBusTxPktDoneMask	0		R/W	1
09	RCBusDDCRpdFailMask	7		R/W	1
	RCBusDDCRpdDoneMask	6			
	Reserved	5		R/W	1
	CLKModeChgMask	4			
	RCBusMSCRpdFailMask	3		R/W	1
	RCBusMSCRpdDoneMask	2		R/W	1
	RCBusMSCReqFailMask	1		R/W	1
	RCBusMSCReqDoneMask	0		R/W	1
0A	RVBusChgMask	7		R/W	1
	RDCapRdyChgMask	6		R/W	1
	RMuteChgMask	5		R/W	1
	RPathEnChgMask	4		R/W	1
	RCBusDisvFailMask	3		R/W	1
	RCBusDisvDoneMask	2		R/W	1
	RWakeUpFailInt	1		R/W	1
	RWakeUpInt	0		R/W	1
0C	RegPPHDCPOpt	7	PackedPixel mode HDCP option 0: use Ch1, 1: use Ch1/Ch2	R/W	0
	Reserved	6:4			
	RegPPHDCPOpt2	3	PackedPixel mode HDCP option 2 for video period 0: use Ch0/Ch1 ; 1: use Ch1/Ch2	R/W	0
	RegClrPathEn	2	FW send PATH_EN{Sink}=0 Write '1' to trigger PATH_EN{Sink}=0 packet	W1P	
	RegSetPathEn	1	FW send PATH_EN{Sink}=1 Write '1' to trigger PATH_EN{Sink}=1 packet	W1P	
	RegEnHWPathEn	0	HW PATH_EN control 0: Disable, 1: Enable	R/W	0
0E	Reserved	7:4			
	RegVBus5VTSel[1:0]	3:2	VBUS 5V deglitch time selection 00: 50ms, 01: 75ms, 10: 100ms, 11: 125ms	R/W	01
	Reserved	1:0			
0F	Reserved	7:6			
	RegEnPPGBSwap	5	GuardBand Swap when PackMode	R/W	1
	RegSWRstDDFSM	4	SW Reset Discovery and Disconnect FSM 0: Normal operation, 1: Stanby Mode Valid only when RegHWRstDDFSM='0'	R/W	1
	Reserved	3:0			
10	Reserved	7:5			
	RPATH_EN	4	PATH_EN status This is hardware internal status and it is updated after the PATH_EN transmission is done. PATH_EN{Sink}=1 to set status to 1 PATH_EN{Sink}=0 to set status to 0	RO	
	RVBus5Vdet	3	0: VBUS 5V not detected	RO	

			1: VBUS 5V detected		
	Reserved	2			
	REnVBUS	1	1: Pwr5V is output from VBUS	RO	
	REnCBUS	0	0: CBUS is not in connected state 1: CBUS is in connected state	RO	
12	R100msTimeCnt[7:0]	7:0	100ms counter value	RO	
13	R100msTimeCnt[15:8]	7:0		RO	
14	R100msTimeCnt[23:16]	7:0		RO	
15	RCBusTxPktFailSts[3:0]	7:4	CBUS Link Layer TX packet fail status Reset when RCBusTxPktFailInt is cleared [7]: Reserved [6]: Initiator arbitrate error [5]: Tx packet timeout [4]: Tx packet fail	RO	
	RCBusRxPktFailSts[3:0]	3:0	CBUS Link Layer RX packet fail status Reset when RCBusRxPktFailInt is cleared [3]: Reserved [2]: Rx parity check fail [1]: Rx packet timeout [0]: Rx packet fail	RO	
16	RCBUSDDCRpdFailSts[7:0]	7:0	CBUS DDC channel responder fail status Reset when RCBusDDCRpdFailInt is cleared [7]: TxState/=IDLE, receive new packet [6]: DDC bus hang [5]: transmit packet failed [4]: receive unexpected STOP [3]: 100ms timeout cause by link layer error [2]: 100ms timeout [1]: RxState/=IDLE, receive unexpected packet [0]: RxState=IDLE, receive non-SOP packet	RO	
17	RCBUSDDCRpdFailSts[15:8]	7:0	[7:1] : Reserved [0]: TxState/=IDLE, receive ddctxarblose	RO	
18	RCBusMSCReqFailSts[7:0]	7:0	CBUS MSC channel requester fail status Reset when RCBusMSCReqFailInt is cleared [7]: receive packet before transmit 1st packet [6]: un-enable HW retry and arbitration lose [5]: MSC_MSG Requester receive NACK packet [4]: receive ABORT packet [3]: Re-try threshold exceed [2]: protocol error [1]: 100ms timeout (too few packet) [0]: Incomplete packet	RO	
19	RCBusMSCReqFailSts[15:8]	7:0	[7:2]: Reserved [1]: FW mode RxPktFIFO is not empty [0]: FW mode fail	RO	
1A	RCBusMSCRpdFailSts[7:0]	7:0	CBUS MSC channel reponder fail status Reset when RCBusMSCRpdFailInt is cleared [7]: Protocol error [6]: MSC_MSG responder Busy [5]: 100ms timeout (too few packet) [4]: Incomplete packet [3]: receive dPacket in reponder Idle [2]: invalid command [1]: incremental Bad Offset [0]: initial bad Offset	RO	
1B	Reserved	7:2			
	RCBusMSCRpdFailSts[9:8]	1:0	CBUS MSC channel responder fail status Reset when RCBusMSCRpdFailInt is cleared [1]: receive ABORT packet [0]: Re-try threshold exceed	RO	
1C	Reserved	7:3			
	RMSCMSGBusy	2	RX MSG register is valid	RO	
	RCBusMSCBusy	1	CBUS MSC channel busy	RO	
	RCBusDDCBusy	0	CBUS DDC channel busy	RO	
1D	RegDDCErrCode[7:0]	7:0	CBUS DDC channel ERRORCODE	R/W	0x00
1E	RegMSCErrCode[7:0]	7:0	CBUS MSC channel ERRORCODE	R/W	0x00
1F	RSStatus	7:0	CBUS Discovery's FSM status	RO	

28	RegCBUSTimerAdj	7		R/W	0
	RegForceMode	6		R/W	0
	RegDongleMode	5	1: Dongle Mode, 0: Receiver Mode	R/W	0
	RegForce_MHLMode	4	1: Force input MHL Mode	R/W	0
	RegCBUSFloatAdj	3	Discovery related pulse width select	R/W	0
	RegSState5_EN	2	1: Permit state transition to Sink5_FloatCBus	R/W	1
	RegForce_Standby	1	1: Force Discovery module to Standby state	R/W	0
	RegVBUS_DET_EN	0	1: enable VBUS detect	R/W	1
29	Reg10usSrcSel	7	0: from Calibration 1: from Crystal 27MHz	R/W	0
	RegVBUSDGSel	6:4	VBUS Deglitch select	R/W	000
	RegCBUSDGSel	3:2	CBUS Deglitch select	R/W	00
	RegCDDGSel	1:0	CDSense Deglitch select	R/W	00
2A	Reserved	7:5			
	RegWKpulseSAdj	4		R/W	0
	RegWKpulseLAdj	3		R/W	0
	Reg5VStableTSel	2:1	Power 5V stable time after RDetCDSense goes high. 00: 75ms , 01: 100ms, 10: 125ms, 11: 150ms	R/W	01
	RegHWRstDDFSM	0	1: enable HW mode for RstDDFSM 0: enable SW mode for RstDDFSM	R/W	1
30	Reg_TParityEn	7	Test parity enable	R/W	0
	Reg_TParity	6	Test parity value	R/W	0
	Reg_RetryMax	5:0	Retry packet number of times	R/W	0x20
31	Reg_CBusOESel	7	Time of Cbus OE selection for driving high 0: 200ns, 1: 300ns	R/W	0
	Reg_EnArbNack	6	Enable arbitration using Nack bit	R/W	0
	Reg_ARB_Bit	5:0	CBUS arbitration Low time	R/W	0x0A
32	Reg_BurstTime	7:0	CBUS requester continue time after ack	R/W	0x0C
33	Reg_PktNumMax	7:0	CBUS initiator output packet maximum number	R/W	0x18
34	Reg_SyncMax	7:0	Sync maximum time	R/W	0x17
35	Reg_SyncMin	7:0	Sync minimum time	R/W	0x07
36	Reg_AckHigh	7:4	ACK high to low time	R/W	0x8
	Reg_AckLow	3:2	ACK low pulse time	R/W	01
	Reg_RxAckSel	1	Rx ACK selection, 0: external, 1: internal	R/W	1
	Reg_EnArbDrvH	0	Enable CBUS driving High at arbitration	R/W	1
37	Reg_PacketEnd	7:0	Follower output packet done	R/W	0x13
38	RegEnDDCStopBusy	7	1: Enable DDC Stop Busy function	R/W	1
	RegRcvAbortRpt	6	1: reply to error status when receive ABORT.	R/W	1
	RegEnRtnAbort	5	1: reply Abort when receive unexpected EOF.	R/W	0
	RegUnexpStopRpy	4	1: reply error to Source when receive unexpected Stop.	R/W	1
	RegEnRptStr	3	1: enable I2C repeat start protocol.	R/W	1
	RegPCReq	2	0: generate I2C clocks. 1: Abort I2C Bus	R/W	0
	RegPCTrg	1	0 => 1: PC I2C request trigger	R/W	0
	RegMasterSel	0	I2C master select. 1: PC , 0: CBUS	R/W	0
39	RegCmd_Deglitch	7	1: Enable I2C Deglitch	R/W	0
	RegSoftDDCSDA	6	1: DDCSDA controlled by SW	R/W	0
	RegSoftDDCSCL	5	1: DDCSCL controlled by SW	R/W	0
	RegSoftDDC	4	1: Enable DDC access by SW	R/W	0
	RegGenCLKPulse	3:0	Generate DDCSCL number by SW	R/W	0000
3A	RegCmd_FiltTap	7	I2C Deglitch Filter Tap select	R/W	0
	RegCmd_FiltType	6	I2C Deglitch Filter Type select	R/W	0
	RegBusHoldT	5:0	I2C bus hold time	R/W	000011
3B	RegI2CStCnt	7:0	I2C frequency setting	R/W	0x63

3C	Reserved	7:4			
	RegEnI2CHWAbort	3	1: Enable HW I2C Abort when DDCBusHang	R/W	1
	RegScratchPadClr	2	1: clear scratch pad registers to 0	R/W	0
	RegOvWrPPMode	1	1: PPMode value when enable Over write	R/W	0
	RegEnOvWrPPMode	0	1: Enable over write PPMode value	R/W	0
3D	RDDCStatus	7:0	[7]: DDC's Arbitration Lose Status [6]: DDC's WaitBus Status [5]: DDC's NAK Status [4]: DDC Done (include SCLGen and Abort) [3]: DDC busy [2]: DDC in WaitBus State [1]: DDC Receive NAK [0]: DDC Normal operation Done	RO	
3E	RDDCDbg	7:0	[7]: DDC Bus Hang [6]: DDC request [5:4] : DDC request command [3:0] : I2C FSM state	RO	
50	RegMSCTxCmd[7:0]	7	WRITE_STAT/SET_INT	W1P	
		6	READ_DEVCAP	W1P	
		5	GET_MSC_ERRORCODE	W1P	
		4	GET_DDC_ERRORCODE	W1P	
		3	CLR_HPD	W1P	
		2	SET_HPD	W1P	
		1	GET_VENDOR_ID	W1P	
		0	GET_STATE	W1P	
51	RegMSCTxCmd[15:8]	7	FW_MODE	W1P	
		6:2	Reserved		
		1	MSC_MSG	W1P	
		0	WRITE_BURST	W1P	
52	RegMSCHwMask[7:0]	7	WRITE_STAT/SET_INT hardware mask 0: handled by HW, 1: handle by FW	R/W	0
		6	READ_DEVCAP hardware mask 0: handled by HW, 1: handle by FW	R/W	0
		5	GET_MSC_ERRORCODE hardware mask 0: handled by HW, 1: handle by FW	R/W	0
		4	GET_DDC_ERRORCODE hardware mask 0: handled by HW, 1: handle by FW	R/W	0
		3	CLR_HPD hardware mask 0: handled by HW, 1: handle by FW	R/W	0
		2	SET_HPD hardware mask 0: handled by HW, 1: handle by FW	R/W	0
		1	GET_VENDOR_ID hardware mask 0: handled by HW, 1: handle by FW	R/W	0
		0	GET_STATE hardware mask 0: handled by HW, 1: handle by FW	R/W	0
53	RegMSCHwMask[15:8]	7	FW_MODE hardware mask 0: enable FW mode, 1: disable FW mode	R/W	1
		6:2	Reserved		
		1	MSC_MSG hardware mask 0: handed by HW, 1: handle by FW	R/W	0
		0	WRITE_BURST hardware mask 0: handled by HW, 1: handle by FW	R/W	0
54	RegMSCTxValue0B[7:0]	7:0	Requester TX value byte 0	R/W	0x00
55	RegMSCTxValue1B[7:0]	7:0	Requester TX value byte 1	R/W	0x00
56	RMSCRxValue0B	7:0	Requester RX value byte 0	RO	
57	RxPktFIFORECnt	7:5		RO	
	TxPktFIFORECnt	4:2		RO	
	TxPktFIFOWECnt	1:0		RO	

58	RMSCTxPktFIFOStg[4:0]	7:3	MSC TX packet FIFO stage	RO	
	RMSCTxPktFIFO[10:8]	2:0	[15:8]=high byte for WRITE_BURST (only [10:8] can be Read Back)	R/W	
59	RMSCTxPktFIFO[7:0]	7:0	[10:9]=hdrbit[1:0], [8]=ctrlbit, [7:0]=value[7:0] Write low byte to push a packet to TxPktFIFO Read low byte to pop a packet from TxPktFIFO	R/W	
5A	RMSCRxPktFIFOStg[4:0]	7:3	MSC RX packet FIFO stage	RO	
	RMSCRxPktFIFO[10:8]	2:0	[10:9]=hdrbit[1:0], [8]=ctrlbit, [7:0]=value[7:0]	RO	
5B	RMSCRxPktFIFO[7:0]	7:0	Read low byte to pop a packet from RxPktFIFO	RO	
5C	RegEnPktFIFOBurst	7	0: Disable TxPktFIFO and RxPktFIFO burst mode 1: Enable TxPktFIFO and RxPktFIFO burst mode	R/W	0
	RegMSCBurstWrID	6	0: ID from TxPktFIFO 1: ID form MHL5E/5F	R/W	0
	RegMSCBurstWrOpt	5	WRITE_BURST command option 0: Write Adopter ID, 1: Not write Adopter ID	R.W	0
	RegMSCEnBurstWr	4	WRITE_BURST command mode 0: single mode, 1: burst mode	R/W	1
	RegEnMSCHwRty	3	MSC hardware retry 0: Disable, 1: Enable	R/W	0
	RegMSCRxUCP2Nack	2	Receive UCP when UCP_RECV_SUPPORT=0 0: return ACK, 1: return NACK	R/W	1
	RMSCRxPktFIFOClr	1	RX packet FIFO clear Write '1' to generate 1T pulse	W1P	
	RMSCTxPktFIFOClr	0	TX packet FIFO clear Write '1' to generate 1T pulse	W1P	
5D	RegVendorID[7:0]	7:0	Vendor ID	R/W	0x00
5E	RegWrBurstIDH[7:0]	7:0	ADOPTER_ID_H of the responder or BURST_ID_H for 3D Burst ID code	R/W	0x00
5F	RegWrBurstIDL[7:0]	7:0	ADOPTER_ID_L of the responder or BURST_ID_L for 3D Burst ID code	R/W	0x00
60	RMSGRxValue0B[7:0]	7:0	MSC_MSG responder RX value byte 0	RO	
61	RMSGRxValue1B[7:0]	7:0	MSC_MSG responder RX value byte 1	RO	
64	Reserved	7:5			
	RMSCRxScrPadNum[4:0]	4:0	(Read Only) Receive scratch pad byte number	RO	
66	Reserved	7:2			
	RegBurstWrTOSel	1:0		R/W	01
80	RegMHLCap00B	7:0	DEV_STATE[7:0]	R/W	0x00
81	RegMHLCap01B	7:4	MHL_VER_MAJOR[3:0]	R/W	0x2
		3:0	MHL_VER_MINOR[3:0]	R/W	0x0
82	RegMHLCap02B	7	Reserved		
		6:5	PLIM[1:0]	R/W	00
		4	POW	R/W	0
		3:0	DEV_TYPE[3:0]	R/W	0x1
83	RegMHLCap03B	7:0	ADOPTER_ID_H[7:0]	R/W	0x00
84	RegMHLCap04B	7:0	ADOPTER_ID_L[7:0]	R/W	0x00
85	RegMHLCap05B	7:6	Reserved		
		5	SUPP_VGA	R/W	1
		4	SUPP_ISLANDS	R/W	1
		3	SUPP_PPIXEL	R/W	0
		2	SUPP_YCBCR422	R/W	1
		1	SUPP_YCBCR444	R/W	1
		0	SUPP_RGB444	R/W	1
86	RegMHLCap06B	7:2	Reserved		
		1	AUD_8CH	R/W	1
		0	AUD_2CH	R/W	1
87	RegMHLCap07B	7	SUPP_VT	R/W	0
		6:4	Reserved		
		3	VT_GAME	R/W	0
		2	VT_CINEMA	R/W	0
		1	VT_PHOTO	R/W	0
		0	VT_GRAPHICS	R/W	0
88	RegMHLCap08B	7	LD_GUI	R/W	0
		6	LD_SPEAKE	R/W	1
		5	LD_RECORD	R/W	0
		4	LD_TUNER	R/W	0
		3	LD_MEDIA	R/W	0

		2	LD_AUDIO	R/W	0
		1	LD_VIDEO	R/W	0
		0	LD_DISPLAY	R/W	1
89	RegMHLCap09B	7:0	BANDWIDTH[7:0]	R/W	0x0F
8A	RegMHLCap10B	7:5	Reserved		
		4	UCP_RECV_SUPPORT	R/W	1
		3	UCP_SEND_SUPPORT	R/W	1
		2	SP_SUPPORT	R/W	1
		1	RAP_SUPPORT	R/W	1
		0	RCP_SUPPORT	R/W	1
8B	RegMHLCap11B	7:0	DEVICE_ID_H[7:0]	R/W	0x00
8C	RegMHLCap12B	7:0	DEVICE_ID_L[7:0]	R/W	0x00
8D	RegMHLCap13B	7:0	SCRATCHPAD_SIZE	R/W	0x10
8E	RegMHLCap14B	7:4	STAT_SIZE[3:0]	R/W	0x3
		3:0	INT_SIZE[3:0]	R/W	0x3
8F	RegMHLCap15B	7:0	Reserved		0x00
A0	RegMHLInt00B	7:5	(Interrupt Status) Wirte '1' to clear this interrupt		
		4	3D_REQ (Interrupt Status) Write '1' to clear this interrupt	W1C	
		3	GNT_WRT (Interrupt Status) Write '1' to clear this interrupt	W1C	
		2	REQ_WRT (Interrupt Status) Write '1' to clear this interrupt	W1C	
		1	DSCR_CHG (Interrupt Status) Write '1' to clear this interrupt	W1C	
		0	(Interrupt Status) Write '1' to clear this interrupt		
A1	RegMHLInt01B	7:2	(Interrupt Status) Write '1' to clear this interrupt		
		1	EDID_CHG (Interrupt Status) Write '1' to clear this interrupt	W1C	
		0	(Interrupt Status) Write '1' to clear this interrupt		
A2	RegMHLInt02B	7:0	(Interrupt Status) Write '1' to clear this interrupt		
A3	RegMHLInt03B	7:0	(Interrupt Status) Write '1' to clear this interrupt		
B0	RegMHLSts00B	7:1	Reserved		
		0	SCAP_RDY (Read Only)	RO	0
B1	RegMHLSts01B	7:5	Reserved		
		4	MUTED (Read Only)	RO	0
		3	PATH_EN (Read Only)	RO	0
		2:0	CLK_MODE[2:0] (Read Only) 011: Normal 24-bit mode 010: PackedPixel mode others: reserved	RO	011
B2	RegMHLSts02B	7:0	Reserved		0x00
B3	RegMHLSts03B	7:0	Reserved		0x00
C0	RegMHLPad00B[7:0]	7:0	Scratchpad register byte 0	RO	0x00
C1	RegMHLPad01B[7:0]	7:0	Scratchpad register byte 1	RO	0x00
C2	RegMHLPad02B[7:0]	7:0	Scratchpad register byte 2	RO	0x00
C3	RegMHLPad03B[7:0]	7:0	Scratchpad register byte 3	RO	0x00
C4	RegMHLPad04B[7:0]	7:0	Scratchpad register byte 4	RO	0x00
C5	RegMHLPad05B[7:0]	7:0	Scratchpad register byte 5	RO	0x00
C6	RegMHLPad06B[7:0]	7:0	Scratchpad register byte 6	RO	0x00
C7	RegMHLPad07B[7:0]	7:0	Scratchpad register byte 7	RO	0x00
C8	RegMHLPad08B[7:0]	7:0	Scratchpad register byte 8	RO	0x00
C9	RegMHLPad09B[7:0]	7:0	Scratchpad register byte 9	RO	0x00
CA	RegMHLPad10B[7:0]	7:0	Scratchpad register byte 10	RO	0x00
CB	RegMHLPad11B[7:0]	7:0	Scratchpad register byte 11	RO	0x00
CC	RegMHLPad12B[7:0]	7:0	Scratchpad register byte 12	RO	0x00
CD	RegMHLPad13B[7:0]	7:0	Scratchpad register byte 13	RO	0x00
CE	RegMHLPad14B[7:0]	7:0	Scratchpad register byte 14	RO	0x00
CF	RegMHLPad15B[7:0]	7:0	Scratchpad register byte 15	RO	0x00

CEC Control register of IT6801

86	RegCECSlaveAdr	7:0	I2C Slave Address for CEC	R/W	0xC8
0E	RegEnCRCLK	0	1: Enable RCLK for CEC	R/W	0

CEC Registers in I2C slave address of IT6801 CEC

CEC Control Registers				
Reg	Name	Bit	Definition	Default
00~05				
06	Reserved	7:6		
	TxFail_Int_Mask	5	0: Interrupt Enable 1: Interrupt Mask	1
	RxDone_Int_Mask	4	0: Interrupt Enable 1: Interrupt Mask	1
	TxDone_Int_Mask	3		1
	RxFail_Int_Mask	2		1
	Rx_Int_Mask	1		1
	Tx_Int_Mask	0		1
07	Reserved	7:5		000
				0
	DBGCEC_Sel	4:2	Select CEC debug pin	000
	Reserved	1:0		00
08	**Fire_Frame**	7	1: Fire CEC command out	0x48
	DBGCEC_Clr	6	1: Clear CEC interrupt for debug	
	CEC_OE	5	Force CEC output value	
	CEC_Force	4	Force CEC output regardless of normal function	
	CEC_SMT	3	Schmitt trigger of CEC IO 1: Enable 0: Disable	
	CEC_Rst	2	Reset CEC block 1: Enable 0: Disable	
	~~REFCLK_Rst~~	~~1~~	~~Software reset 1: Enable 0: Disable~~	
	Reg_CECInt_En	0	CEC interrupt enable 1: Enable 0: Disable	
09	DataBit_Sel	7	Select data bit 1: Increase 0.1ms 0: Normal	0x20
	Region_Sel	6	Select region for error bit 1: Whole region 0: Region form state Start to IDLE	
	RxSelf_Sel	5	Initiator received CEC bus data. 1: Disable 0: Enable	
	Refire	4	Retry to fire CEC command. 1: Enable 0: Disable	
	ACKTrig_Sel	3	Acknowledge for broadcast mode 1: ACK 0: NACK	
	Pulse_Sel	2	Select illegal bit as error bit 1: Enable 0: Disable	
	NACK_En	1	Acknowledge from follower to initiator 1: NACK 0: ACK	
	En100ms_Cnt	0	Used as a reference 100ms time interval for CEC calibration.	
0A	Reserved	7:5		0x00
	ArBit_Sel	4	Select bit time for arbitration lose. 1: 3 bit time 0: 5 bit time	

	BitEnd_Sel	3:2	Select logic 0 and logic 1 output bit time. 00: Standard 01: Logic 0 maximum and logic 1 minimum 10: Logic 1 maximum and logic 0 minimum	
	BusFree_Sel	1:0	Select bus free bit time. 00: Automatic 01: 3 bit time. 10: 5 bit time 11: 7 bit time	
0B	Data_Min	7:0	Minimum data bit time	0x14
0C	Timer_Unit	7:0	CEC timer unit, nominally 100us. This value should be decided from MS_Count.	0x59
0D	CEC_Drv[1:0]	7:6	00: 2.5mA, 01:5mA, 10:7.5mA, 11:10mA	01
	CEC_IOSR	5	CEC IO slew rate control	0
	CEC_IOPU	4	0: Normal, 1: Pull-up	1
		3:0		
0E~ 0F				

CEC Initiator Registers in I2C slave address of IT6801 CEC

10	Tx_Header	7:0	CEC initiator command header	0x00
11	Tx_Opcode	7:0	CEC initiator command opcode	0x00
12	Tx_Operand1	7:0	CEC initiator command operand1	0x00
13	Tx_Operand2	7:0	CEC initiator command operand2	0x00
14	Tx_Operand3	7:0	CEC initiator command operand3	0x00
15	Tx_Operand4	7:0	CEC initiator command operand4	0x00
16	Tx_Operand5	7:0	CEC initiator command operand5	0x00
17	Tx_Operand6	7:0	CEC initiator command operand6	0x00
18	Tx_Operand7	7:0	CEC initiator command operand7	0x00
19	Tx_Operand8	7:0	CEC initiator command operand8	0x00
1A	Tx_Operand9	7:0	CEC initiator command operand9	0x00
1B	Tx_Operand10	7:0	CEC initiator command operand10	0x00
1C	Tx_Operand11	7:0	CEC initiator command operand11	0x00
1D	Tx_Operand12	7:0	CEC initiator command operand12	0x00
1E	Tx_Operand13	7:0	CEC initiator command operand13	0x00
1F	Tx_Operand14	7:0	CEC initiator command operand14	0x00
20	Tx_Operand15	7:0	CEC initiator command operand15	0x00
21	Tx_Operand16	7:0	CEC initiator command operand16	0x00
22	Reserved	7:4		0x00
	Logical_Addr	3:0	CEC target logical address	
23	Reserved	7:5		0x00
	Out_Num	4:0	CEC output byte size in a frame	
24~ 2F				

CEC Follower Registers in I2C slave address of IT6801 CEC

30	Rx_Header	7:0	RO. CEC follower command header	0x00
31	Rx_Opcode	7:0	RO. CEC follower command opcode	0x00
32	Rx_Operand1	7:0	RO. CEC follower command operand1	0x00
33	Rx_Operand2	7:0	RO. CEC follower command operand2	0x00
34	Rx_Operand3	7:0	RO. CEC follower command operand3	0x00
35	Rx_Operand4	7:0	RO. CEC follower command operand4	0x00
36	Rx_Operand5	7:0	RO. CEC follower command operand5	0x00
37	Rx_Operand6	7:0	RO. CEC follower command operand6	0x00
38	Rx_Operand7	7:0	RO. CEC follower command operand7	0x00
39	Rx_Operand8	7:0	RO. CEC follower command operand8	0x00
3A	Rx_Operand9	7:0	RO. CEC follower command operand9	0x00
3B	Rx_Operand10	7:0	RO. CEC follower command operand10	0x00
3C	Rx_Operand11	7:0	RO. CEC follower command operand11	0x00
3D	Rx_Operand12	7:0	RO. CEC follower command operand12	0x00
3E	Rx_Operand13	7:0	RO. CEC follower command operand13	0x00
3F	Rx_Operand14	7:0	RO. CEC follower command operand14	0x00
40	Rx_Operand15	7:0	RO. CEC follower command operand15	0x00
41	Rx_Operand16	7:0	RO. CEC follower command operand16	0x00
42	Reserved	7:5		0x00
	In_Cnt	4:0	RO. CEC follower received bytes.	

CEC Misc. Registers in I2C slave address of IT6801 CEC

43	Reserved	7:5		0x00
	Out_Cnt	4:0	RO. CEC initiator output bytes.	
44	Reserved	7		0x00
	Ready_Fire	6	RO. Bus ready for firing a CEC command.	0x00
	Error_Status	5:4	RO. Error status. 00: No error occurs. 01: Received data period < minimum data bit period. 10: Illegal held-low period. 11: Both	0x00
	Out_Status	3:2	RO. Output status. 00: Received ACK 01: Received NACK 10: Retry, if no ACK, NACK or arbitration lose. 11: Fail	
	Bus_Status	1	RO. Bus status. 0: Busy 1: Free	
	Reserved	0		
45	MS_Count	7:0	RO. MS_Count[7:0]	0x00
46	MS_Count	7:0	RO. MS_Count[15:8]	0x00
47	Reserved	7:4		0x00
	MS_Count	3:0	RO. MS_Count[19:16]	
48	Reserved	7:6		0x00
	CEC_Int	5	CEC interrupt status	
	DBG_Int	4	CEC interrupt for debug	
	DBG_State	3:0	RO. Debug CEC error state.	
49	Reserved	7:5		0x00
	DBG_Block	4:0	RO. Debug CEC error block number	
4A	Reserved	7:4		0x00
	DBG_Bit	3:0	RO. Debug CEC error bit number.	
4B	DBG_Timing	7:0	Debug CEC error data bit time.	0x00
4C	Reserved	7:6		0x00
	TxFail_Int	5	R: CEC initiator output fail interrupt. W: Write 1 clear this interrupt	
	RxDone_Int	4	R: CEC received finish interrupt. W: Write 1 clear this interrupt	
	TxDone_Int	3	R: CEC output finish interrupt. W: Write 1 clear this interrupt	
	RxFail_Int	2	R: CEC received fail interrupt. W: Write 1 clear this interrupt	
	Rx_Int	1	R: CEC follower received byte interrupt. W: Write 1 clear this interrupt	
	Tx_Int	0	R: CEC initiator output byte interrupt. W: Write 1 clear this interrupt	
4D~ FF				

EDID Control register of IT6801

87	RegEDIDSlaveAdr	7:1	I2C Slave Address for EDID	R/W	1010100
	RegEnEDIDSlaveAdr	0	1: Enable access EDID block	R/W	0
C0	Reserved	7			
	RegEnMultiSeg	6	1: Enable multiple segment	R/W	0
	RegSoftEDIDRst	5	1: EDID reset	R/W	0
	RegAutoPwdEDID	4	1: auto powerdown EDID	R/W	0
	RegEDIDAdrSel	3	1: EDID address A2 ; 0: EDID address A0	R/W	0
	RegEnDetDDC	2	1: Enable monitor DDC detect start	R/W	1
	Reg_P1DisableShadow	1	1: disable Port 1 Internal EDID	R/W	1
	Reg_P0DisableShadow	0	1: disable Port 0 Internal EDID	R/W	1

EDID Register in I2C slave address of IT6801 EDID.

Reg	Register Name	Bit	Definition	Default
00	EDID_00h	7:0		
~	…			
FF	EDID_FFh	7:0		