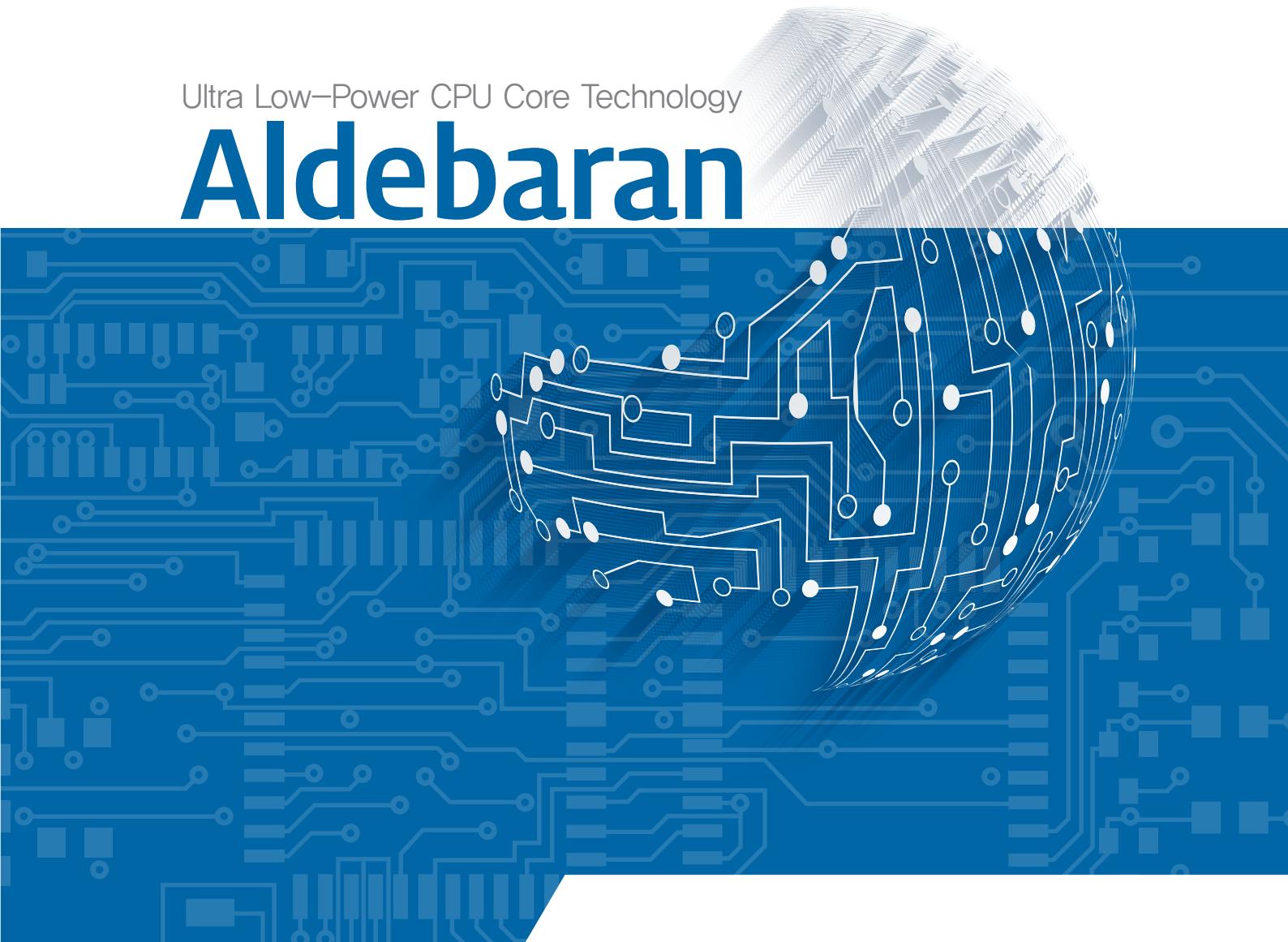


Ultra Low-Power CPU Core Technology

# Aldebaran



SoC Research Department

## Aldebaran CPU Core

The Aldebaran<sup>1)</sup> CPU core was developed independently by the Electronics and Telecommunications Research Institute (ETRI).

It is based on a power-efficient microarchitecture and includes the ADE (Aldebaran Software Development Environment), an open source (GNU) based SW toolchain (C/C++ compiler, assembler, linker, debugger, bootloader, etc) for efficient adoption into a system.

ETRI is the sole owner, developer, and maintainer of intellectual property rights of the technology behind Aldebaran. The hardware design code (RTL: Register Transfer Level Code) of Aldebaran's micro-architecture and CPU core can be obtained by a client from ETRI and further customized development is possible according to the requests of the client.

The Aldebaran CPU core (S2, S4) design consists of a 13 stage dual-issue superscalar architecture that includes performance enhancing mechanisms such as branch prediction and an instruction queue, as well as in-order execution, cache access optimization, DVFS (Dynamic Voltage-Frequency Scaling) mechanisms for optimized power efficiency. With its high performance and minimal power consumption architecture, Aldebaran is optimal for Wearable Smart Device applications.

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### Aldebaran(S2) Specification

- Dual-issue Superscalar Architecture with L1 I/D Cache, L2, and TLB
- Branch prediction with 3.7KB BTB (Branch Target Buffer), 1KB BP (Branch Predictor), and 10-bit GHR (Global History Register)
- I/D Cache with 32KB/32KB 4-way Set-associative Data memory, 2.12KB Tag, and 32Bytes/Line
- I/D TLB with Fully-associative 32-entry and 64-bit PTE(Page Table Entry) with selective FLUSH/PROBE
- Dual-rail decode with instruction queue
- In-order scheduler with Scoreboard
- RF(Register File) with 10 Read/Write ports
- Execution Queue for parallel execution
- Superscalar execution unit including 2 integer units, 1 load store, and Single & Double-Precision FPU
- 800MHz@65nm, 1.1V, 1.2GHz@40nm, 1.0V

Linux OS, RTOS (RTEMS, FreeRTOS), AUTOSAR OS, etc. have been ported onto Aldebaran enabling it to be used for a wide variety of applications. A Linux kernel optimized for Aldebaran's architecture and MMU (Memory Management Unit) is provided to ensure that clients preferring Linux OS have a convenient development platform for their target products. Further, the platform is furnished with several peripheral device IP device drivers to provide a complete Aldebaran CPU core based SoC and software integration platform.

The Aldebaran-S2 is a System on Chip (SoC) realizing the Aldebaran CPU core on TSMC 65nm technology with a maximum operating frequency of 800MHz while boasting an industry leading energy efficiency of 0.24 mW/Hz.

With the application of new low-power high performance CPU core technology, an effective and efficient technical support, and optimizations customized to needs of the industry, the Aldebaran CPU Core represents a significant milestone in securing home-grown CPU core technology. It is predicted to have a lasting impact in boosting national competitiveness in the CPU core industry, reducing the technological gap, and enhancing product competitiveness of its clients.

### CPU Core Technology

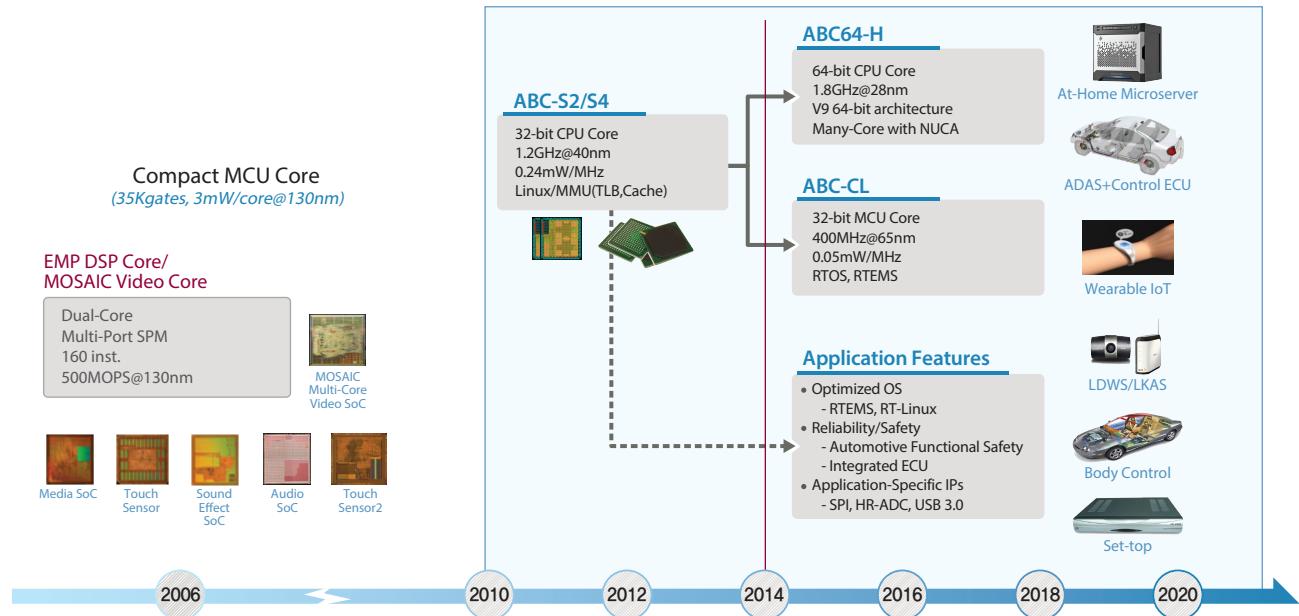
In almost all IT devices, the CPU (Central Processing Unit) generally assumes an integral role as the brain of the system. Typically, software consists of code that defines the work the CPU must carry out for a given application. Software application code written by the developer is translated to machine language, a language the CPU understands, via the compiler, and the CPU executes the instructions that correspond to the code originally specified by the developer.

The rapid evolution of IT has brought us to an era of smart devices, wearable devices, IoT devices, etc. CPUs undoubtedly play a vital role in these devices and is a crucial factor that determines a product's performance, battery power consumption, functionality, etc. Historically, development of CPU technology has largely been limited to global companies in technologically advanced countries such as the USA, Japan, EU, etc. While national (Rep. of Korea) Processor SoC (System-on-Chip) design and chip fabrication technology are world-class, CPU core technology is lagging and mainly dependent on importing of foreign technology that entails huge royalty costs.

The Aldebaran CPU core, which boasts an original microarchitecture, cutting edge low-power technology, and an open-source based user-friendly development environment, was developed independently by the Electronics and Telecommunications Research Institute (ETRI) in an effort to enhance the competitiveness of nationally possessed CPU core and software technology.

1) Aldebaran is the brightest star in the zodiac constellation of Taurus.

## Aldebaran Roadmap



## Aldebaran Portfolio

Code name	Application Category			Architecture	Cache	MMU <sup>4)</sup>	FT <sup>5)</sup>	OS	Status
	Speed <sup>1)</sup>	Lo-Power <sup>2)</sup>	Reliability <sup>3)</sup>						
S2	○	○	—	Core 32bit, AXI 32bit	L1:32K	I/D TLB <sup>6)</sup> FA <sup>7)</sup>	—	Linux RTOS	Complete
S4	○	○	—	Core 32bit AXI 64bit	L1:32K L2:512K	I/D TLB FA	—	Linux RTOS	Complete
S4T	○	○	○	Core 32bit AXI 64bit	L1:32K L2:32K	I/D TLB FA	DCLS <sup>8)</sup>	AUTOSAR RTOS	Complete
H1	○	△	—	Core 64bit AXI 128bit	L1: 32K L2: 1M L3: 4M	I/D TLB PTE cache <sup>9)</sup> FA	—	Linux	2015 Q4
CL	○	○	—	Core 32bit AXI 32bit	L1: I/D 8K-32K <sup>10)</sup>	—	—	RTOS	Complete
CLT	○	○	○	Core 32bit AXI 32bit	L1: I/D 8K-32K	—	ETRI FTA <sup>11)</sup>	RTOS RT-Linux	2015 Q3

1) Applications that require GHz level high performance such as Linux OS, automotive ADAS vision applications, etc

2) Applications that require 600MHz level performance with low power for longer battery life such as IoT, wearable devices

3) Applications that require Functional Safety as described by ISO26262, ISO19451, IEC61508

4) MMU(Memory Management Unit) used for Dynamic Thread Allocation/Deallocation

5) FT(Fault-Tolerance): Mechanisms for the detection and recovery from permanent fault and transient fault in the CPU core

6) TLB(Translation Lookaside Buffer): basic component of MMU that caches a portion of the Page Table

7) The TLB in Aldebaran is Fully Associative

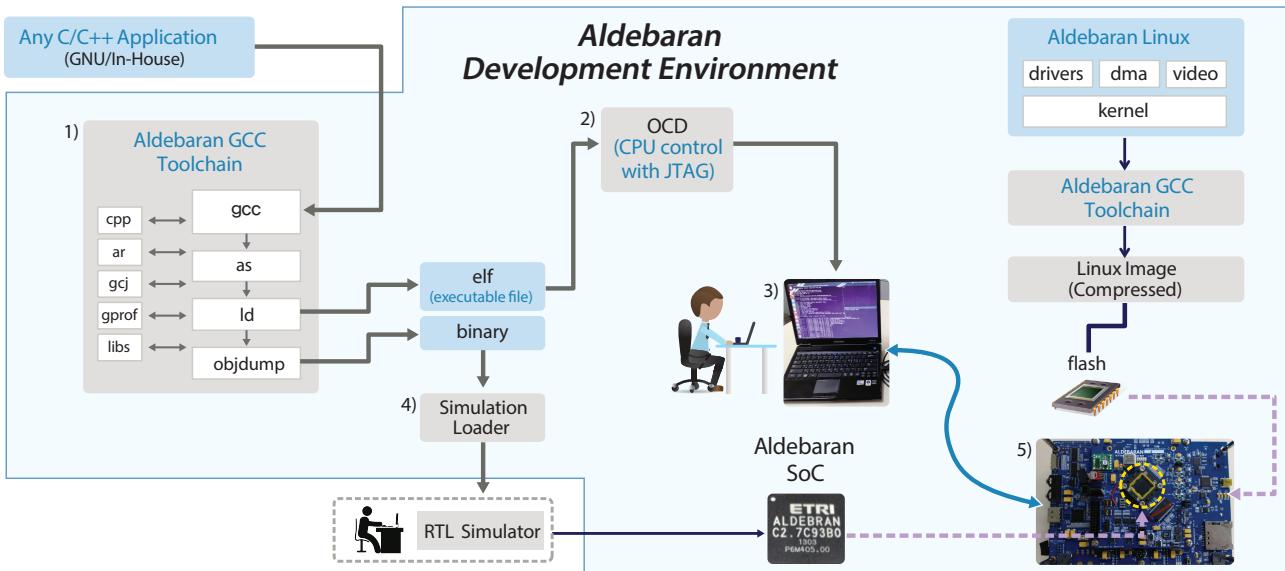
8) DCLS(Dual-Core Lock Step): Technique to detect faults by comparing two cores running the same work but with a temporal difference

9) The PTE(Page Table Entry) is a basic element of the Page Table and a separate cache for the PTE is included for H1

10) Index, Way (Associativity) of L1 cache in Aldebaran can be configured from 8K to 32K

11) Additional circuitry for ETRI FT-arch that minimizes the redundancy area while maintaining performance for fault detection and recovery

## ADE(Aldebaran Development Environment)



The Aldebaran Development Environment (ADE) consisting of the GNU SW toolchain and Aldebaran OS(Linux, RTEMS) are provided for application development and optimization.

- 1) The Aldebaran compiler is based on Machine Description optimized for Aldebaran's microarchitecture and the Assembler is designed customized for Aldebaran CPU core's general and support registers.
- 2) The executable produced by the Linker can be run on the system board using the Aldebaran On-Chip Debugger(OCD) to perform source-level debugging.
- 3) Within the Aldebaran CPU core, a separate high speed debugging module called "Aldebaran Eyes" is accessible via USB2JTAG interface (5-pin) communication. Aldebaran Eyes provides a means for performing CPU core functions Stop, Resume, Register probe/set, TLB probe-/set, Memory probe/set, as well as a variety of software debugging functions for debugging purposes while occupying minimal area.
- 4) Separate from this, scripts provided within ADE can be utilized to run SoC simulation for the executables.
- 5) Several evaluation boards including SoC based systems (such as the Aldebaran-S2), Xilinx Virtex-7 2000T FPGA based system boards, and Xilinx Artix-7 200T FPGA based low-cost system boards are available.

## Aldebaran Platform IP

The Aldebaran CPU core is fully compatible with AXI protocol based On-Chip Bus and constructing an SoC is greatly simplified. The following IPs are furnished for companies that wish to collaborate with ETRI to develop a product based on the Aldebaran CPU core.

IP	Description	Spec. <sup>1)</sup>
VC	Video Display Unit	Internal DMA, HDMI Support
iROM/iRAM	Internal ROM/RAM	Bootloader in ROM/RAM
ARESET	System init. Controller	System initializer
PMU	Power Management Unit	CPU power-down mode control
NFC	NAND Flash Controller	128M-32Gbytes, 400Mbps
SDC	SD Controller	SD card/SDIO/SPI
SMC	Host Interface Controller	Ethernet(LAN9220)
DMA	DMA Controller	Multi-channel/dimension DMA
USBHS	USB Host Controller	USB 1.1
Timer	Timer	Periodic/On-Shot, 4sets
WDT	Watch-dog Timer	Watchdog interrupt
RTC	Real-Time Clock	Leap year, BCD, 32.768khz XTAL
UART	Serial 8-bit Transceiver	UART 16550
AC97	AC97 codec	Audio output
I2C	Inter-IC Control	7-bit/10-bit, Master/Slave
PWM	Pulse-Width Modulation	PWM signal generation
GPIO	General-Purpose I/O	Bidirectional, upto 64 GPIOs
CAN	Controller Area Network	Automotive CAN 2.0A, 2.0B, FD
FM	Fault Manager	Automotive Fault Management

1) The above is an abbreviated specification. Details can be found in Aldebaran Platform Architecture Manual.