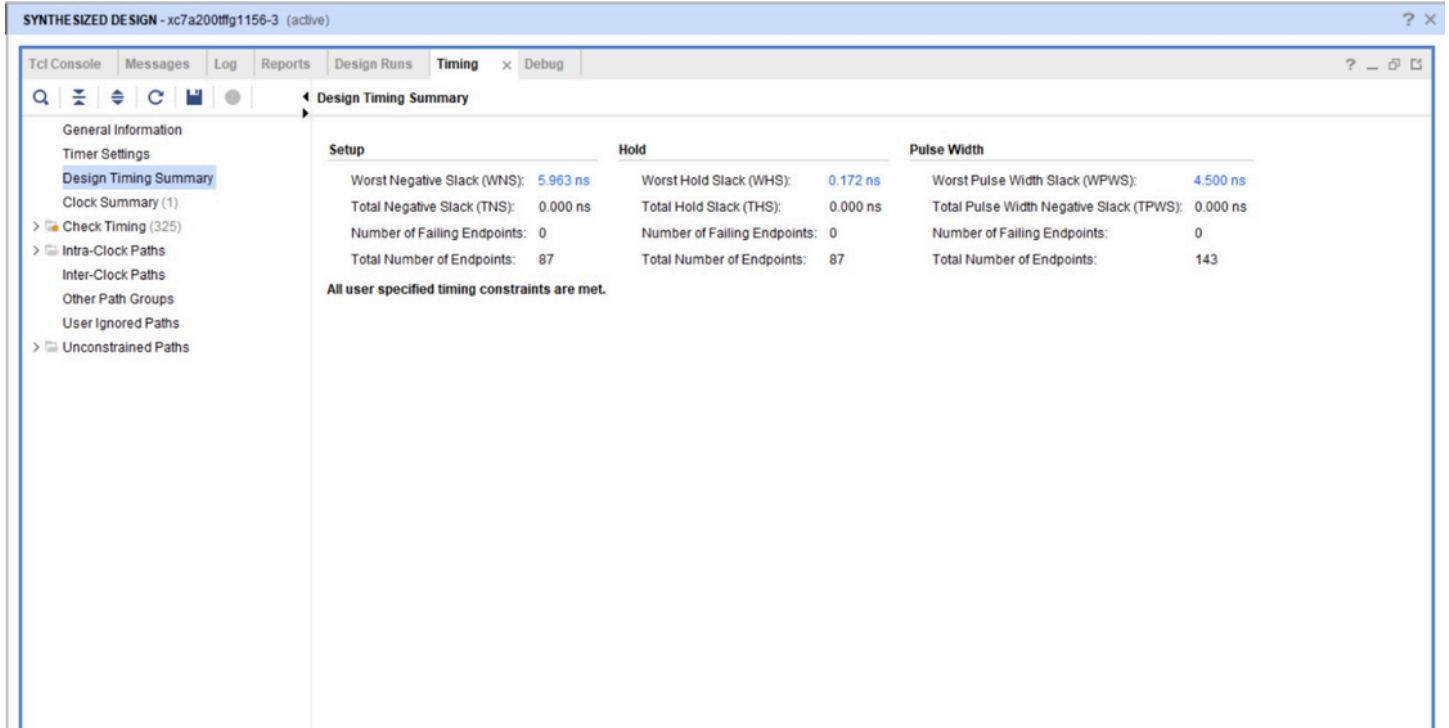


Timing_report_snippits

After synthesis :



SYNTHESIZED DESIGN - xc7a200tffg1156-3 (active)

Tcl Console Messages Log Reports Design Runs Timing x Debug

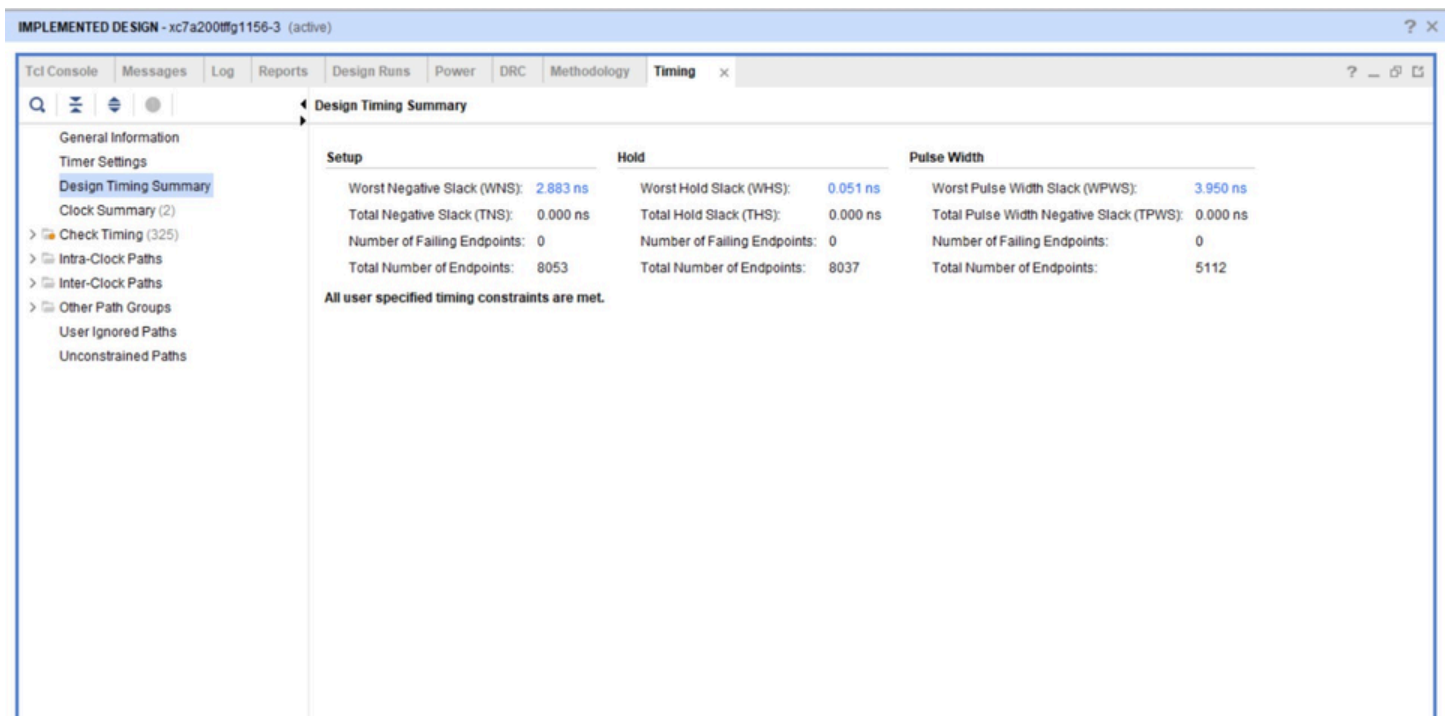
Design Timing Summary

General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (325)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 5.963 ns	Worst Hold Slack (WHS): 0.172 ns	Worst Pulse Width Slack (WPWS): 4.500 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 87	Total Number of Endpoints: 87	Total Number of Endpoints: 143

All user specified timing constraints are met.

After implementation :



IMPLEMENTED DESIGN - xc7a200tffg1156-3 (active)

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing x

Design Timing Summary

General Information
Timer Settings
Design Timing Summary
Clock Summary (2)
Check Timing (325)
Intra-Clock Paths
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths

Setup	Hold	Pulse Width
Worst Negative Slack (WNS): 2.883 ns	Worst Hold Slack (WHS): 0.051 ns	Worst Pulse Width Slack (WPWS): 3.950 ns
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): 0.000 ns
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: 0
Total Number of Endpoints: 8053	Total Number of Endpoints: 8037	Total Number of Endpoints: 5112

All user specified timing constraints are met.