

# utilization\_report\_snippits

After synthesis :

SYNTHESIZED DESIGN - xc7a200tfg1156-3 (active)

Tcl Console Messages Log Reports Design Runs Utilization x Timing Debug

Hierarchy

Name	Slice LUTs (134600)	Slice Registers (269200)	DSP s (740)	Bonded IOB (500)	BUFGCTRL (32)
DSP_48	257	141	1	326	1

Left sidebar (Hierarchy):

- Summary
- ▼ Slice Logic
  - ▼ Slice LUTs (<1%)
    - LUT as Logic (<1%)
  - ▼ Slice Registers (<1%)
    - Register as Flip Flop (<1%)
- Memory
- ▼ DSP
  - ▼ DSPs (<1%)
    - DSP48E1 only
- ▼ IO and GT Specific
  - ▼ Bonded IOB (65%)
    - IOB Master Pads
- ▼ Clocking
  - BUFGCTRL (3%)
- Specific Feature
- Primitives
- Black Boxes
- Instantiated Netlists

After Implementation :

IMPLEMENTED DESIGN - xc7a200tfg1156-3 (active)

Tcl Console Messages Log Reports Design Runs Power DRC Methodology Timing Utilization x

Hierarchy

Name	Slice LUTs (133800)	Slice Registers (267600)	F7 Muxes (66900)	F8 Muxes (33450)	Slice (33450)	LUT as Logic (133800)	LUT as Memory (46200)	LUT Flip Flop Pairs (133800)	Block RAM Tile (365)	DSP s (740)	Bonded IOB (500)	BUFGCTRL (32)	BSCAN2 (4)
▼ DSP_48	2725	4202	97	9	1490	2251	474	1590	8	1	326	2	1
> u_dbg_hub (dbg_hub)	475	727	0	0	254	451	24	302	0	0	0	1	1
> u_ila_0 (u_ila_0)	1993	3334	97	9	1157	1543	450	1220	8	0	0	0	0

Left sidebar (Hierarchy):

- Summary
- ▼ Slice Logic
  - ▼ Slice LUTs (2%)
    - ▼ LUT as Memory (1%)
      - LUT as Shift Register
      - LUT as Distributed RAM
    - LUT as Logic (2%)
  - F8 Muxes (<1%)
  - F7 Muxes (<1%)
  - ▼ Slice Registers (2%)
    - Register as Flip Flop (2%)
- ▼ Slice Logic Distribution
  - ▼ Slice (4%)
    - SLICEM
    - SLICEL
  - ▼ LUT as Memory (1%)
    - ▼ LUT as Shift Register
      - using O5 output only
      - using O6 output only
      - using O5 and O6
    - ▼ LUT as Distributed RAM
      - using O5 and O6
    - ▼ LUT Flip Flop Pairs (1%)
      - LUT-FF pairs with one or more fully used LUT-FF pairs