Cairo University
Faculty of Engineering
Dept. of Electronics and Electrical Communications
Second Year

Analog Electronics
ELC 2060

Electronics Project

Presented to ENG. Mahamed Ramadan

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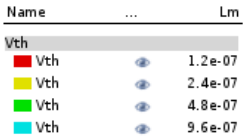
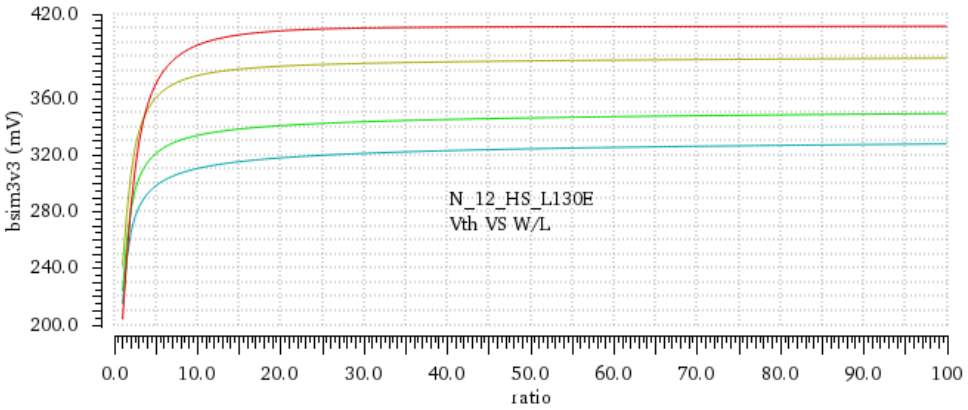
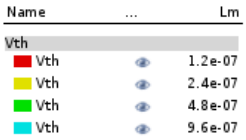
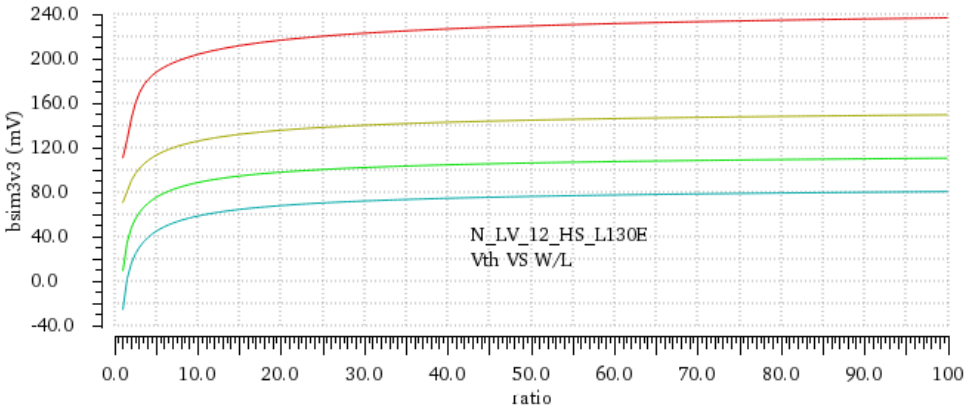
Task #1:

1. Plotting:
   - For V_{th}:

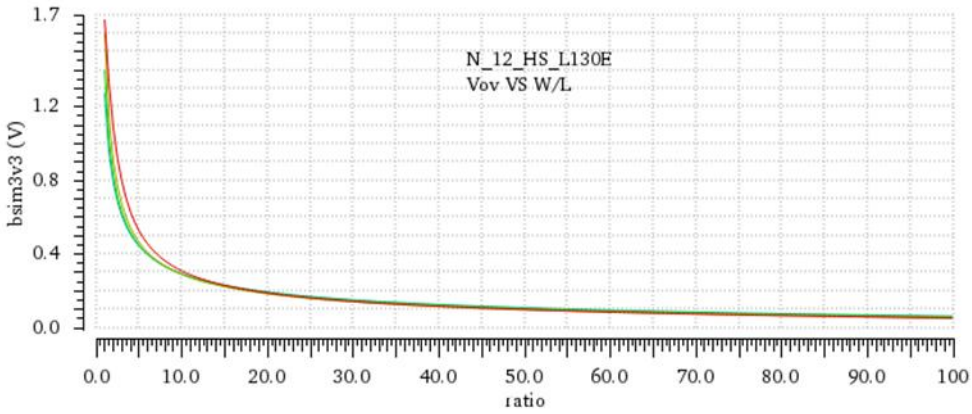


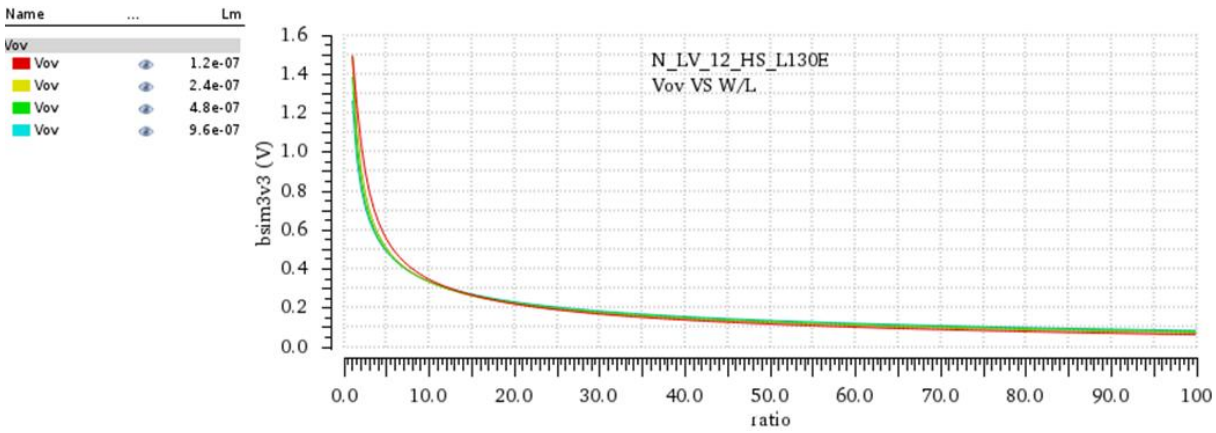




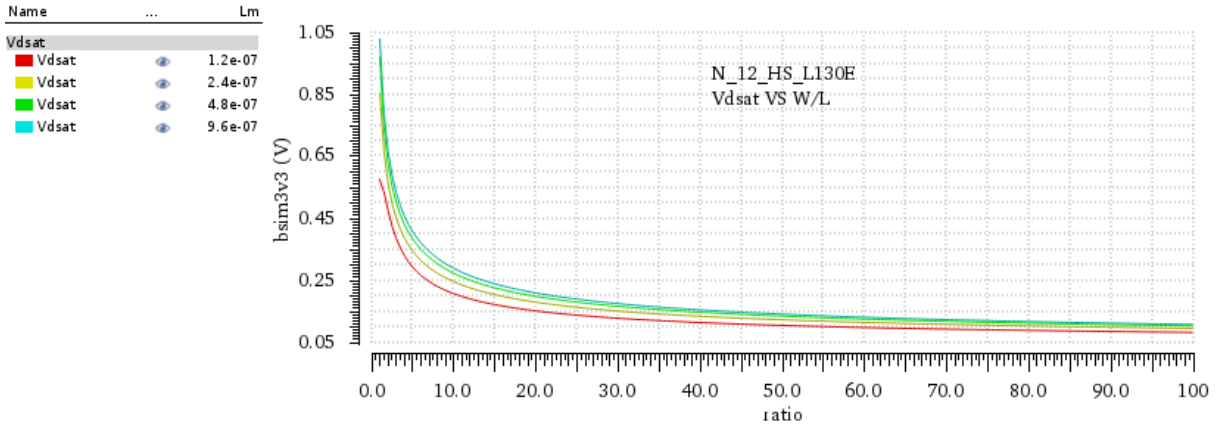


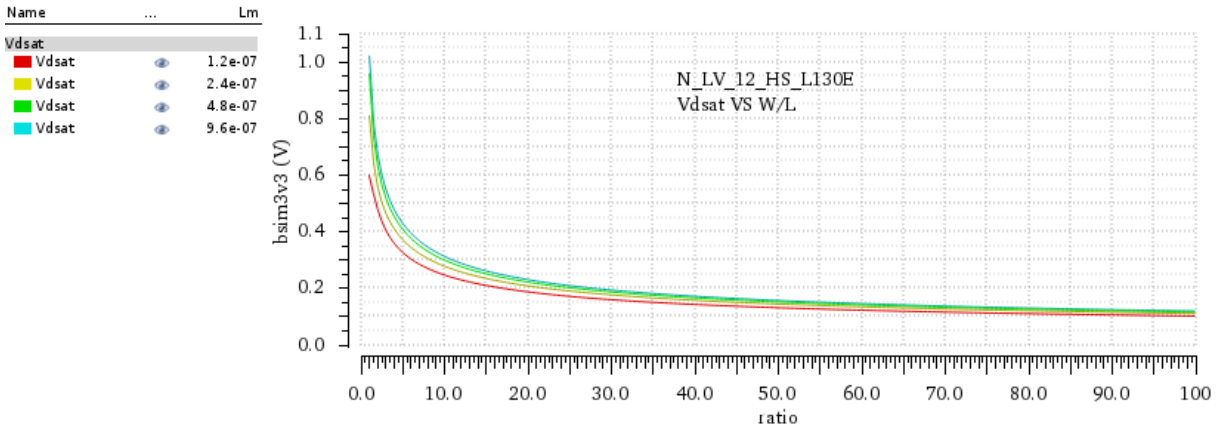
   - For V_{OV}:



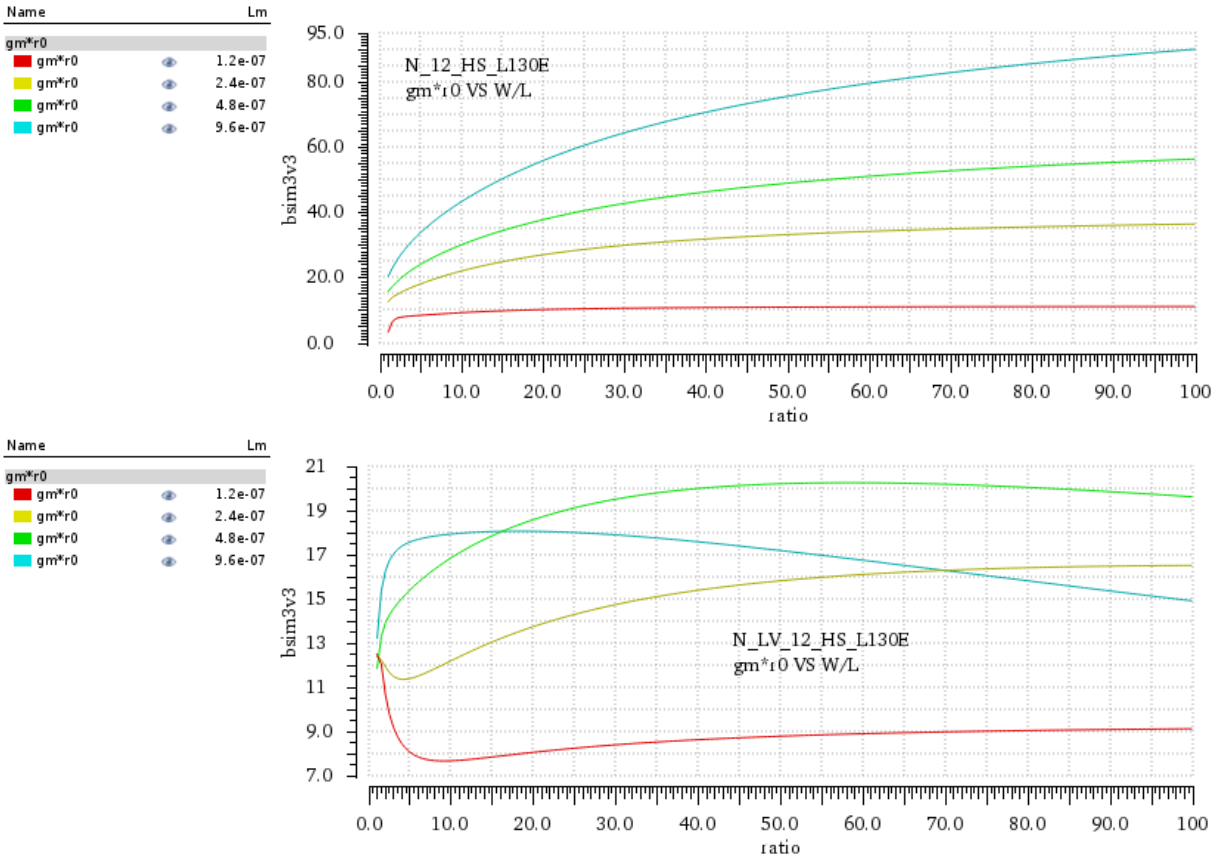

Name ... Lm
Vov
Vov 1.2e-07
Vov 2.4e-07
Vov 4.8e-07
Vov 9.6e-07
N_LV_12_HS_L130E
Vov VS W/L
bsim3v3 (V)
1.6
1.4
1.2
1.0
0.8
0.6
0.4
0.2
0.0
0.0 10.0 20.0 30.0 40.0 50.0 60.0 70.0 80.0 90.0 100
ratio

- For V_{Dsat}:


Name ... Lm
Vdsat
Vdsat 1.2e-07
Vdsat 2.4e-07
Vdsat 4.8e-07
Vdsat 9.6e-07
N_12_HS_L130E
Vdsat VS W/L
bsim3v3 (V)
1.05
0.85
0.65
0.45
0.25
0.05
0.0 10.0 20.0 30.0 40.0 50.0 60.0 70.0 80.0 90.0 100
ratio


Name ... Lm
Vdsat
Vdsat 1.2e-07
Vdsat 2.4e-07
Vdsat 4.8e-07
Vdsat 9.6e-07
N_LV_12_HS_L130E
Vdsat VS W/L
bsim3v3 (V)
1.1
1.0
0.8
0.6
0.4
0.2
0.0
0.0 10.0 20.0 30.0 40.0 50.0 60.0 70.0 80.0 90.0 100
ratio

- For gm*r_O:



2. Mention the long-channel equation for V_{th}, V_{ov}, &gm*r_0. Is the trend of the simulations similar to the equations?

- For V_{th}:

$$V_{th} = V_{FB} + \gamma\sqrt{2\phi_F} + 2\phi_F$$

According to the long-channel equation, V_{th} is independent of W/L. But, At small W/L values When the channel width is very small, the threshold voltage Vth decreases significantly. This phenomenon is known as the Inverse Narrow Width Effect, which matches graph trend.

- For V_{OV}:

$$V_{ov} = \sqrt{\frac{2I_D}{\mu_n c_{ox}\frac{W}{L}}}$$

According to the long-channel equation, V_{ov} decreases as W/L increases, which matches graph trend.

- For V_{Dsat}:

$$V_{Dsat} = V_{gs} - V_{ov} = \sqrt{\frac{2I_D}{\mu_n c_{ox}\frac{W}{L}}}$$

According to the long-channel equation, V_{ov} decreases as W/L increases, which matches graph trend.

- For $gm*r_0$:

$$gm * r_0 = r_0 * \sqrt{2\mu_n c_{ox} \frac{W}{L} I_D}$$

According to the long-channel equation, $gm*r_0$ increases as W/L increases, which matches graph trend, but in the low V_{th} MOSFET the equation doesn't match graph.

3. Comparison Between N_LV_12_HS_L130E and N_12_HS_L130E:
   - Advantage of N_LV_12_HS_L130E:

     Operates at a lower voltage since its threshold voltage is lower, it can turn on with a lower gate voltage.
   - Disadvantage of N_LV_12_HS_L130E:

     Higher leakage current due to the lower V_{th}, leading to unwanted power consumption and reduced circuit efficiency.

   N_12_HS_L130E is the better choice because It has a higher V_{th} reduces noise and It has a smaller channel-length modulation effect, leading to a higher $gm*r_0$ product, which increases the intrinsic gain.

Task #2:

1. Parameter assumptions:

RNPPO_MML130E (R) =2KΩ: to ensure proper biasing the resistance value R was chosen as 2kΩ not to set the reference current directly, but rather to assist in stabilizing the circuit operation and ensuring proper biasing conditions. The current source used to generate I_{ref} provides a fixed and stable current independent of R. However, the chosen resistance value ensures that voltage drops and bias points across certain nodes remain within practical and safe limits. A higher resistance might lead to slower startup behavior or higher node impedance, while a lower resistance might lead to unnecessary power consumption or disturb the designed biasing conditions. Therefore, a moderate value of 2kΩ was chosen to balance these trade-offs.

L = 4µm: we chose this value –which is 33 times the minimum length – for multiple reasons

- **Reducing channel length modulation**: a higher value of L will reduce the channel length modulation which will lead to more accurate mirroring ratio independent on the values of Vds
- **Increasing output resistance**: the output resistance in our circuit depends mainly on the value of **ro** which increase by increasing the **L**
- **Lowering the value of Vcomp:** with longer **L** values the required drain voltage to make the transistors in saturation region become less

W = 80µm (for M3 and M1 and twice for M2 and M4):

- **Improving Rout:** the aspect ratio in those transistors is 20 and as known gm α W/L and the output resistance depend on gm
- **Ensure the needed current ratio:** from project spics we needed Iout = 2Iref and

$$\frac{\boldsymbol{Iout}}{\boldsymbol{Iref}} = \frac{(\frac{\boldsymbol{W}}{\boldsymbol{L}})_2}{(\frac{\boldsymbol{W}}{\boldsymbol{L}})_1}$$

so, by maintaining the ratio of 2:1 will manage to satisfy the current goal

2. Hand analysis :

- Since $V_{gs4} = V_{gs3}$ (by neglecting the body effect)

  So, the current mirroring only depends on K value $(\frac{W}{L})$

  $\frac{\text{Iout}}{\text{Iref}} = \frac{(\frac{\text{W}}{\text{L}})_2}{(\frac{\text{W}}{\text{L}})_1} = \frac{40}{20} = \frac{\text{Iout}}{100\mu}$

  $\therefore \text{Iout} = 200\boldsymbol{\mu}\text{A}$

- Let $(\frac{\text{W}}{\text{L}})_1 = (\frac{\text{W}}{\text{L}})_3$ & $(\frac{\text{W}}{\text{L}})_2 = (\frac{\text{W}}{\text{L}})_4$

  Then $V_{gs1} = V_{gs3}$ & $V_{gs4} = V_{gs2}$

  And we neglected the body effect by connecting the bulk to the source

  Minimum $V_{comp} = V_{ov2} + V_{ov4}$ & $V_{ov2} = V_{ov4}$

  Then $V_{comp} = 2V_{ov2}$

  And since $V_{comp} \leq 350m$v

  $\therefore \boldsymbol{V_{ov2}}$ **maximum = 175mv** (1)

- For M3 to remain in sat

  $V_{D3} \geq V_{G3} - V_{TH} \rightarrow V_{G1} \geq V_{G3} - V_{TH} \rightarrow V_{TH} \geq V_{G3} - V_{G1}$

  $Iref * R = V_{G3} - V_{G1} \rightarrow V_{TH} \geq Iref * R$

  $\therefore \text{R} \leq \frac{V_{TH}}{Iref}$

- For M2 to remain in sat

  $Iref * R = V_{GS4} + V_{GS2} - V_{GS2} = V_{DS2}$

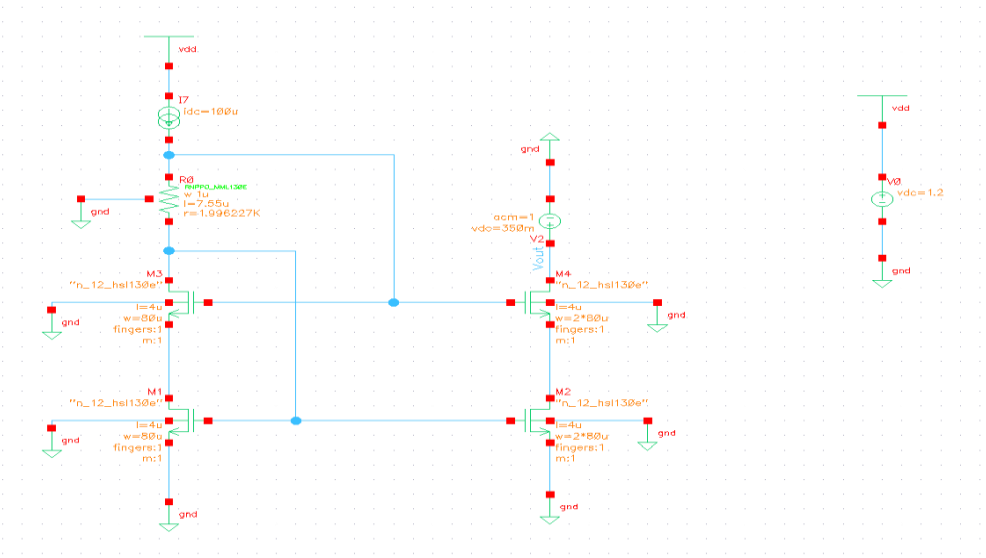
  $\therefore \text{R} \geq \frac{V_{ov2}}{Iref}$

- And from (1) gm = $\frac{2I_{ds}}{V_{ov}}$

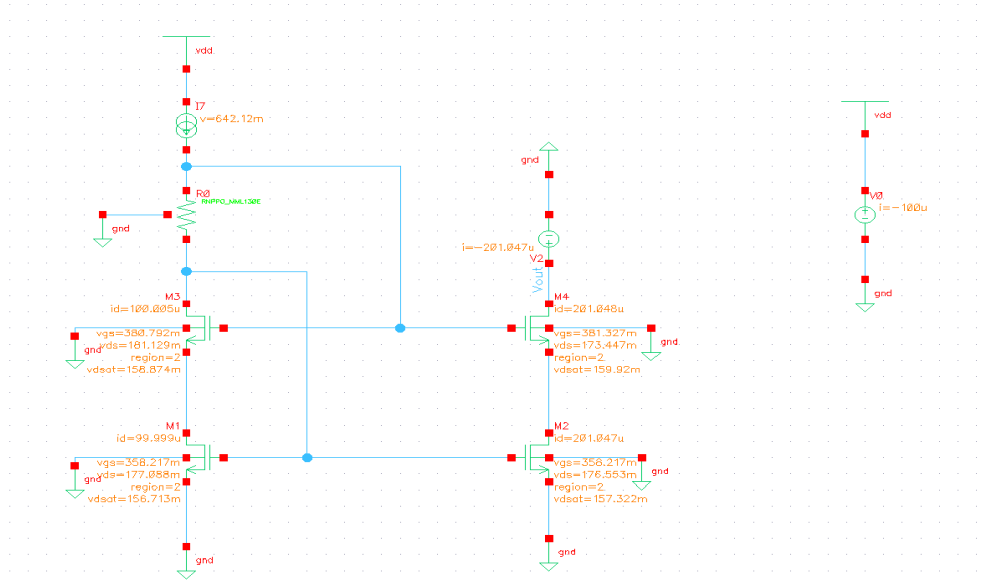
  $\therefore \text{gm}_2$ minimum $\sim 2.28mS$

3. Results :

- **Circuit components and parameters:** schematic diagram and components values

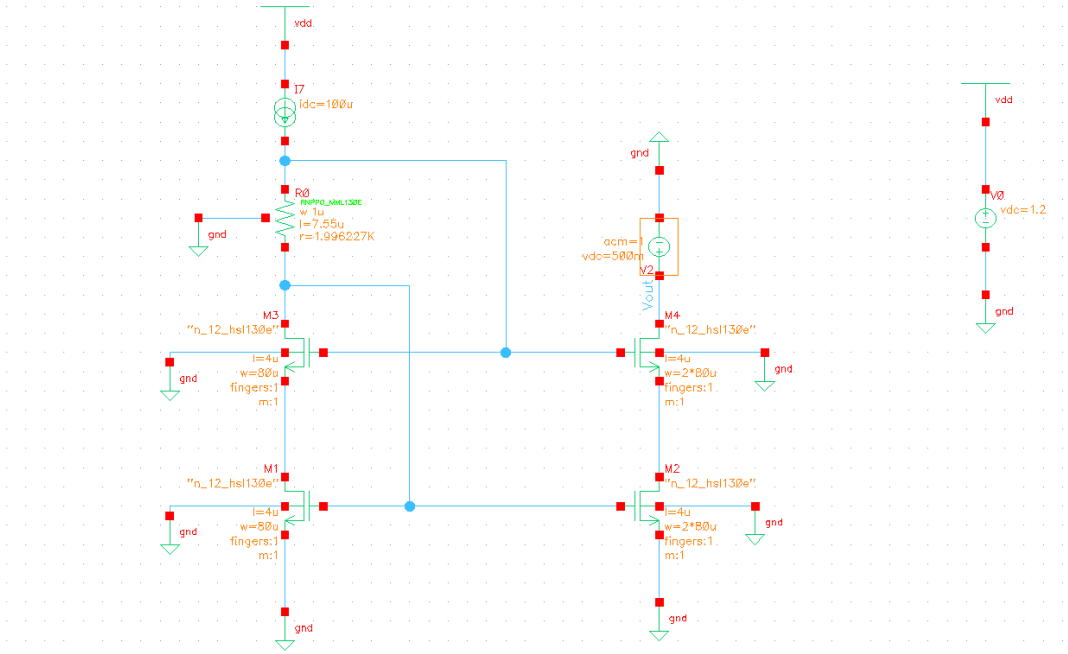


- **DC operating point ensuring Vout:** we used the circuit above and ran a DC analysis with Vout = 350mV and here is the result



as shown all transistors are in saturation region (region = 2) with Vout = 350mV which mean that the Vcomp is lower than 350mV achieving the first requirement

- **Iout and Rout:** for the Iout and Rout specifications we changed the value of the vout to become 500mV and here is the new circuit and putting AC magnitude of 1 V:

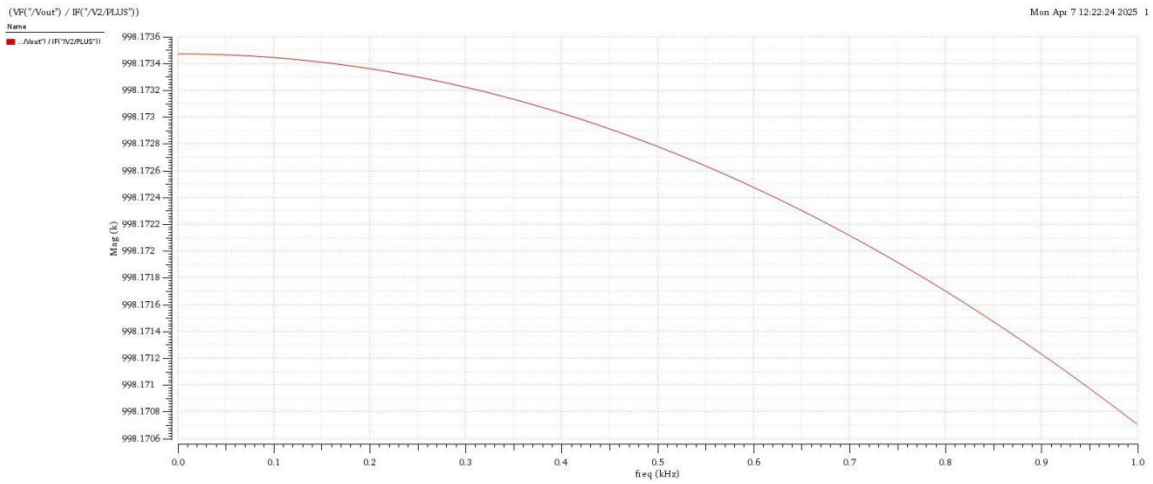


After that we ran a DC analysis to get the value of Iout and here is the result was

1	IDC("/M4/D")	201.559u

for measuring the error $\left|\frac{Iout-Ireq}{Ireq}\right| * 100 = \left|\frac{201.559-200}{200}\right| * 100 = 0.77\%$ which is lower that 1% as required achieving the second requirement

and for Rout we ran AC analysis and here is the results and we are interested in frequencies near DC:



as shown the Rout is equal to 998.1735KΩ at DC which is higher than 500kΩ achieving the third requirement

- Estimating of mirror area:

  Resistor area: $L_R * W_r = 7.55\mu * 1\mu = 7.55\mu m^2$
  M1 & M3 area: $2 * [L1 * W1] = 2 * [4\mu * 80\mu] = 640\mu m^2$
  M2 & M4 area: $2 * [L2 * W2] = 2 * [4\mu * 160\mu] = 1280\mu m^2$

  the total area: $7.55 + 640 + 1280 = 1927.55\mu m^2$

- Spec scarified to have reasonable area:

  1) **Error (I_out ≤ 1% @ Vout = 500mV)**
     Sacrifice: Increase the error margin slightly (e.g., allowing 2% or 3% instead of 1%).
     Pros: Reducing the precision can reduce the required sizes of transistors and resistors, resulting in a smaller area.
     Cons: The accuracy of the current mirror will degrade, and the circuit may not provide the exact output current as specified.

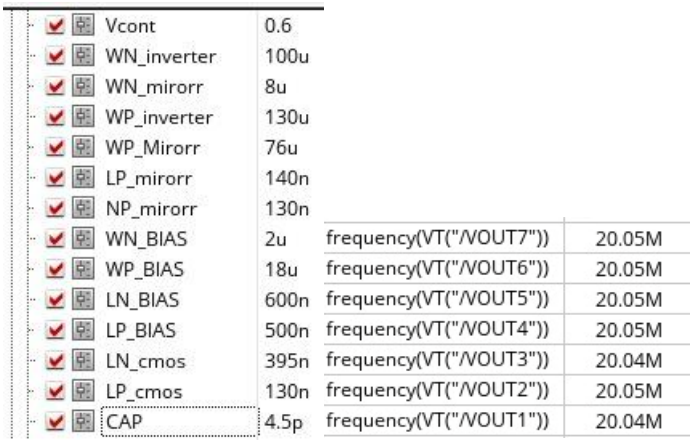
  2) **V_comp (≤ 350mV)**
     Sacrifice: Relax the V_comp requirement to 400mV or even 450mV.
     Pros: A less stringent requirement on the voltage at which all devices are in saturation, reducing the complexity and size of transistors.
     Cons: The devices may enter saturation later, potentially affecting the performance, especially at lower output voltages.

  3) **Output Resistance (R_out ≥ 500kΩ @ Vout = 500mV)**
     Sacrifice: Reducethe required output resistance to 400kΩ or 300kΩ.
     Pros: By lowering the output resistance requirement, you can use smaller transistors or fewer of them, thus reducing the overall area.
     Cons: A decrease in output resistance means the current mirror will have a less ideal current sourcing capability, leading to potential deviations in the current delivered to the load

Task #3:

1. Explain why this is called a Voltage Controlled Oscillator (VCO):
   - This circuit is called Voltage Controlled Oscillator (VCO) because input voltage (V_{cont}) controls the Oscillation frequency.
   - The Instantaneous Oscillation frequency is determined in terms of the applied input Voltage as V_{cont} controls in the value of current in the circuit which is charge the gate capacitance of the inverters Where the faster the charging and discharging, the lower delay time, the higher the Oscillation frequency.

2. Determine the dimensions of all the transistors (Use 1.2V devices N_12_HSL130E or P_12_HSL130E) to generate an output frequency of 20MHz using 7-stages with Vcont= VDD/2:
   - Dimensions of MOSFETs:

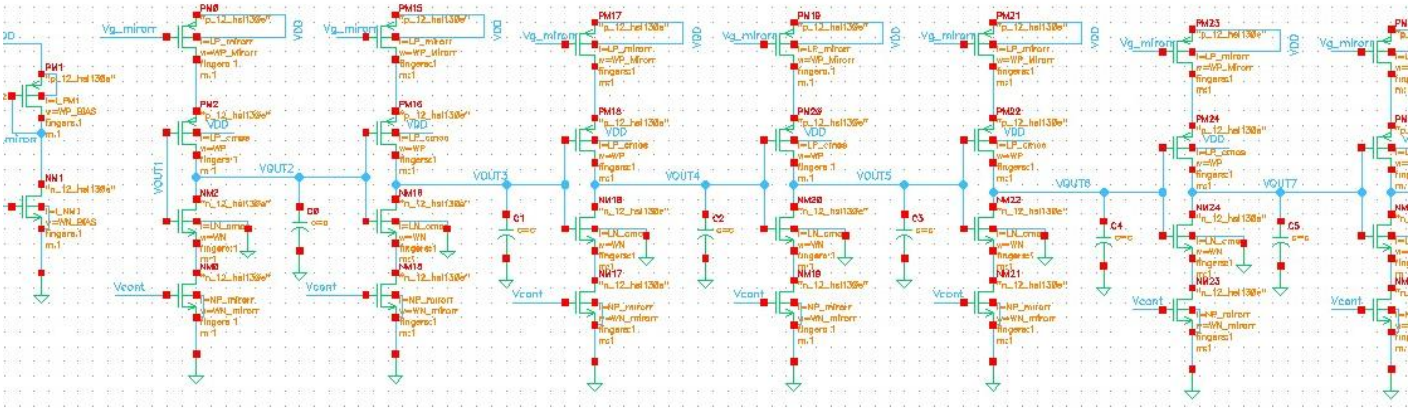


Vcont	0.6		
WN_inverter	100u		
WN_mirorr	8u		
WP_inverter	130u		
WP_Mirorr	76u		
LP_mirorr	140n		
NP_mirorr	130n		
WN_BIAS	2u	frequency(VT("/VOUT7"))	20.05M
WP_BIAS	18u	frequency(VT("/VOUT6"))	20.05M
LN_BIAS	600n	frequency(VT("/VOUT5"))	20.05M
LP_BIAS	500n	frequency(VT("/VOUT4"))	20.05M
LN_cmos	395n	frequency(VT("/VOUT3"))	20.04M
LP_cmos	130n	frequency(VT("/VOUT2"))	20.05M
CAP	4.5p	frequency(VT("/VOUT1"))	20.04M

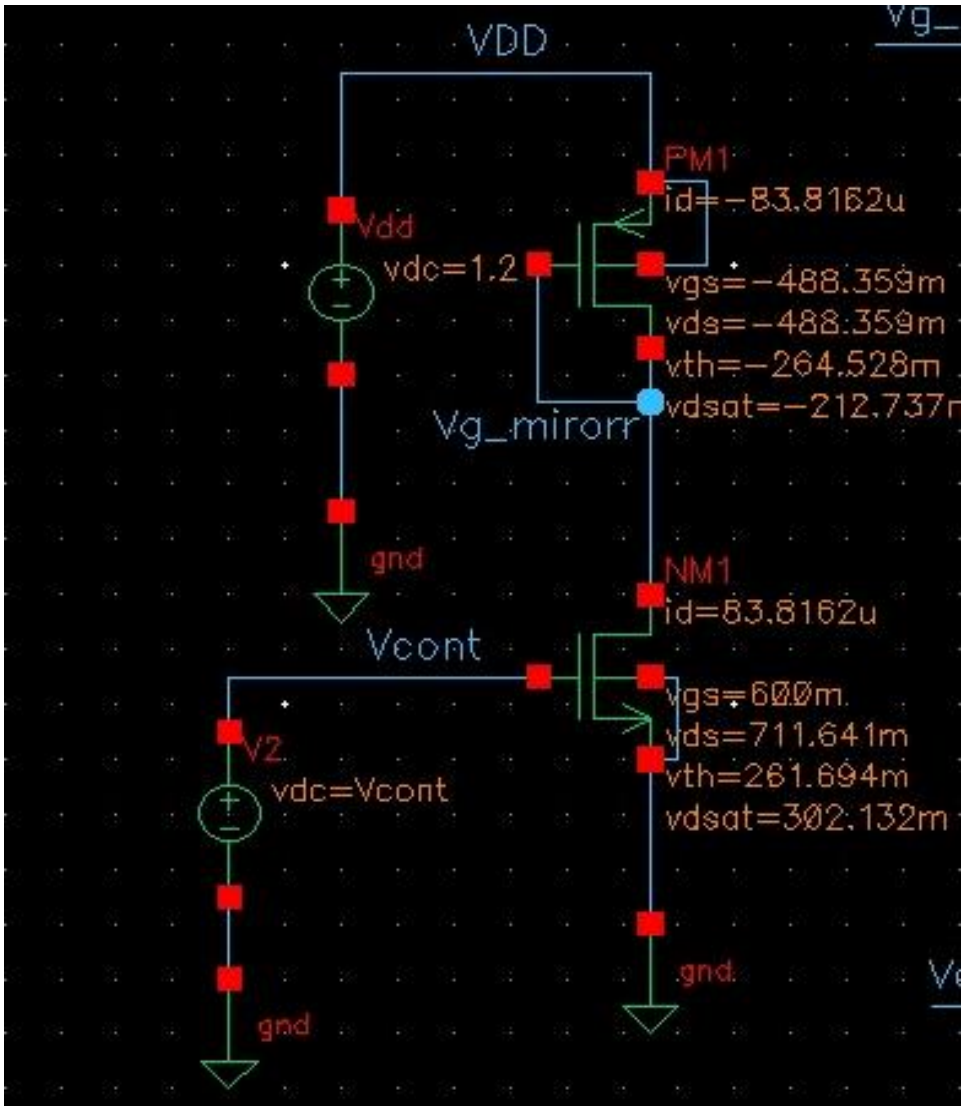
this dimensions make our PMOS and CMOS in the sat region and make our oscillator with the required frequency 20MHZ

3. Requirements:

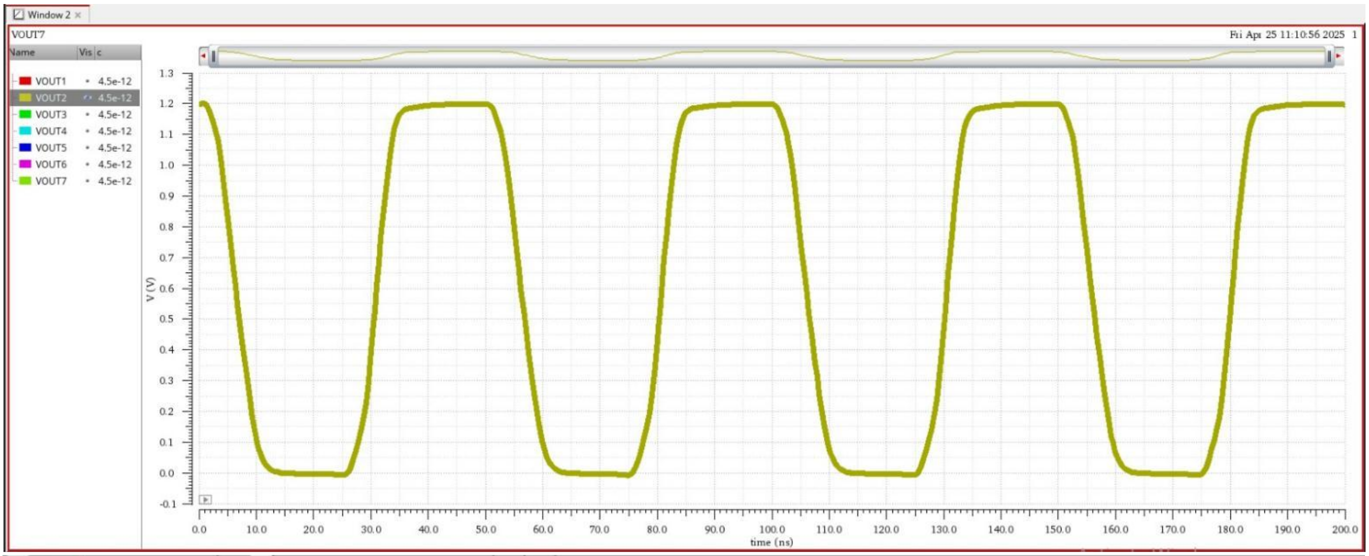
- Schematic diagram showing dimensions of all transistors:

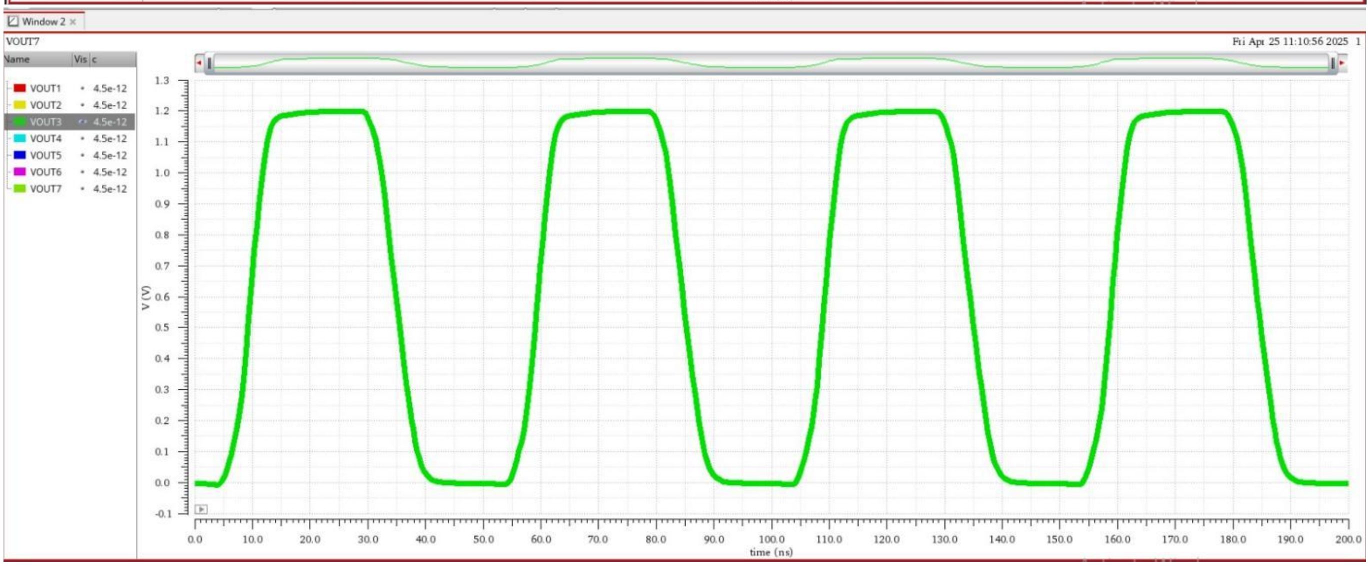


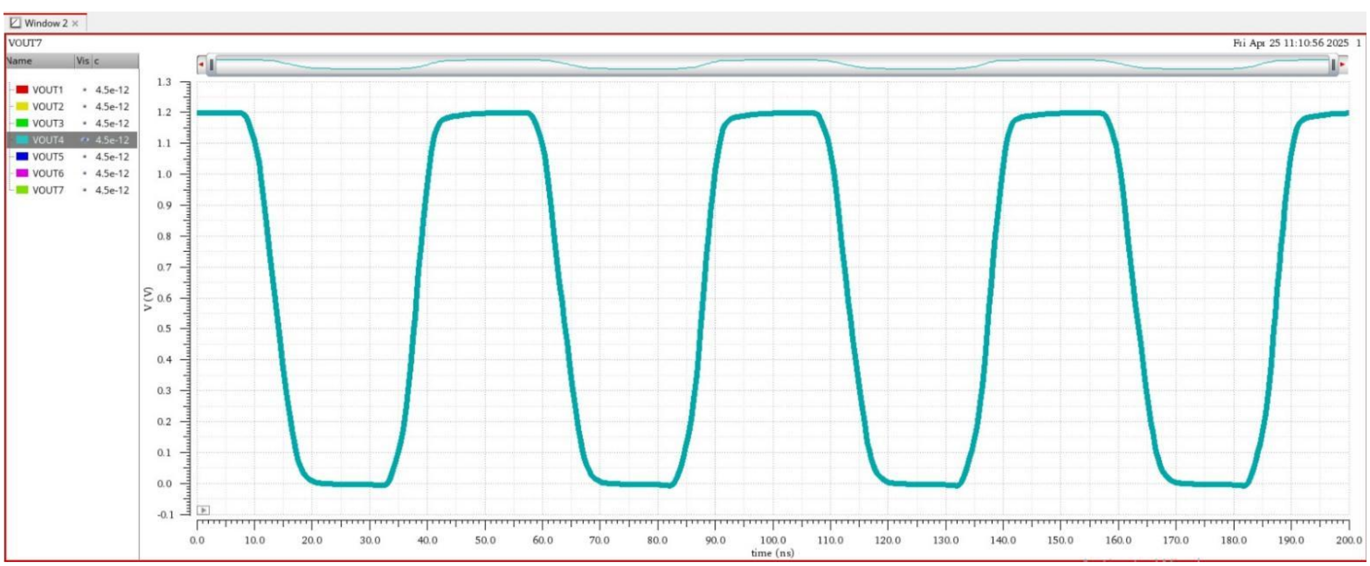
- First stage Schematic diagram showing dimensions transistors and bias current

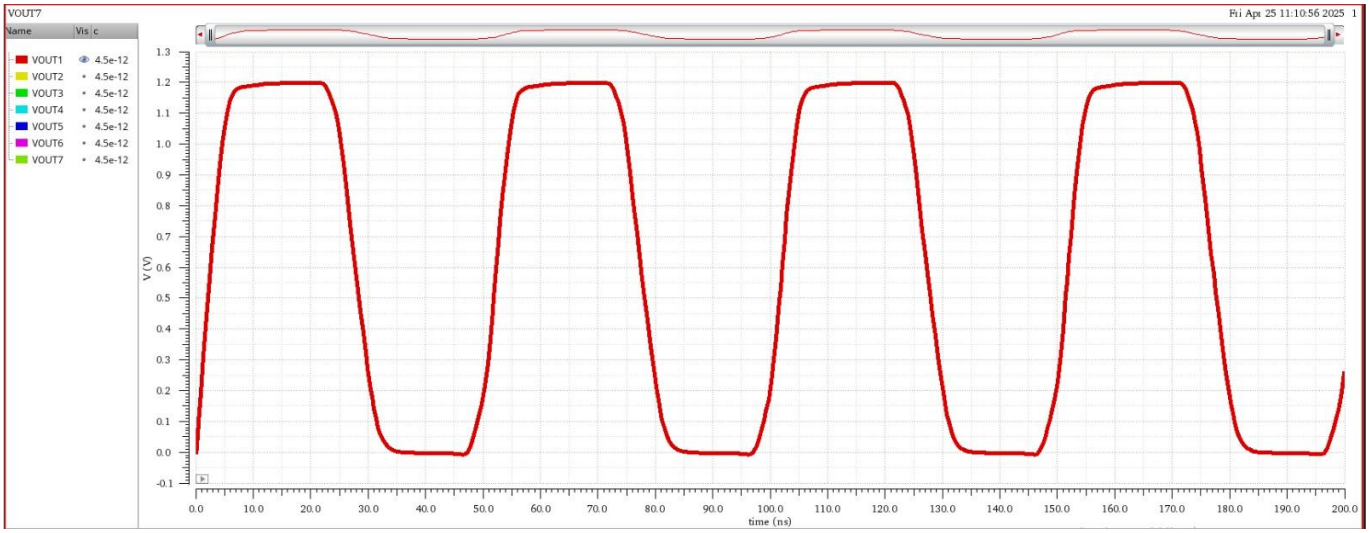


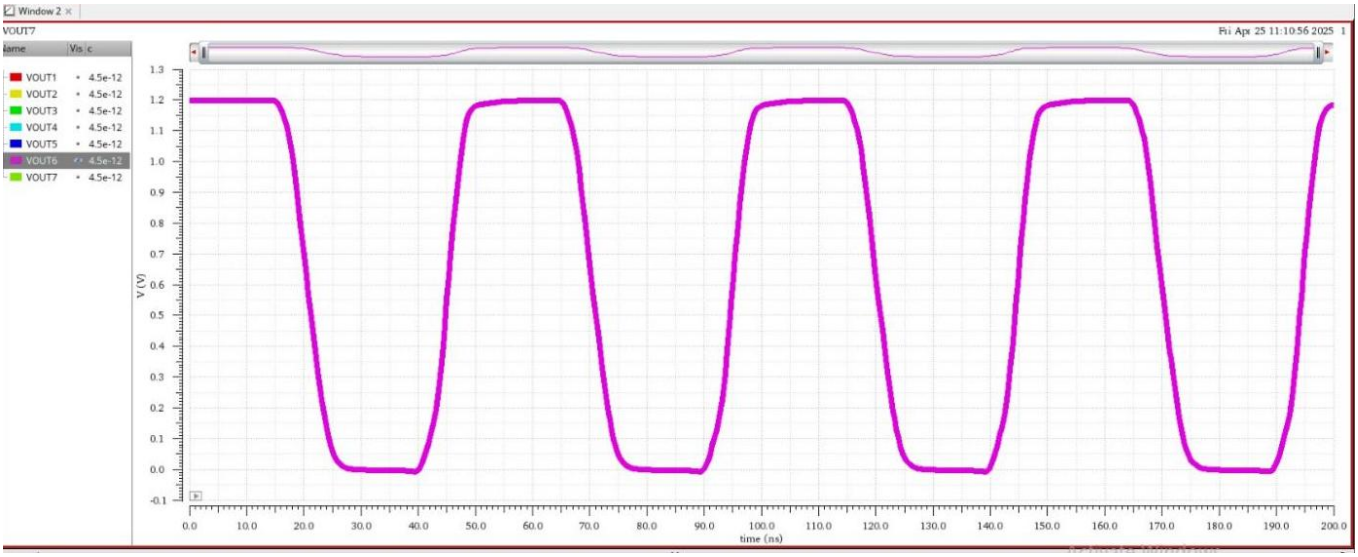
- transient waveforms at all inverter outputs showing the output frequency:

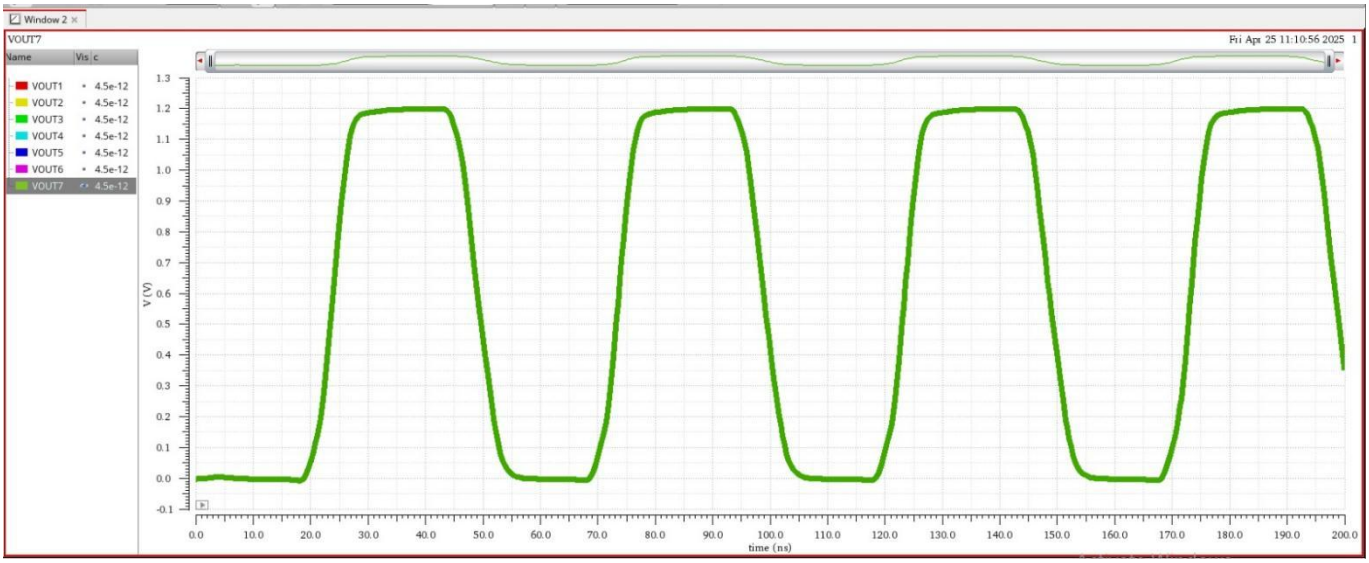


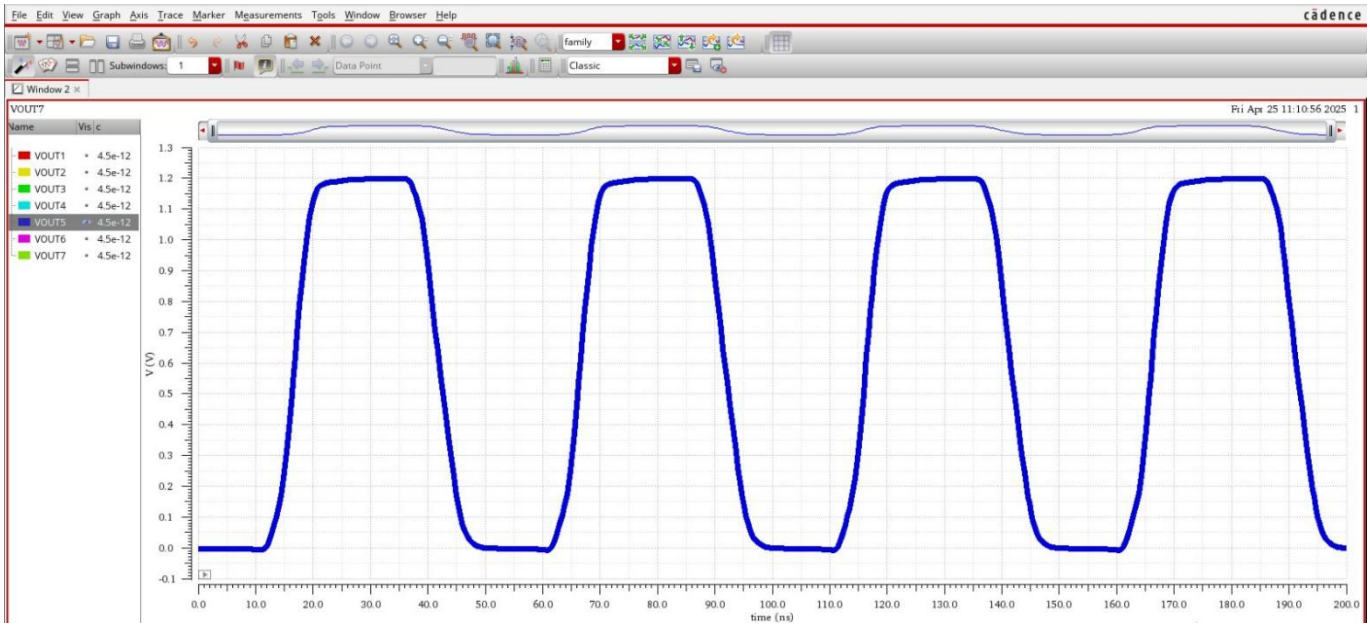




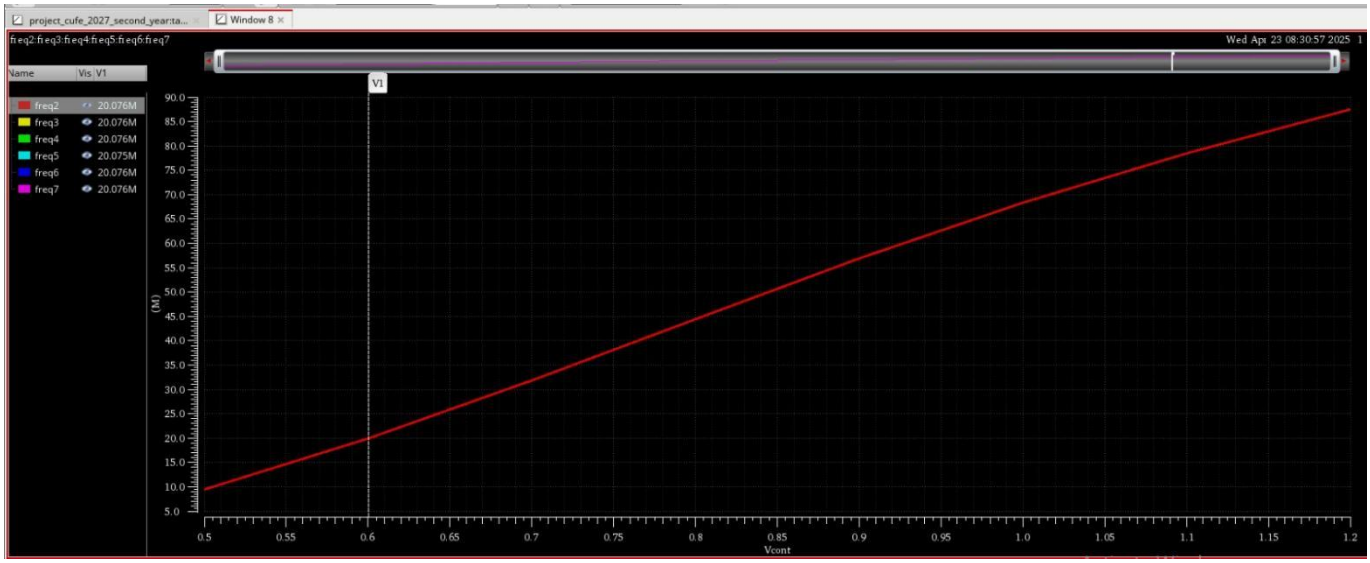

VOUT7
Fri Apr 25 11:10:56 2025 1
Name
Vis
c
VOUT1 4.5e-12
VOUT2 4.5e-12
VOUT3 4.5e-12
VOUT4 4.5e-12
VOUT5 4.5e-12
VOUT6 4.5e-12
VOUT7 4.5e-12
V (V)
time (ns)


Window 2
VOUT7
Fri Apr 25 11:10:56 2025 1
VOUT1 4.5e-12
VOUT2 4.5e-12
VOUT3 4.5e-12
VOUT4 4.5e-12
VOUT5 4.5e-12
VOUT6 4.5e-12
VOUT7 4.5e-12
V (V)
time (ns)


Window 2
VOUT7
Fri Apr 25 11:10:56 2025 1
VOUT1 4.5e-12
VOUT2 4.5e-12
VOUT3 4.5e-12
VOUT4 4.5e-12
VOUT5 4.5e-12
VOUT6 4.5e-12
VOUT7 4.5e-12
V (V)
time (ns)

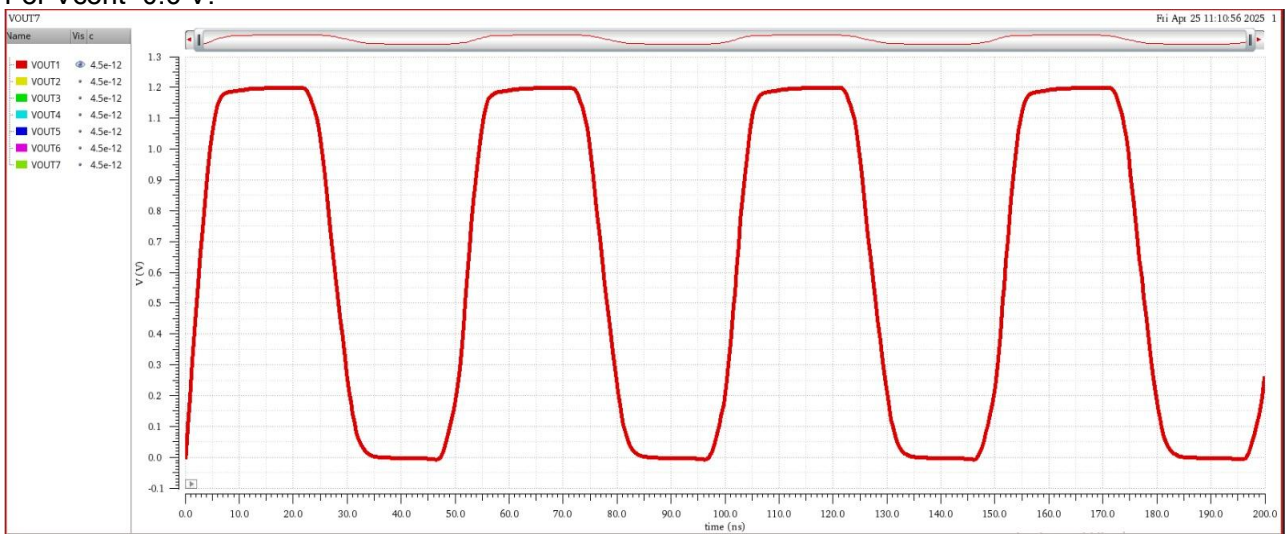


- Vary V_{cont} from 0 to VDD and record the output frequency versus V_{cont} in steps of 0.1V.

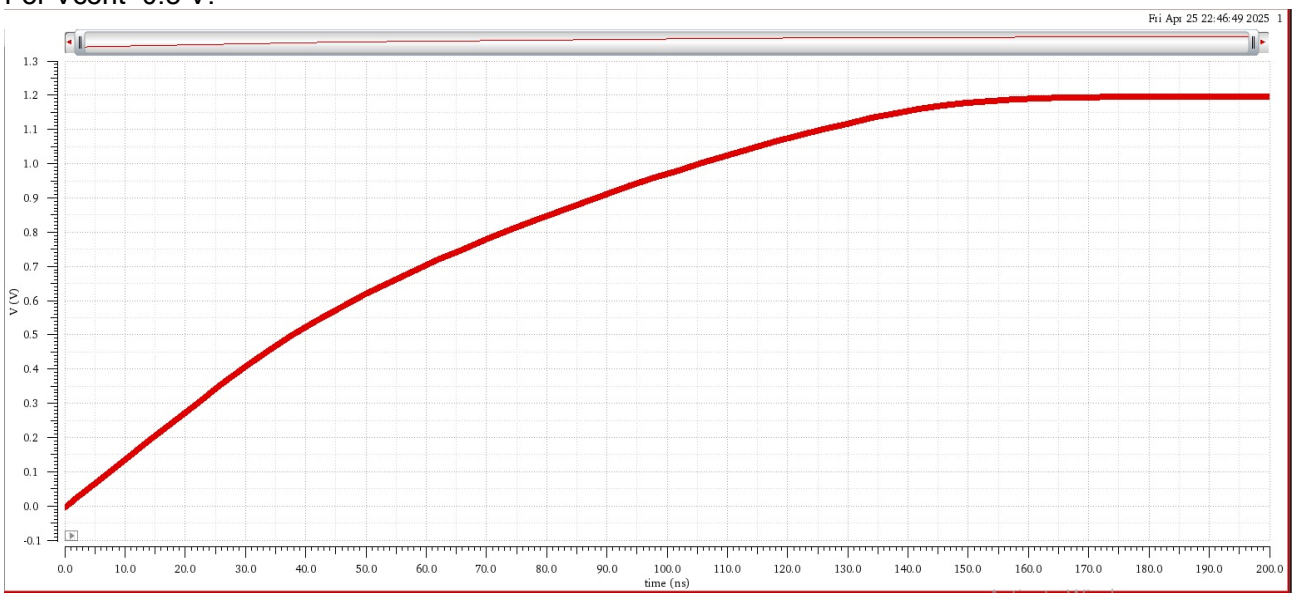


- Plot the oscillator output for 3 different steps:

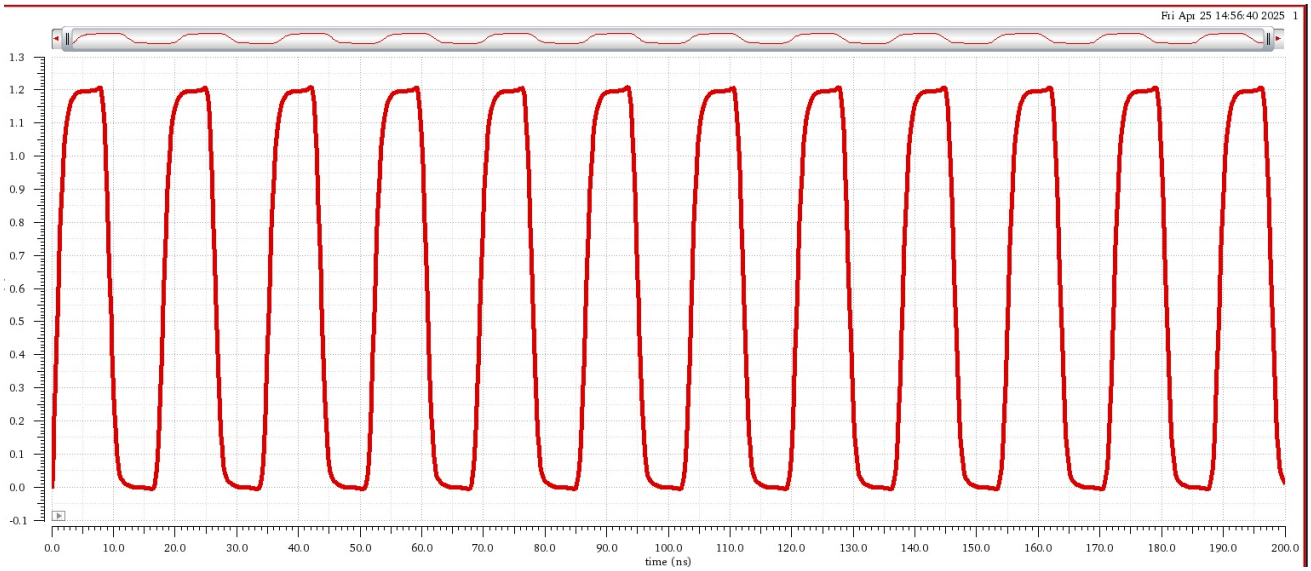
For Vcont=0.6 V:



For Vcont=0.3 V:



For Vcont=1 V:



4. Observation:

when V_{cont} increases current is also increases then delay time will become lower than the oscillation frequency get higher. the maximum value of the oscillation frequency is become true at $V_{cont} = V_{dd}$ and when V_{cont} lower than Vth the Oscillation frequency = 0 because there is no current in the circuit. So, as we said above V_{cont} controls the oscillation frequency in this circuit and with this methodology we can get wide range of oscillation frequencies and we can get higher Oscillation frequency by reducing the number of stages the delay time is get lower also, but in this case the Gain of the Oscillator becomes lower also.