Project (Deadline: Saturday May 3rd, 2025)

For the 3 tasks, use the PDK of a UMC 0.13µm technology:

Task #1 :

For an NMOS with Drain and Gate connected to $V_{DD} = 1.2V$ and Source connected to a current source $I_{REF} = 200\mu A$ to GND and Bulk connected to GND. Sweep W from W=L to W=100L.

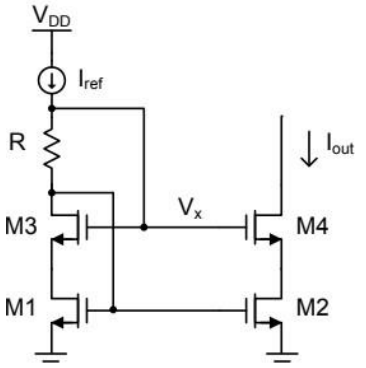
1. For the parameters:
    - V_{th}
    - V_{ov}
    - V_{DSAT}
    - $g_m r_o$

    Plot each of these parameters vs W/L at $L=L_{min}$, $L=2L_{min}$, $L=4L_{min}$, and $L=8L_{min}$ for the following devices:
    - **N_12_HS_L130E** (high-speed NMOS)
    - **N_LV_12_HS_L130E** (Low-Vth high-speed NMOS)

    (For each parameter, insert 2 figures next to each other, each having the 4 parametric curves for one of the 2 devices)
2. **Mention** the long-channel equation for V_{th}, V_{ov}, &$g_m r_o$. Is the trend of the simulations similar to the equations?
3. **Mention one** advantage and **one** disadvantage for **N_LV_12_HS_L130E** compared to **N_12_HS_L130E**. What do you recommend to be used in a **high-gain amplifier**?

Task #2 :

Use the NMOS core high speed HS transistor (**N_12_HS_L130E**) and the poly resistor (**RNPPO_MML130E**) to design an accurate high-swing current mirror (according to the architecture shown) operating at $V_{DD} = 1.2V$ with the following specifications:



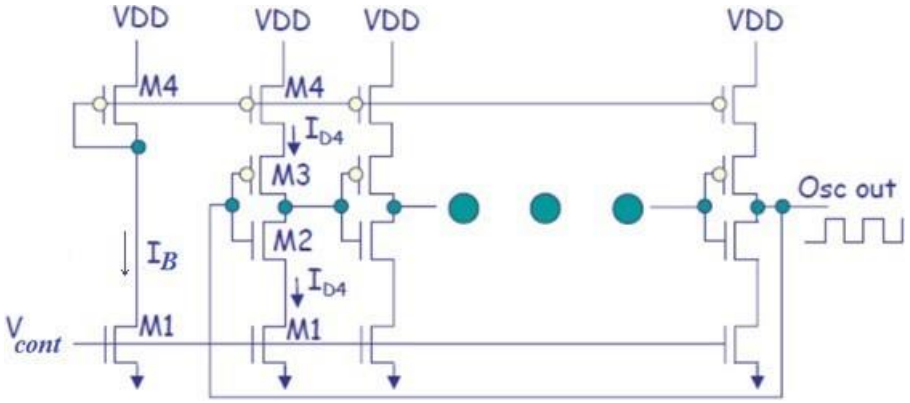
- $I_{out} = 2I_{REF} = 200\mu A$, with error $< 1\%$ @V_{out}=500mV
- $V_{comp} \leq 350mV$ (defined as the minimum output voltage required for all devices to operate in saturation)
- $R_{out} \geq 500\text{k}\Omega$ @ $V_{out} = 500mV$

The documentation of your design must include the following:

1. Schematic diagram with dimensions and component values annotated.
2. Schematic diagram with DC operating point annotated at V_{out}=350mV to verify the V_{comp} specification.
3. Simulation results to verify I_{out} and R_{out} specifications
4. An estimate of this mirror's area.
5. If the area you ended up with is too large and you need to sacrifice one of the specs to have reasonable area, suggest a modification and comment on what you will gain and lose from it.

Task #3:

Design the CMOS ring oscillator shown with $V_{DD} = 1.2V$. The unit cell (stage) consists of a CMOS inverter (M_2 and M_3), an NMOS current source (M_1), and a PMOS current source (M_4). This is called a "Voltage Controlled Oscillator (VCO)".



- Explain why this is called a Voltage Controlled Oscillator (VCO).
- Determine the dimensions of all the transistors (Use 1.2V devices N_12_HSL130E or P_12_HSL130E) to generate an output frequency of **20MHz** using **7-stages** with $V_{cont} = V_{DD}/2$.

The documentation of your design must include the following:

1- Schematic diagram showing dimensions of all transistors and bias current (I_B)

2- Simulate the ring oscillator and plot the transient waveforms at all inverter outputs showing the output frequency (you might need to add an initial condition to start the oscillation).

3- Vary V_{cont} from 0 to V_{DD} and record the output frequency versus V_{cont} in steps of 0.1V. Plot the oscillator output for 3 different steps.

4- Provide your observations and conclusions.

Assessment:

- Maximum number of students per group is **5**
- You are required to deliver a **pdf report** that clearly describes your work, including all the required items.
- Report size should not exceed 20 pages.
- Late delivery will be penalized
- Copied reports will get a direct **ZERO** grade