IT COOKBOOK

디지털논리회로

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(Problem Solutions of Chapter 7)

한빛미디어 Hanbit Media, Inc.

1. 반감산기와 전감산기를 설계

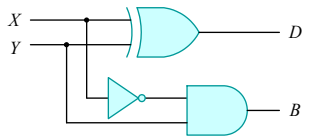
① 반감산기

두 수의 차(difference) : D, 자리빌림(barrow) : B

입력		출력	
X	Y	D	B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

반감산기 진리표

진리표에서 출력을 부울함수로 표시하고, 이를 논리회로로 표시하면 다음과 같다.



$$D = \overline{X}Y + X\overline{Y} = X \oplus Y$$
$$B = \overline{X}Y$$

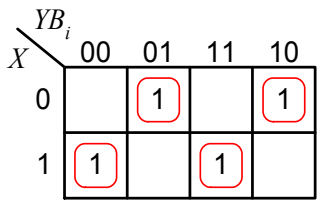
② 전감산기

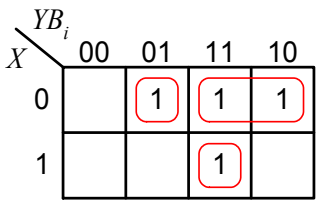
전감산기는 자리빌림(barrow) 입력을 처리하기 위해 B_i를 추가.

입력			출력	
X	Y	B_i	D	B_o
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

전감산기 진리표

카르노 맵을 이용하여 출력을 간소화하면

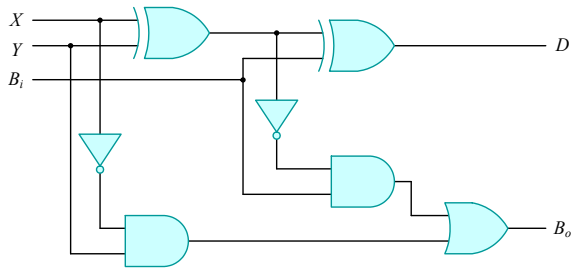




$$D = \overline{X}\overline{Y}B_i + \overline{X}Y\overline{B_i} + X\overline{Y}\overline{B_i} + XYB_i$$
$$= X \oplus Y \oplus B_i$$

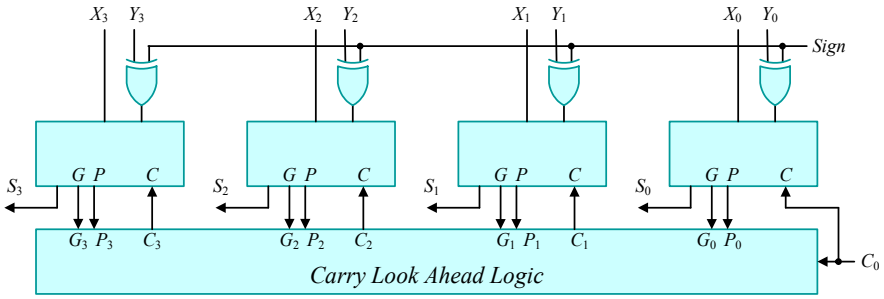
$$B_o = \overline{X}Y + B_i\overline{(X \oplus Y)}$$

이 부울함수를 논리회로로 표시하면

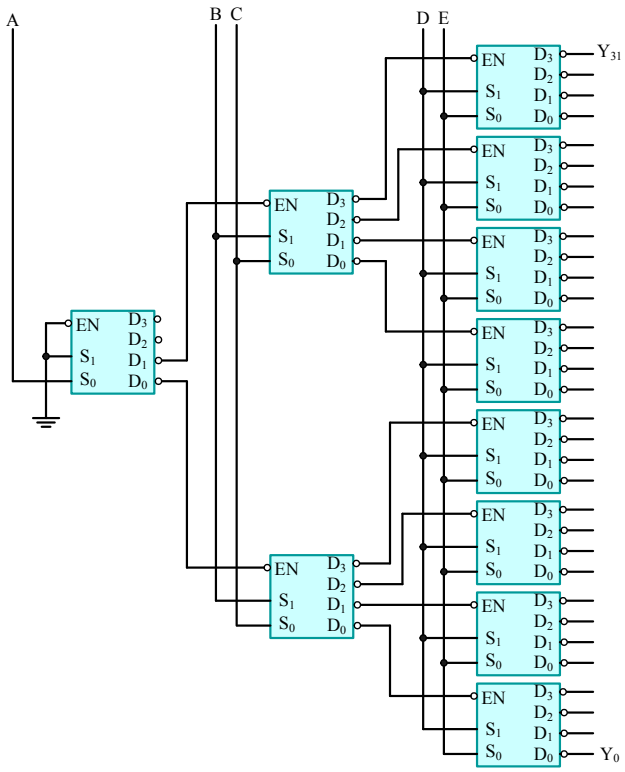


2. 뺄셈이 가능한 캐리예측 가산기 설계

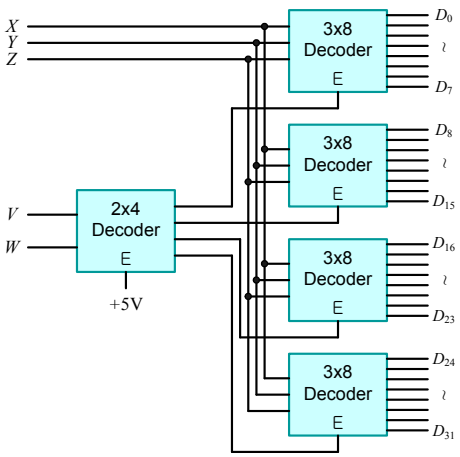
Sign=0이면, 가산기. Sign=1이면, 뺄셈기로 동작.



3. Enable을 가진 2×4 디코더를 이용하여 5×32 디코더를 설계



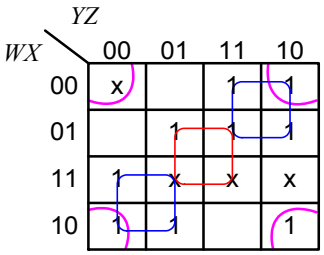
4. 5×32 디코더 회로설계



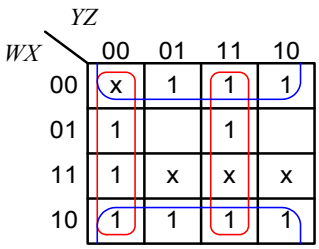
5. 특수한 8-segment LED 회로 설계

입력변수 : W, X, Y, Z 출력변수 : $a \sim h$

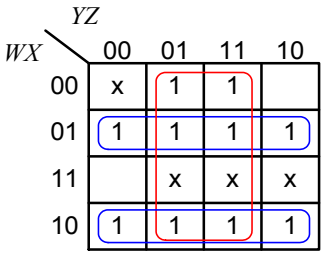
10진수	W	X	Y	Z	a	b	c	d	e	f	g	h
0	0	0	0	0	x	x	x	x	x	x	x	x
1	0	0	0	1	0	1	1	0	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1	0
3	0	0	1	1	1	1	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0	0	1	1	0
5	0	1	0	1	1	0	1	1	0	1	1	0
6	0	1	1	0	1	0	1	1	1	1	1	0
7	0	1	1	1	1	1	1	0	0	1	0	0
8	1	0	0	0	1	1	1	1	1	1	1	0
9	1	0	0	1	1	1	1	1	0	1	1	0
10	1	0	1	0	1	1	1	1	1	1	0	1
11	1	0	1	1	0	1	1	0	0	0	0	1
12	1	1	0	0	1	1	0	1	1	0	1	1
13	1	1	0	1	x	x	x	x	x	x	x	x
14	1	1	1	0	x	x	x	x	x	x	x	x
15	1	1	1	1	x	x	x	x	x	x	x	x



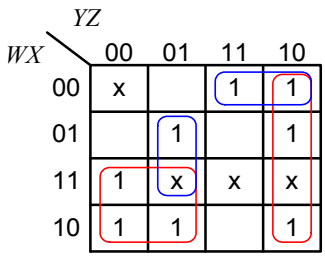
$a = \overline{X}\overline{Z} + W\overline{Y} + XZ + \overline{W}Y$
$= (W \oplus Y) + (X \odot Z)$



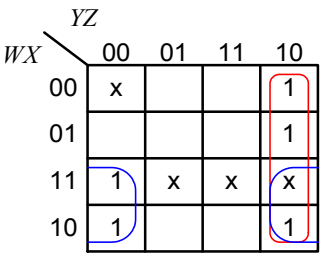
$b = \overline{X} + YZ + \overline{Y}\overline{Z}$
$= \overline{X} + (Y \odot Z)$



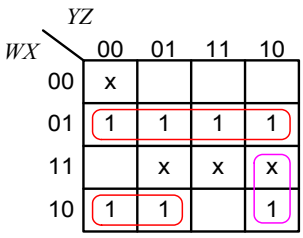
$c = Z + \overline{W}X + W\overline{X}$
$= Z + (W \oplus X)$



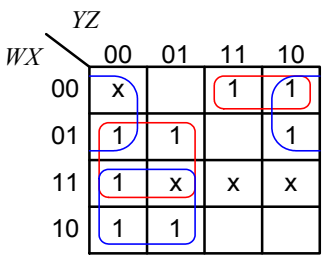
$d = W\overline{Y} + Y\overline{Z} + \overline{W}\overline{X}Y + X\overline{Y}Z$



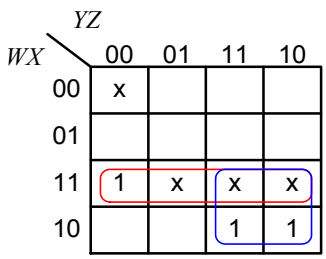
$e = W\overline{Z} + Y\overline{Z}$



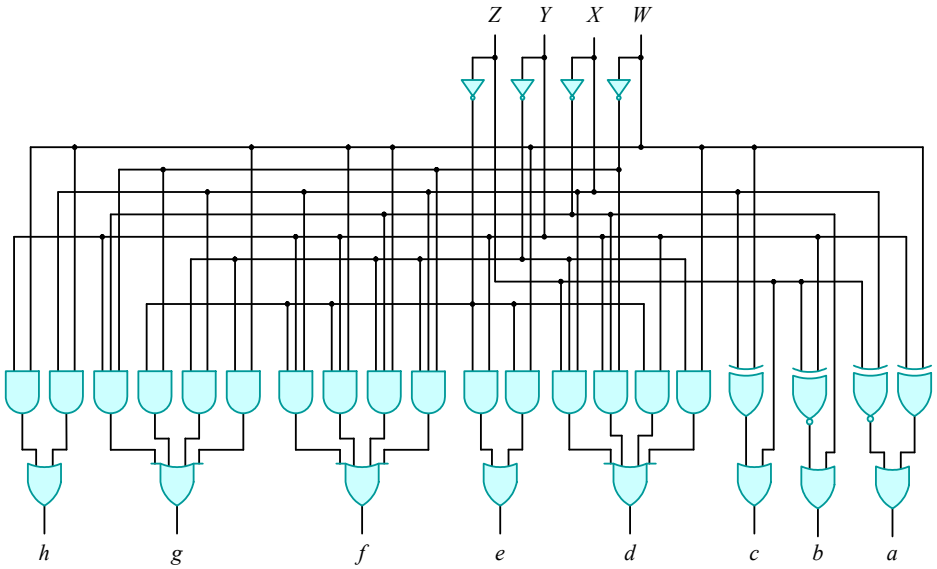
$f = \overline{W}X + W\overline{X}\overline{Y} + WY\overline{Z}$



$g = W\overline{Y} + X\overline{Y} + \overline{W}\overline{Z} + \overline{W}\overline{X}Y$



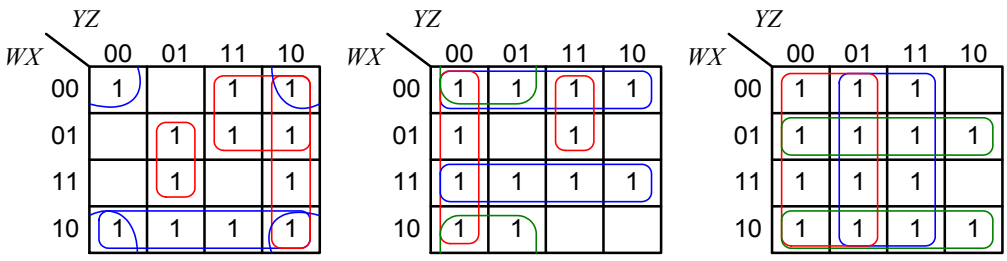
$h = WX + WY$



6. 특수한 8-segment LED 회로 설계

입력변수 : W, X, Y, Z 출력변수 : $a \sim h$

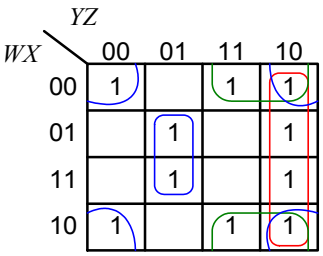
표시	W	X	Y	Z	a	b	c	d	e	f	g	h
0	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	0	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1	0
3	0	0	1	1	1	1	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0	0	1	1	0
5	0	1	0	1	1	0	1	1	0	1	1	0
6	0	1	1	0	1	0	1	1	1	1	1	0
7	0	1	1	1	1	1	1	0	0	0	0	0
−8	1	0	0	0	1	1	1	1	1	1	1	1
−7	1	0	0	1	1	1	1	0	0	0	0	1
−6	1	0	1	0	1	0	1	1	1	1	1	1
−5	1	0	1	1	1	0	1	1	0	1	1	1
−4	1	1	0	0	0	1	1	0	0	1	1	1
−3	1	1	0	1	1	1	1	1	0	0	1	1
−2	1	1	1	0	1	1	0	1	1	0	1	1
−1	1	1	1	1	0	1	1	0	0	0	0	1



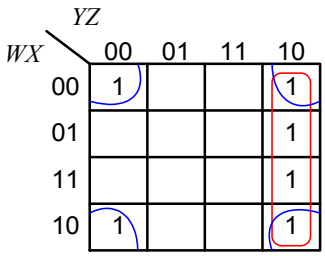
$a = \overline{W}Y + \overline{X}\overline{Z} + YZ + X\overline{Y}Z$

$b = WX + \overline{W}\overline{X} + \overline{X}\overline{Y} + \overline{Y}\overline{Z} + \overline{W}YZ$
$= (W \odot X) + \overline{X}\overline{Y} + \overline{Y}\overline{Z} + \overline{W}YZ$

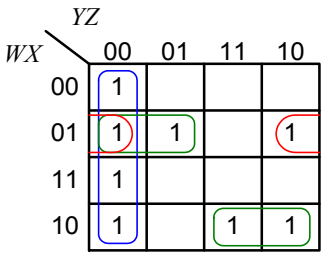
$c = \overline{Y} + Z + \overline{W}X + W\overline{X}$
$= \overline{Y} + Z + (W \oplus X)$



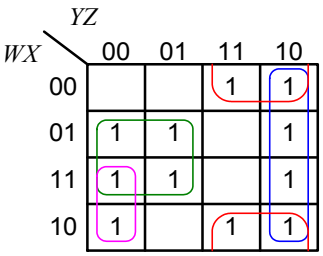
$d = \overline{X}Y + \overline{X}\overline{Z} + Y\overline{Z} + X\overline{Y}Z$



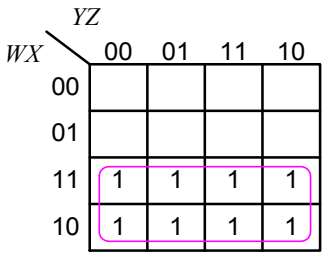
$e = \overline{X}\overline{Z} + Y\overline{Z}$



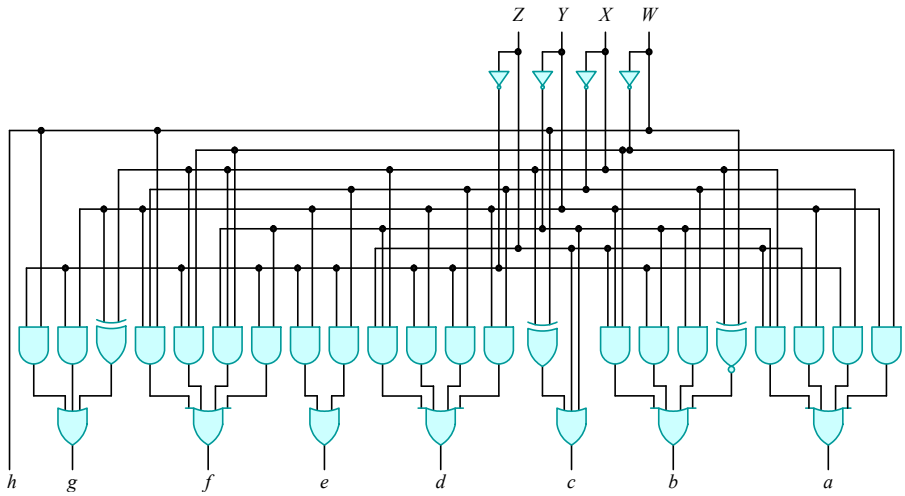
$f = \overline{Y}\overline{Z} + \overline{W}X\overline{Y} + \overline{W}\overline{X}\overline{Z} + W\overline{X}Y$



$g = X\overline{Y} + \overline{X}Y + Y\overline{Z} + W\overline{Z}$
$= (X \oplus Y) + Y\overline{Z} + W\overline{Z}$



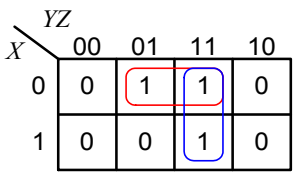
$h = W$



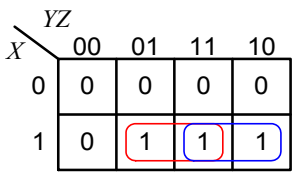
7. 특수한 8-segment LED 회로 설계

입력변수 : X, Y, Z 출력변수 : $a \sim h$

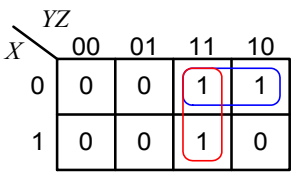
10진수	표시	X	Y	Z	a	b	c	d	e	f	g	h
0		0	0	0	0	0	0	0	0	0	0	0
1	↑	0	0	1	1	0	0	0	1	0	1	0
2	↓	0	1	0	0	0	1	0	1	0	1	0
3	↕	0	1	1	1	0	1	0	1	0	1	0
4	←	1	0	0	0	0	0	1	0	1	0	1
5	→	1	0	1	0	1	0	0	0	1	0	1
6	↔	1	1	0	0	1	0	1	0	1	0	1
7		1	1	1	1	1	1	1	1	1	1	1



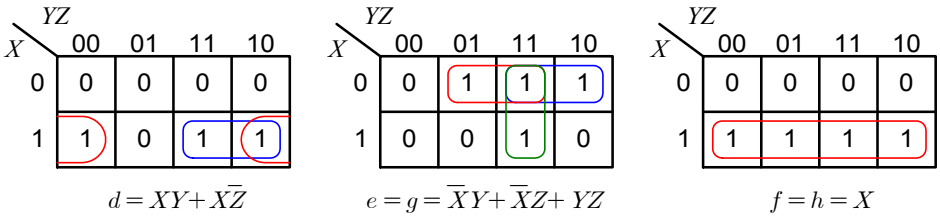
$a = \overline{X}Z + YZ$



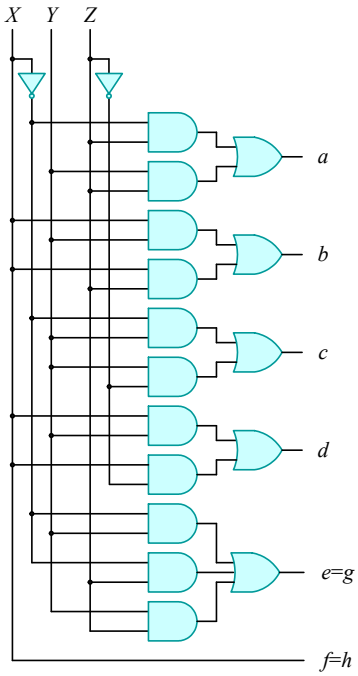
$b = XY + XZ$



$c = \overline{X}Y + YZ$

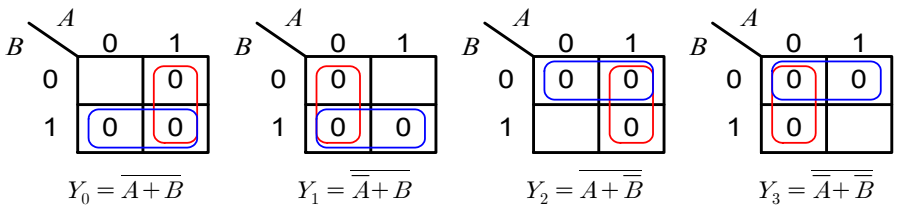


$d = XY + X\overline{Z}$ $e = g = \overline{X}Y + \overline{X}Z + YZ$ $f = h = X$

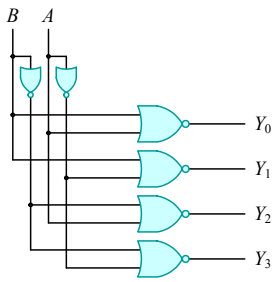


8. NOR 게이트만을 이용한 2×4 디코더 설계

입력		출력			
B	A	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0



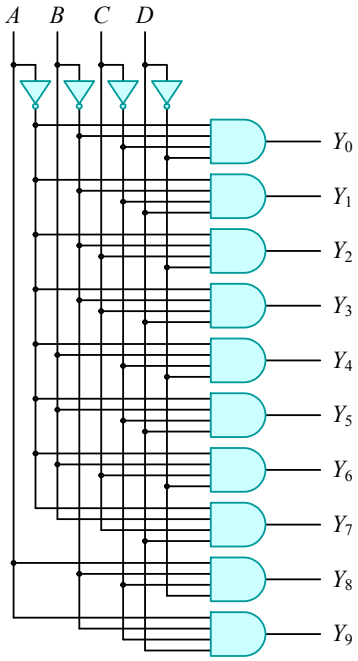
$Y_0 = \overline{A + B}$ $Y_1 = \overline{\overline{A} + B}$ $Y_2 = \overline{A + \overline{B}}$ $Y_3 = \overline{\overline{A} + \overline{B}}$



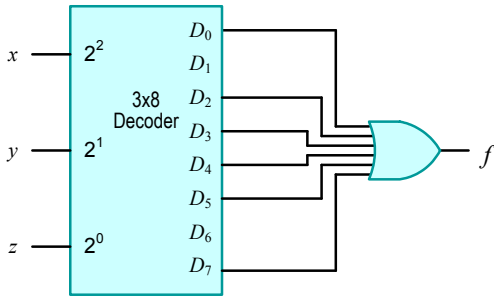
9. BCD-to-10 디코더 회로 설계

입력변수 : A, B, C, D 출력변수 : $Y_0 \sim Y_9$

10진수	A	B	C	D	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Y_9
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	0	0	0	0	0	0	1	0
2	0	0	1	0	0	0	0	0	0	0	0	1	0	0
3	0	0	1	1	0	0	0	0	0	0	1	0	0	0
4	0	1	0	0	0	0	0	0	0	1	0	0	0	0
5	0	1	0	1	0	0	0	0	1	0	0	0	0	0
6	0	1	1	0	0	0	0	1	0	0	0	0	0	0
7	0	1	1	1	0	0	1	0	0	0	0	0	0	0
8	1	0	0	0	0	1	0	0	0	0	0	0	0	0
9	1	0	0	1	1	0	0	0	0	0	0	0	0	0

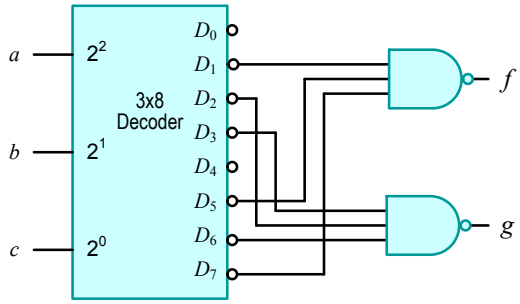


10. 74138 디코더와 OR 게이트를 이용하여 논리함수 구현

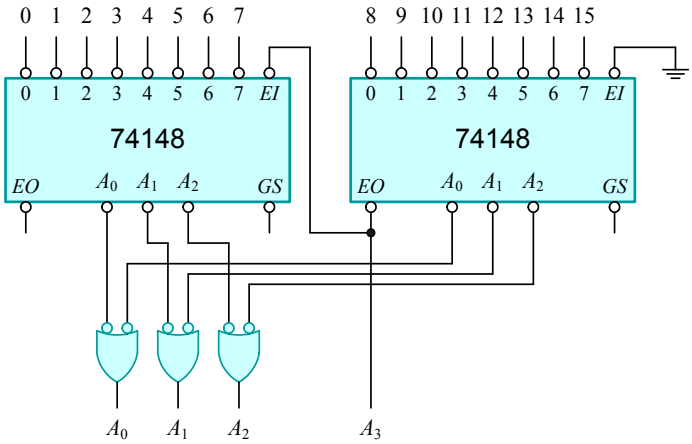


11. 디코더와 NAND 게이트를 이용하여 논리함수 구현

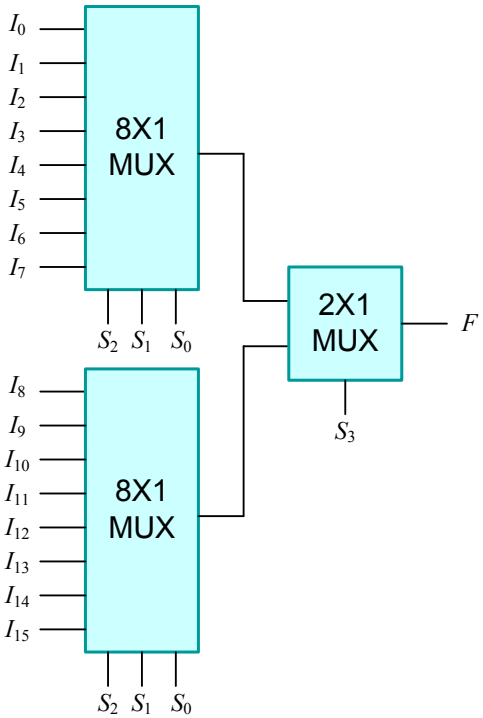
3×8 디코더의 내부가 NAND 게이트로 구성되어 있으므로 디코더의 출력은 active low로 동작한다. 그러나 출력 f와 g는 active high로 동작한다.



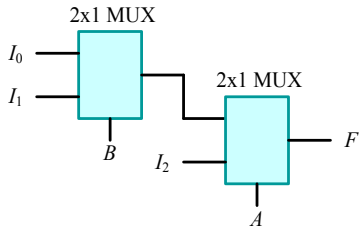
12. 74148을 이용하여 16×4 인코더 설계



13. 16×1 멀티플렉서 설계

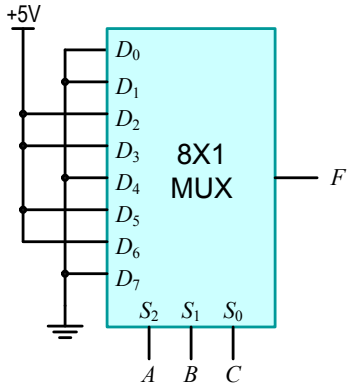


14. 2개의 2×1 멀티플렉서로 다른 게이트 추가없이 3×1 멀티플렉서를 구성



15. 논리함수 F를 8x1 멀티플렉서, 4x1 멀티플렉서를 이용하여 각각 설계

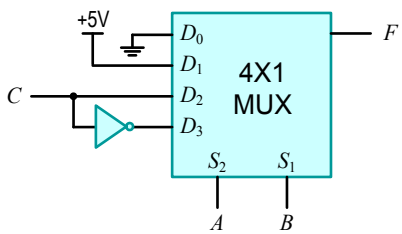
논리함수 $F = AB\overline{C} + \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}C$ 는 입력변수 조합이 110, 010, 011,101일 때, F가 1이 되며, 다른 조합일 때는 F가 0이다. 8x1 멀티플렉서로 이 함수를 구현하려면 F가 1이 되는 변수값들의 조합에 대응하는 데이터 입력들을 High로 연결하고, 이외의 다른 데이터 입력들을 Low에 연결한다.



4x1 멀티플렉서로 함수 F를 구현하려면 데이터 선택 입력 중에서 하나의 비트를 데이터 입력들과 연결하면 된다. 함수 F의 진리표는 아래와 같다.

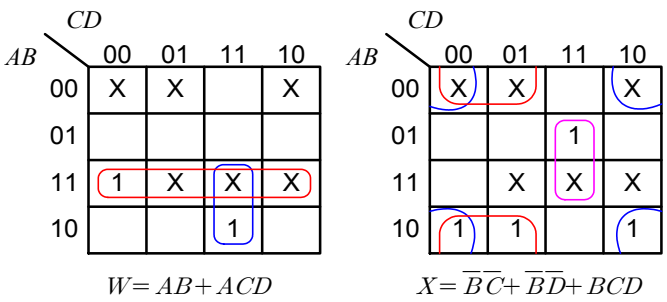
입력			출력
A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

진리표의 첫 번째 행을 보면 $AB=00$일 때 $F=0$이고, 2번째 행도 $AB=00$일 때 $F=0$이므로 $D_0=0$이다. 3번째 행은 $AB=01$일 때 $F=1$이고, 4번째 행도 $AB=01$일 때 $F=1$이므로 $D_1=1$이다. 5번째 행은 $AB=10$일 때 $F=C$이고, 6번째 행도 $AB=10$일 때 $F=C$이므로 $D_2=C$이다. 7번째 행은 $AB=11$일 때 $F=\overline{C}$이고, 8번째 행도 $AB=11$일 때 $F=\overline{C}$이므로 $D_3=\overline{C}$이다.

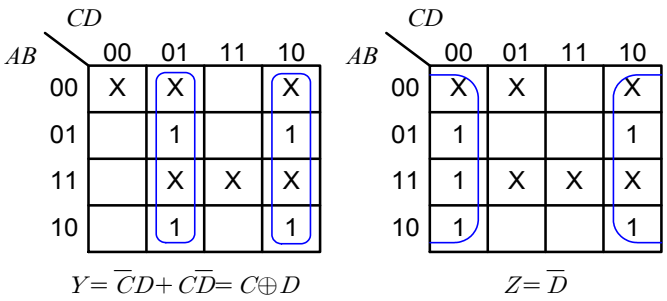


16. 3 초과 코드($ABCD$)를 BCD 코드($WXYZ$)로 변환하는 조합논리회로

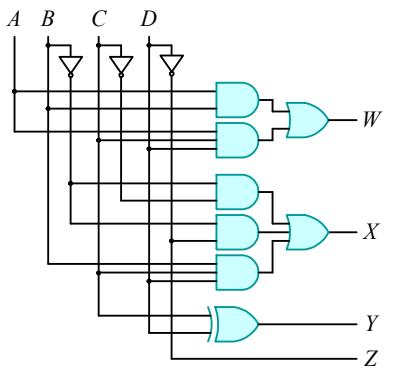
입 력				출 력			
A	B	C	D	W	X	Y	Z
0	0	0	0	x	x	x	x
0	0	0	1	x	x	x	x
0	0	1	0	x	x	x	x
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	1
0	1	0	1	0	0	1	0
0	1	1	0	0	0	1	1
0	1	1	1	0	1	0	0
1	0	0	0	0	1	0	1
1	0	0	1	0	1	1	0
1	0	1	0	0	1	1	1
1	0	1	1	1	0	0	0
1	1	0	0	1	0	0	1
1	1	0	1	x	x	x	x
1	1	1	0	x	x	x	x
1	1	1	1	x	x	x	x



$W = AB + ACD$ $X = \overline{B}\,\overline{C} + \overline{B}\,\overline{D} + BCD$

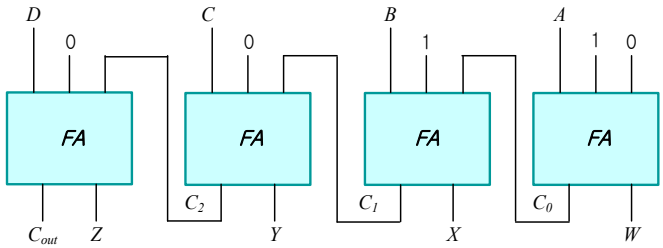


$Y = \overline{C}D + C\overline{D} = C \oplus D$ $Z = \overline{D}$



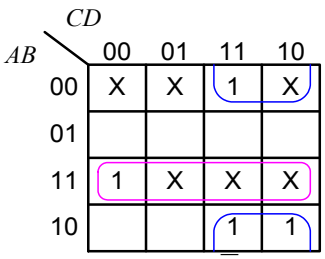
17. 4비트 가산기를 이용하여 BCD코드를 3 초과코드로 변환하는 회로

입력변수 : $DCBA$, 출력변수 : $ZYXW$

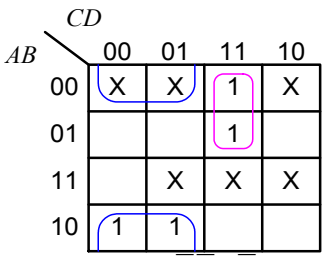


18. 3 초과 코드($ABCD$)를 2 out-of 5 코드($VWXYZ$)로 변환하는 회로

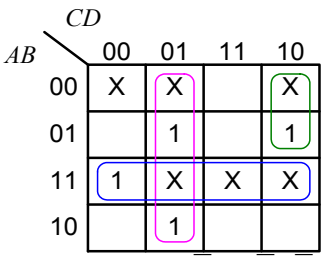
입 력				출 력				
A	B	C	D	V	W	X	Y	Z
0	0	0	0	x	x	x	x	x
0	0	0	1	x	x	x	x	x
0	0	1	0	x	x	x	x	x
0	0	1	1	1	1	0	0	0
0	1	0	0	0	0	0	1	1
0	1	0	1	0	0	1	0	1
0	1	1	0	0	0	1	1	0
0	1	1	1	0	1	0	0	1
1	0	0	0	0	1	0	1	0
1	0	0	1	0	1	1	0	0
1	0	1	0	1	0	0	0	1
1	0	1	1	1	0	0	1	0
1	1	0	0	1	0	1	0	0
1	1	0	1	x	x	x	x	x
1	1	1	0	x	x	x	x	x
1	1	1	1	x	x	x	x	x



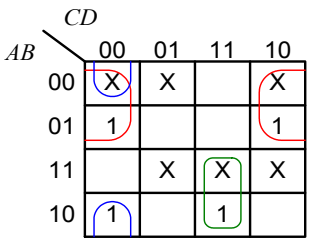
$V = AB + \overline{B}C$



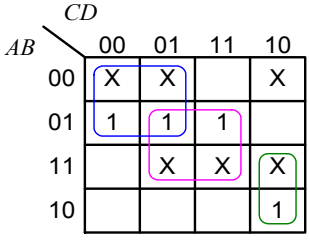
$W = \overline{B}\,\overline{C} + \overline{A}CD$



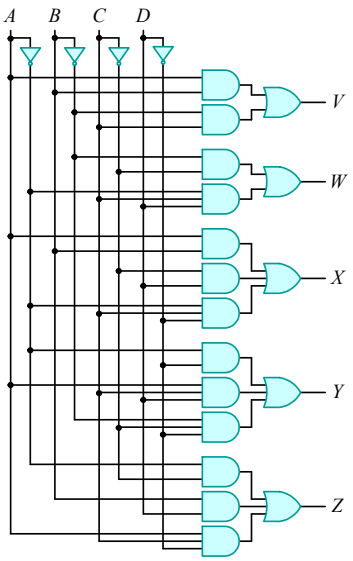
$X = AB + \overline{C}D + \overline{A}\,\overline{C}\,\overline{D}$



$Y = \overline{A}\,\overline{D} + ACD + \overline{B}\,\overline{C}\,\overline{D}$



$Z = \overline{A}\,\overline{C} + BD + AC\overline{D}$



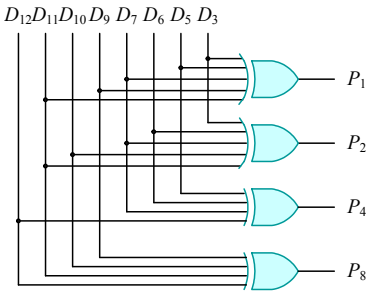
19. 8비트 2진 데이터에 대한 헤밍코드를 생성하는 회로 설계

$$P_1 = D_3 \oplus D_5 \oplus D_7 \oplus D_9 \oplus D_{11}$$

$$P_2 = D_3 \oplus D_6 \oplus D_7 \oplus D_{10} \oplus D_{11}$$

$$P_4 = D_5 \oplus D_6 \oplus D_7 \oplus D_{12}$$

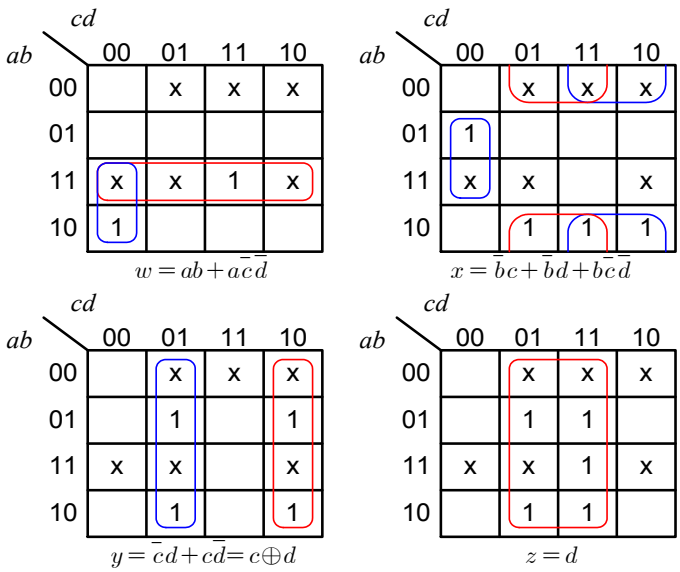
$$P_8 = D_9 \oplus D_{10} \oplus D_{11} \oplus D_{12}$$

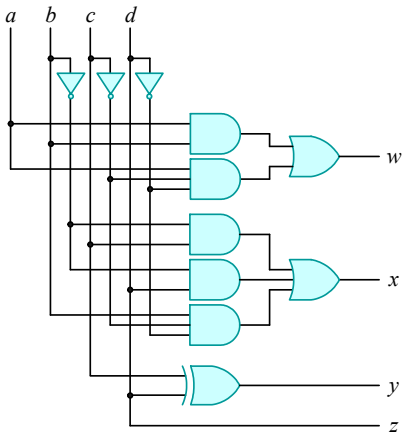


20. 84-2-1 코드를 BCD 코드로 변환하는 회로

입력변수 : a, b, c, d 출력변수 : w, x, y, z

10진수	84-2-1코드				BCD코드			
	a	b	c	d	w	x	y	z
0	0	0	0	0	0	0	0	0
1	0	1	1	1	0	0	0	1
2	0	1	1	0	0	0	1	0
3	0	1	0	1	0	0	1	1
4	0	1	0	0	0	1	0	0
5	1	0	1	1	0	1	0	1
6	1	0	1	0	0	1	1	0
7	1	0	0	1	0	1	1	1
8	1	0	0	0	1	0	0	0
9	1	1	1	1	1	0	0	1

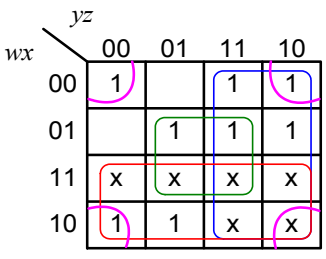




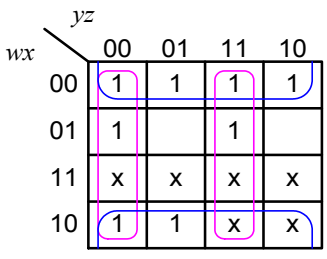
21. NAND 게이트만을 이용하여 BCD 코드를 7-Segment 코드로 변환하는 회로설계

입력변수 : w, x, y, z 출력변수 : a, b, c, d, e, f, g

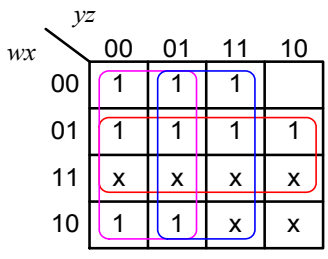
10진수	w	x	y	z	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1
10	1	0	1	0	x	x	x	x	x	x	x
11	1	0	1	1	x	x	x	x	x	x	x
12	1	1	0	0	x	x	x	x	x	x	x
13	1	1	0	1	x	x	x	x	x	x	x
14	1	1	1	0	x	x	x	x	x	x	x
15	1	1	1	1	x	x	x	x	x	x	x



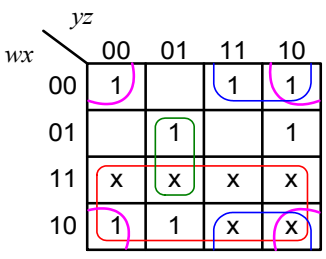
$a = w + y + xz + \bar{x}\bar{z}$



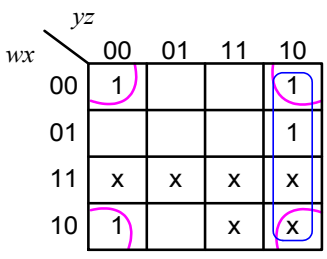
$b = \bar{x} + yz + \bar{y}\bar{z}$



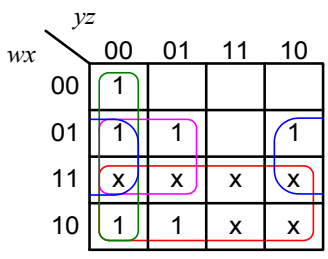
$c = x + \bar{y} + z$



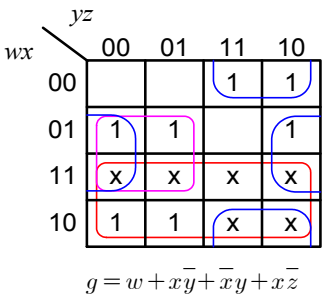
$d = w + \bar{x}y + \bar{x}\bar{z} + x\bar{y}z$



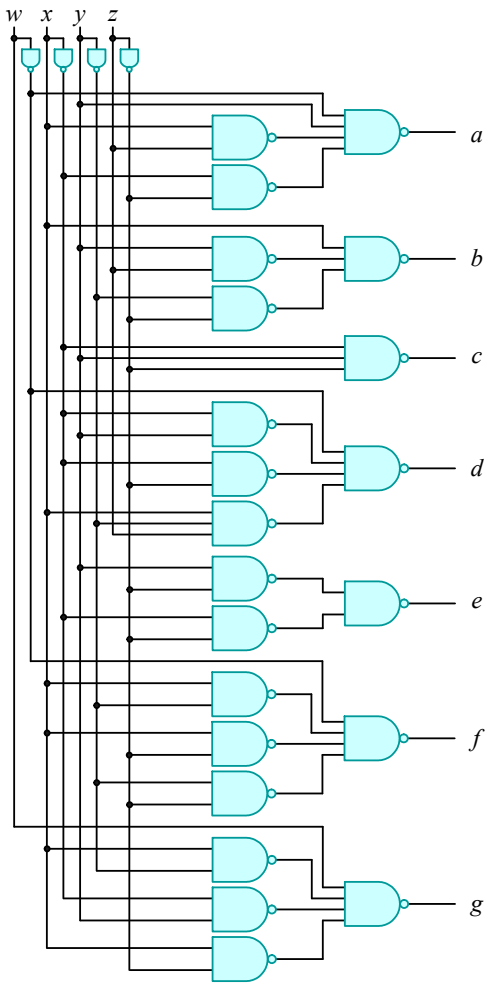
$e = y\bar{z} + \bar{x}\bar{z}$



$f = w + x\bar{y} + x\bar{z} + \bar{y}\bar{z}$



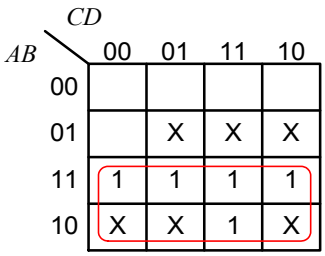
$$g = w + x\bar{y} + \bar{x}y + x\bar{z}$$



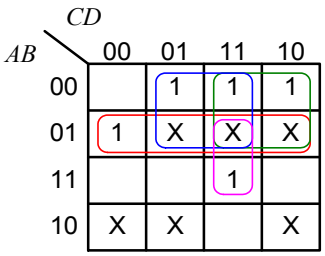
22. 2421 코드를 84-2-1 코드로 변환하는 회로 설계

입력변수 : A, B, C, D 출력변수 : W, X, Y, Z

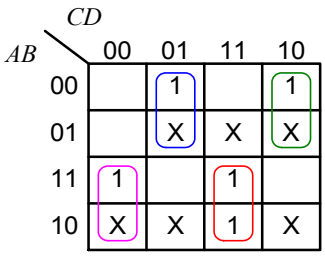
10진수	2421 코드				84-2-1 코드			
	A	B	C	D	W	X	Y	Z
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	1	1
2	0	0	1	0	0	1	1	0
3	0	0	1	1	0	1	0	1
4	0	1	0	0	0	1	0	0
5	1	0	1	1	1	0	1	1
6	1	1	0	0	1	0	1	0
7	1	1	0	1	1	0	0	1
8	1	1	1	0	1	0	0	0
9	1	1	1	1	1	1	1	1



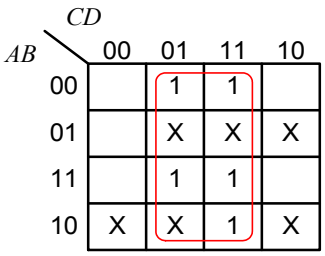
$W = A$



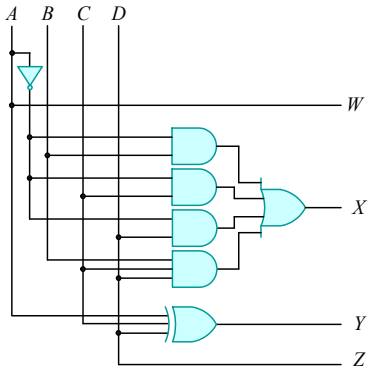
$X = \overline{A}B + \overline{A}C + \overline{A}D + BCD$



$Y = A\overline{C}\overline{D} + ACD + \overline{A}\overline{C}D + \overline{A}C\overline{D}$
$= \overline{A}(C \oplus D) + A(C \odot D)$
$= A \oplus C \oplus D$



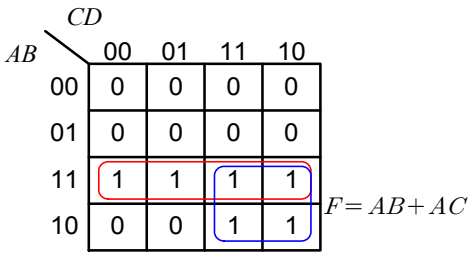
$Z = D$

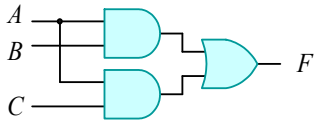


23. BCD 코드 검사회로 설계

입력변수 : A, B, C, D 출력변수 : F

A	B	C	D	F
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

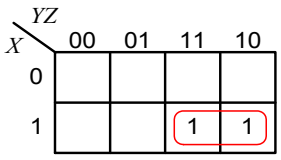




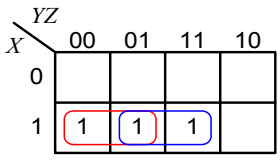
24. 입력된 수의 제곱을 출력하는 회로 설계

입력변수 : X, Y, Z 출력변수 : $a \sim f$

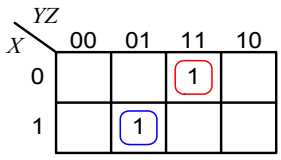
10진수	X	Y	Z	a	b	c	d	e	f
0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	1
2	0	1	0	0	0	0	1	0	0
3	0	1	1	0	0	1	0	0	1
4	1	0	0	0	1	0	0	0	0
5	1	0	1	0	1	1	0	0	1
6	1	1	0	1	0	0	1	0	0
7	1	1	1	1	1	0	0	0	1



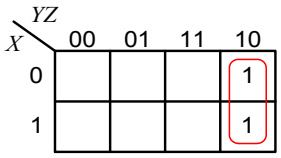
$a = XY$



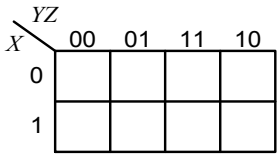
$b = X\bar{Y} + XZ$



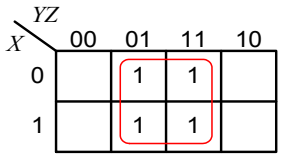
$c = Z(X \oplus Y)$



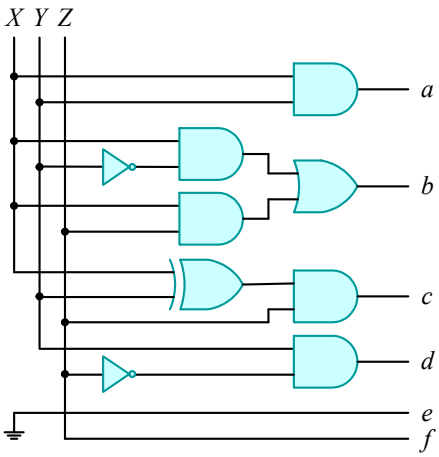
$d = Y\bar{Z}$



$e = 0$

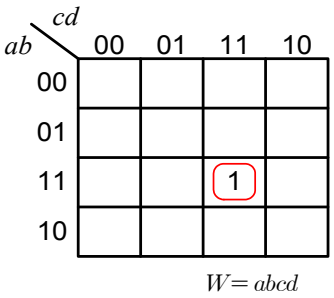


$f = Z$

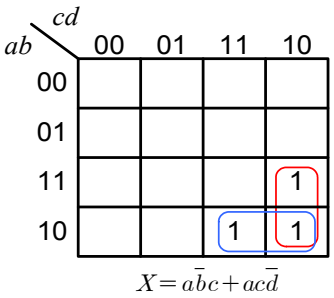


25. 2 비트 숫자 ab와 cdd를 곱하여 4 비트 곱 w, x, y, z를 만드는 회로를 설계

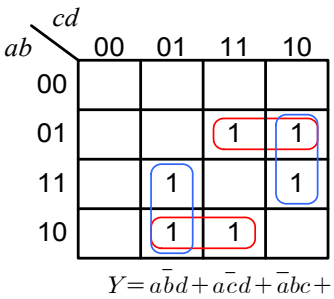
입 력				출 력			
a	b	c	d	W	X	Y	Z
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	0
0	0	1	0	0	0	0	0
0	0	1	1	0	0	0	0
0	1	0	0	0	0	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	0	1	1
1	0	0	0	0	0	0	0
1	0	0	1	0	0	1	0
1	0	1	0	0	1	0	0
1	0	1	1	0	1	1	0
1	1	0	0	0	0	0	0
1	1	0	1	0	0	1	1
1	1	1	0	0	1	1	0
1	1	1	1	1	0	0	1



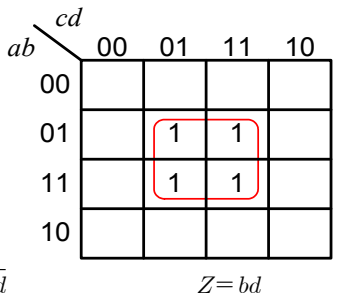
$W = abcd$



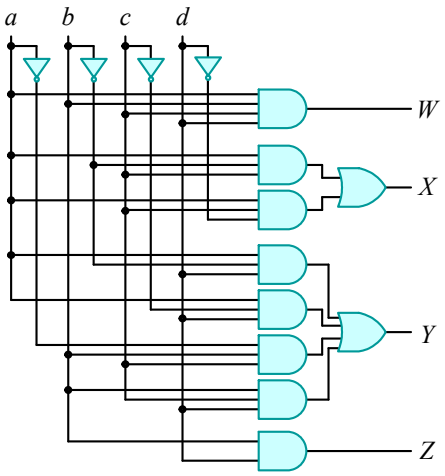
$X = a\bar{b}c + ac\bar{d}$



$Y = a\bar{b}d + a\bar{c}d + \bar{a}bc + b\bar{c}\bar{d}$



$Z = bd$

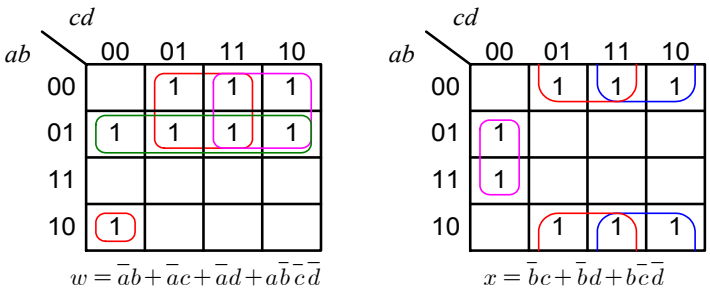


26. 2의 보수를 계산하는 회로 설계

입력변수 : $a,\ b,\ c,\ d$ 출력변수 : $w,\ x,\ y,\ z$

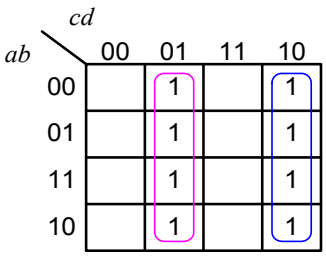
10진수	a	b	c	d	w	x	y	z
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	1	1
2	0	0	1	0	1	1	1	0
3	0	0	1	1	1	1	0	1
4	0	1	0	0	1	1	0	0
5	0	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	0
7	0	1	1	1	1	0	0	1
8	1	0	0	0	1	0	0	0
9	1	0	0	1	0	1	1	1
10	1	0	1	0	0	1	1	0
11	1	0	1	1	0	1	0	1
12	1	1	0	0	0	1	0	0
13	1	1	0	1	0	0	1	1
14	1	1	1	0	0	0	1	0
15	1	1	1	1	0	0	0	1

입출력 관계로부터 다음과 같은 카르노 맵을 얻으며 이를 정리한다.

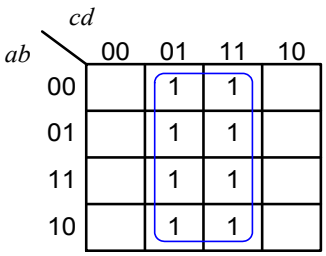


$w = \bar{a}b + \bar{a}c + \bar{a}d + a\bar{b}\bar{c}\bar{d}$

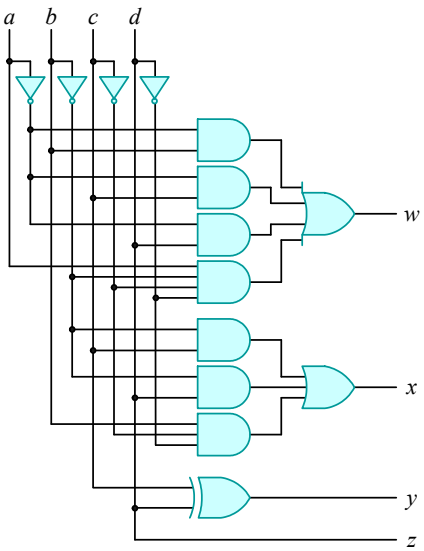
$x = \bar{b}c + \bar{b}d + b\bar{c}\bar{d}$



$y = c\bar{d} + \bar{c}d = c \oplus d$



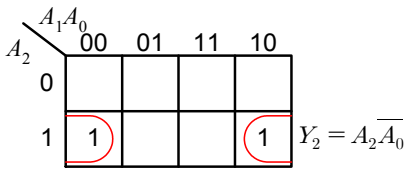
$z = d$

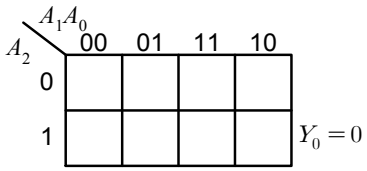


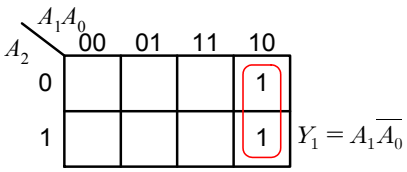
27. 짝수만을 통과시키는 논리회로 설계

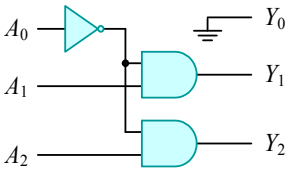
입력변수 : A_2, A_1, A_0 출력변수 : Y_2, Y_1, Y_0

A_2	A_1	A_0	Y_2	Y_1	Y_0
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	0	1	0
0	1	1	0	0	0
1	0	0	1	0	0
1	0	1	0	0	0
1	1	0	1	1	0
1	1	1	0	0	0





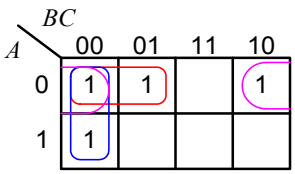




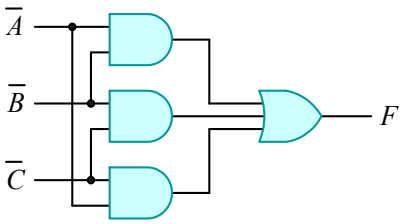
28. Majority Function 설계

입력변수 : A, B, C 출력변수 : F

A	B	C	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0



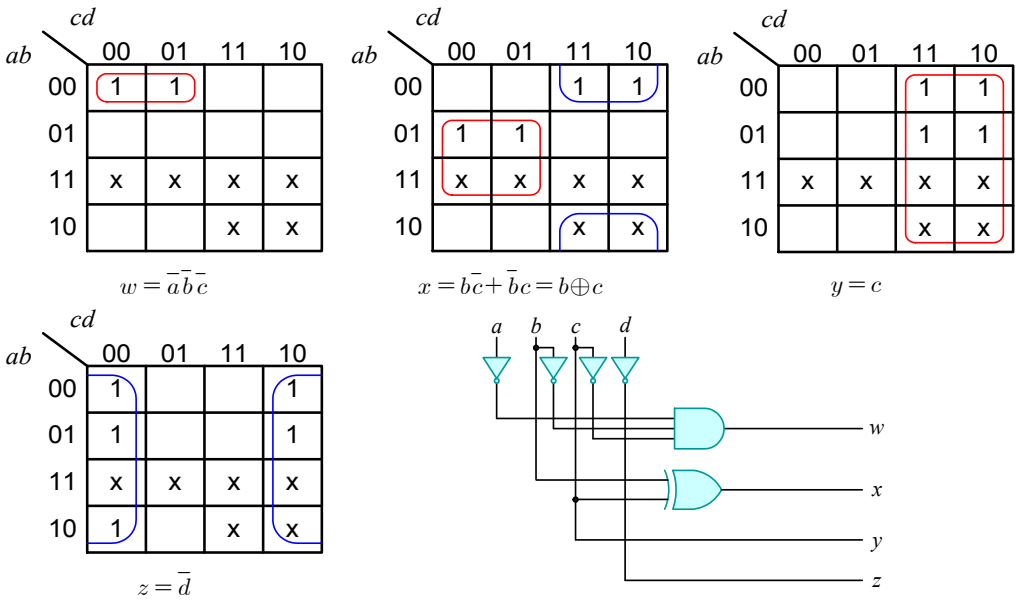
$F = \overline{A}\overline{B} + \overline{B}\overline{C} + \overline{A}\overline{C}$



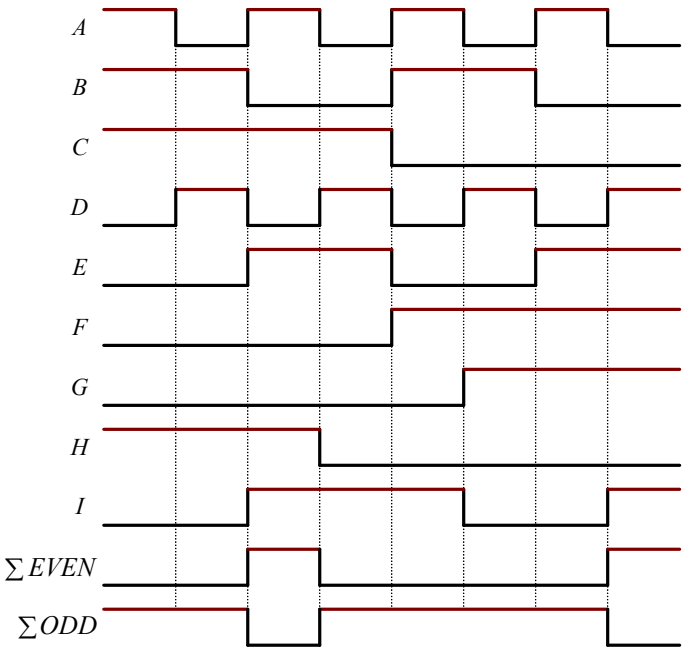
29. 9의 보수 생성회로 설계

입력변수 : a, b, c, d 출력변수 : w, x, y, z

10진수	a	b	c	d	w	x	y	z
0	0	0	0	0	1	0	0	1
1	0	0	0	1	1	0	0	0
2	0	0	1	0	0	1	1	1
3	0	0	1	1	0	1	1	0
4	0	1	0	0	0	1	0	1
5	0	1	0	1	0	1	0	0
6	0	1	1	0	0	0	1	1
7	0	1	1	1	0	0	1	0
8	1	0	0	0	0	0	0	1
9	1	0	0	1	0	0	0	0



30. 9-비트 패리티 발생기/검출기에서 출력 $\Sigma EVEN$과 ΣODD를 구하는 문제.

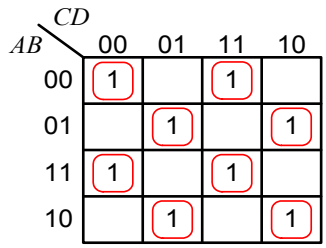


31. 4비트 홀수 패리티 발생기와 짝수 패리티 발생기를 설계

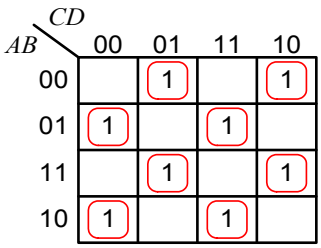
(1) 진리표

데이터	패리티	
$A\ B\ C\ D$	홀수(P_{ODD})	짝수(P_{EVEN})
0 0 0 0	1	0
0 0 0 1	0	1
0 0 1 0	0	1
0 0 1 1	1	0
0 1 0 0	0	1
0 1 0 1	1	0
0 1 1 0	1	0
0 1 1 1	0	1
1 0 0 0	0	1
1 0 0 1	1	0
1 0 1 0	1	0
1 0 1 1	0	1
1 1 0 0	1	0
1 1 0 1	0	1
1 1 1 0	0	1
1 1 1 1	1	0

(2) 카르노 맵을 이용한 간소화



$P_{ODD} = A \odot B \odot C \odot D$



$P_{EVEN} = A \oplus B \oplus C \oplus D$

(3) 회로도