Calculating Fabrication Cost
Selecting a Commercial Chip Fabricator

EEL 3801

Given: You're tasked with selecting the most cost-competitive foundry for producing uni-core MIPS-74K processors, which have die dimensions of 1 cm x 1 cm:

- Taiwan Semiconductor Inc. produces 30cm diameter wafers with 90% yield for $2,000.
- Global Foundries Inc. produces 45cm diameter wafers with 70% yield for $3,000.

Both foundries' other packaging, test, and production costs total $1 per shippable chip,.

Partial Credit 1: Which relation below can be used to approximate the total number of [Dies on a wafer]?

a) [Wafer area] / (pi * [Die area])
b) [Wafer area] / (pi * [Die area]^2)
c) [Wafer area] / sqrt([Die area])
d) [Wafer area] / [Die area]
e) [Die area] / (pi * [Wafer area])
f) [Die area] / (pi * [Wafer area]^2)
g) [Die area] / sqrt([Wafer area])
h) [Die area] / [Wafer Area]

Partial Credit 2: Which relation below can be used to calculate the [Number of Working Dies] per wafer?

a) [Dies on a Wafer] * [Yield]
b) [Dies on a Wafer] / [Yield]
c) [Yield] / [Dies on a Wafer]
d) [Yield]^2 / [Dies on a Wafer]
e) [Yield]^2 / ([Dies on a Wafer] + 1)
f) [Yield] / ([Dies on a Wafer]^2)
g) [Yield] / ([Dies on a Wafer] + 1)^2
h) ([Yield] + 1) / ([Dies on a Wafer]^2)

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Partial Credit 3: Which choice below best indicates the low cost supplier along with its unit cost per chip?

a) Taiwan Semiconductor having unit cost of $1.12
b) Taiwan Semiconductor having unit cost of $3.15
c) Taiwan Semiconductor having unit cost of $635
d) Taiwan Semiconductor having unit cost of $704
e) Taiwan Semiconductor having unit cost of $705
f) Taiwan Semiconductor having unit cost of $706
g) Taiwan Semiconductor having unit cost of $707
h) Taiwan Semiconductor having unit cost of $1,112
i) Global Foundries having unit cost of $0.12
j) Global Foundries having unit cost of $1.12
k) Global Foundries having unit cost of $2.12
l) Global Foundries having unit cost of $2.70
m) Global Foundries having unit cost of $3.70
n) Global Foundries having unit cost of $1,112
y) none of the choices listed
z) insufficient information to determine

Partial Credit 4: True or False: "Global Foundries has a lower number of defects per mm^2 than Taiwan Semiconductor."

a) True
b) False

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Solution 1: [Dies on a Wafer] ≈ [Wafer Area] / [Die Area]. So select choice d).
We can understand this as an approximation because wafers are round due to how the silicon ingot naturally forms. Meanwhile, Dies are rectangular as they get diced with a saw. So a small amount of rounded area near the wafer's edge can be used for test pads rather than functional rectangular Dies.

Solution 2: [Number of Working Dies] = [Dies on a Wafer] * [Yield]. So select choice a).
We can understand this as the definition of Yield, by knowing its meaning without memorizing this formula.

Solution 3: First, determine the number of dies on a wafer as approximated by the area of a circular wafer:
[Dies on a wafer] ≈ [Wafer area] / [Die area]
For the 30cm wafer, [Dies on a wafer] = [pi*(15cm)^2]/ [1 cm * 1 cm)] = about 706 dies. Of those, 0.90*706=635 would be operational. Thus, the cost is $2000/635=$3.15 per die, plus $1 for packaging, provides a shippable chip for $4.15.
For the 45cm wafer, [Dies on a wafer] = [pi*(22.5cm)^2]/ [1 cm * 1 cm)] = about 1589 dies. Of those, 0.70*1589=1112 would be operational. Thus, a cost of $3000/1112=$2.70 per die, plus $1 for packaging, provides a shippable chip for $3.70.
Thus, Global Foundries has the least cost per chip at $3.70 so select choice m). The governing equation is:

$$[\text{Die Fabrication Cost}] = \frac{[\text{Photolithography Cost}]}{\{[\text{Dies on a Wafer}] \times [\text{Yield}]\}}$$

$\{[\text{Dies on a Wafer}] \times [\text{Yield}]\}$ ⟷ *number of working dies*

Solution 4: False. Since its yield is less at only 70% rather than 90%, because Yield is inversely-related to Defect Density with a non-linear squared relationship:

$$[\text{Yield}] = \frac{1}{(1+\{0.5\times[\text{Defect Density}]\times[\text{Die Area}]\})^2}$$

Likewise it is important to know that Yield is also inverse-related to Die Area with a non-linear squared relationship.

Calculating Fabrication Cost

Manufacturing vs. Edifice cost of dual-core i3 chip

Given: An Intel 300mm diameter wafer has a photolithography cost of $5000 for a dual-core Core i3 processor which has a (10mm x 10mm) die. The defect density for a production run is 0.00105 defects/mm^2. Chip package and other production costs incur an additional $2 per die.

Sought: Estimate the fabrication cost of a packaged Core i3 chip.

Solution: [Dies on a Wafer] = [Wafer Area] / [Die Area]

= [π * {(150mm)^2}] / [100 mm^2] *since 300mm diameter → 150mm radius*

= [3.14 * 22500] / [100] = 706 dies on a wafer

$$[\text{Yield}] = \frac{1}{(1+\{0.5\times[\text{Defect Density}]\times[\text{Die Area}]\})^2}$$

Yield = 1 / ([1 + {0.5 * 0.00105 defect/mm^2 * 100 mm^2 }) ^2 }

= 1 / { (1 + 0.0525) ^2 } = 1 / { 1.0525^2 } = 1/1.108 = 0.902 *"90.2% yield"*

Substituting into [Die Fabrication Cost] = [Photolithography Cost] / { [Dies on a Wafer] * Yield}

= $5000 / {706*0.902) = $7.85

so fabrication cost of packaged chip = $7.85 + $2 = $9.85

$100 sales price with 50% profit margin, but typically 80% of the $50 product expense is amortizing the equipment and edifice costs.

Power Dissipation
Re-designing CPU for Power Reduction

Given: Suppose a new CPU is being considered that will have:

- 85% of capacitive load of the original CPU design
- 15% voltage reduction
- 15% frequency reduction

Sought: How does its power dissipation compare with the original design?
Provide a precise declarative statement on the impact for a formal report, and an informal statement for discussion at an upcoming project meeting.

Solution: Power dissipation is given by $P = C \times V^2 \times F$. Relative power would then be expressed as the ratio:

$$\frac{P_{new}}{P_{orig}} = \frac{C_{old} \times 0.85 \times (V_{old} \times 0.85)^2 \times F_{old} \times 0.85}{C_{old} \times V_{old}^{\ 2} \times F_{old}} = (0.85)^4 = 0.52$$

Thus, the new design dissipates 52% of the power of the original design.

Expressed as power savings, the new design saves (1-0.52)/1 * 100% = 48%. So the combination of the above 15% individual reductions would realize 48% savings in power dissipation.

Less formally, the above modifications would combine to cut power dissipation nearly in half.

1.10 Assume a 15 cm diameter wafer has a cost of 12, contains 84 dies, and has 0.020 defects/cm^2. Assume a 20 cm diameter wafer has a cost of 15, contains 100 dies, and has 0.031 defects/cm^2.

1.10.1 [10] <§1.5> Find the yield for both wafers.

1.10.2 [5] <§1.5> Find the cost per die for both wafers.

1.10.3 [5] <§1.5> If the number of dies per wafer is increased by 10% and the defects per area unit increases by 15%, find the die area and yield.

1.10.4 [5] <§1.5> Assume a fabrication process improves the yield from 0.92 to 0.95. Find the defects per area unit for each version of the technology given a die area of 200 mm^2.

1.10.1 $\text{die area}_{15cm} = \text{wafer area/dies per wafer} = \pi * 7.5^2 / 84 = 2.10\ cm^2$

$\text{yield}_{15cm} = 1/(1+(0.020*2.10/2))^2 = 0.9593$

$\text{die area}_{20cm} = \text{wafer area/dies per wafer} = \pi * 10^2/100 = 3.14\ cm^2$

$\text{yield}_{20cm} = 1/(1+(0.031*3.14/2))^2 = 0.9093$

1.10.2 $\text{cost/die}_{15cm} = 12/(84*0.9593) = 0.1489$

$\text{cost/die}_{20cm} = 15/(100*0.9093) = 0.1650$

1.10.3 $\text{die area}_{15cm} = \text{wafer area/dies per wafer} = \pi * 7.5^2/(84*1.1) = 1.91\ cm^2$

$\text{yield}_{15cm} = 1/(1 + (0.020*1.15*1.91/2))^2 = 0.9575$

$\text{die area}_{20cm} = \text{wafer area/dies per wafer} = \pi * 10^2/(100*1.1) = 2.86\ cm^2$

$\text{yield}_{20cm} = 1/(1 + (0.03*1.15*2.86/2))^2 =$ 0.9053

1.10.4 $\text{defects per area}_{0.92} = (1-y\text{^}.5)/(y\text{^}.5*\text{die\_area}/2) = (1-0.92\text{^}.5)/(0.92\text{^}.5*2/2) = 0.043\ \text{defects/cm}^2$

$\text{defects per area}_{0.95} = (1-y\text{^}.5)/(y\text{^}.5*\text{die\_area}/2) = (1-0.95\text{^}.5)/(0.95\text{^}.5*2/2) = 0.026\ \text{defects/cm}^2$

Processor Energy
Calculating Joules/instruction & MIPS/mW

Given: Instructions executed on a prototype system have characteristics indicated in the table below:

Instruction Class	CPI	Energy (nanojoule)
{Set}	1	1
{Add}	2	2
{Branch}	4	3
{Read, Write}	3	8

1) processor **Sets** loop index i=0 /* i=0 */
2) processor **Reads** data from memory address 50
3) processor **Reads** data from memory address 51
4) processor **Adds** to create result
5) processor **Adds** one to loop index i /* i=i+1 */
6) processor **Branches** if (i<=4999) then goto step 4)
7) processor **Writes** result to address 52

Sought: If the processor clock cycle time is 333 psec then calculate the Energy needed to complete execution of the program listed above. Also, calculate the metric of MIPS/mW.

Solution: Energy is independent of execution rate. Thus, Energy consumed to execute the program can be computed as the sum of energy consumed by each instruction executed. This program executes 1 Set, 2 Read, 1 Write, and 5000*{Add, Add, Branch} instructions consuming 1*1 + 2*8 + 1*8 + 5000*{2+2+3} nanojoule = 1+16+8+5000*7=35025 nanojoule = 35 microjoule in total.

To compute MIPS/mW, we can first find MIPS. The number of clocks required for [1 Set, 2 Read, 1 Write, and 5000*{Add, Add, Branch}] is [1*1 + 2*3 + 1*3 + 5000*{2+2+4}] = [1+6+3+5000*8] = 40010 clocks. Thus, the program requires [40010 clocks] * [333 psec/clock] = 13,323,330 psec = 13,323 nsec = 13.323 usec. The number of instructions executed was [3+(5000*3)+1]=15,004 instructions=(15.004E3) instructions =(0.015004E6) instructions = 0.015004 Million Instructions. That number of instructions were executed in [13.323E-6] seconds, yielding [0.015004 Million Instructions]/[13.323E-6 sec] = 1126.1 MIPS.

Since E=P*[Running Time], then power is calculated as P=E/[Running Time]=[(35E-6) joule]/[(13.323E-6) sec]=2.627 joule/sec=2.627 Watt=2627 mW.

Thus, it achieves [1126.1 MIPS] / [2627 mW] = 0.428 MIPS/mW.