Lab 4: 1 GHz Microwave Amplifier with a Specified Gain

Youssef Samwel

yo800238@ucf.edu

EEL5439C RF and Microwave Active Circuits

Prof. Dr. Kenle Chen - Section 0012

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1.0 Experiment Objective

The objective of this lab is to design and simulate a microwave amplifier at 1 GHz with a specified gain.

2.0 Schematic Design

For this experiment, we will be designing a small signal power amplifier at 1 GHz, the gain is to be determined by the student, for my design, I choose 12 dB power gain.

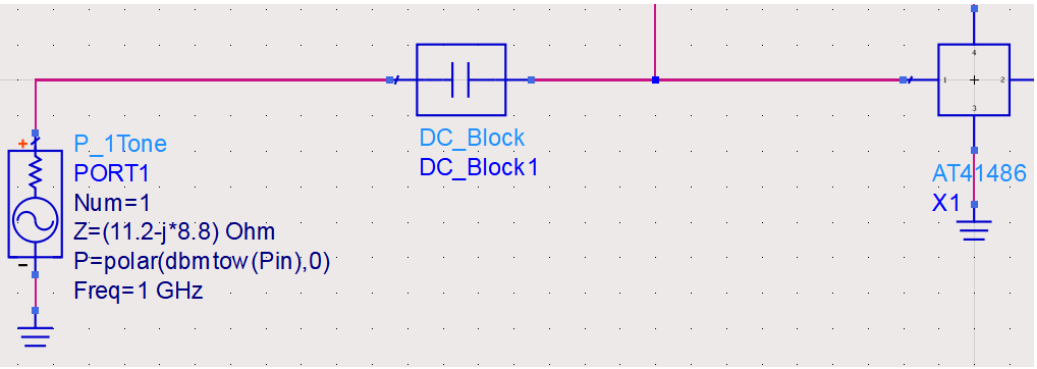
The first step in any Power Amplifier (PA) synthesis is the schematic design. Our PA is composed of four components which are the following:

- DC biasing network
- Input Matching Circuit (w/ DC block)
- Output Matching Circuit (w/ DC block)
- Active Device (transistor; BJT for this lab)

A critical first step in any PA design is the DC feeding network. The active devices need to be biased in the forward active regions so that small deviations at the input port will lead to large deviations at the output port. An issue will arise if we directly connect the DC bias circuit to the base junction. The input RF signal will “see” the DC bias circuit as ground and therefore the majority of the RF signal will be shorted. The same will happen with the DC current as it will also “see” the RF source as ground and will be shorted. To fix this issue we will use a RF choke to prevent the RF short and DC block to prevent DC block.

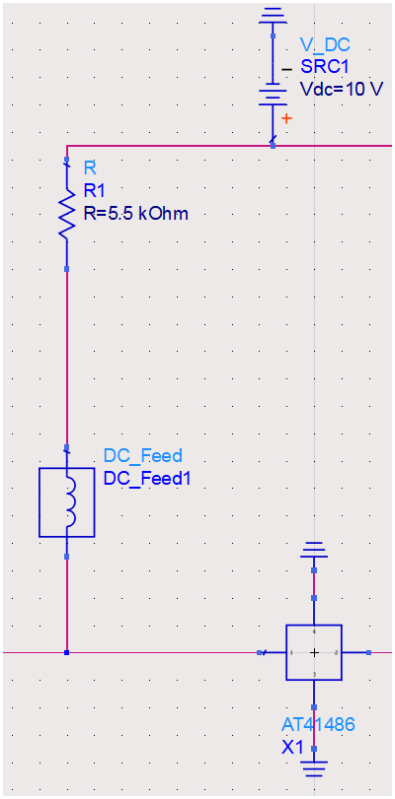
The RF choke is an inductor (or the equivalent distributed element) that is connected in the following manner. The DC current will see the inductor as a zero impedance whereas the RF signal will see the inductor as high impedance.

The same principle is also used with the DC block. The DC current will see an infinite impedance at the capacitor whereas the RF signal will see a zero impedance at the capacitor.



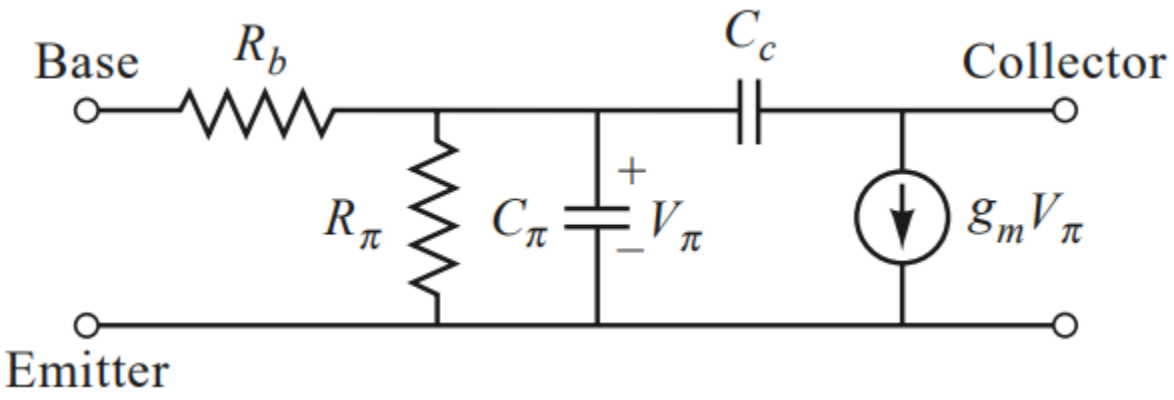
DC Block

For this lab, our focus was more on PA design process which is why we used a simplistic DC bias circuit. Our biasing network does not account for process variations in h_{FE} or temperature changes.



RF Choke

The active device is the component responsible for the amplification, however, the device must be in the right configuration to amplify the input signal.

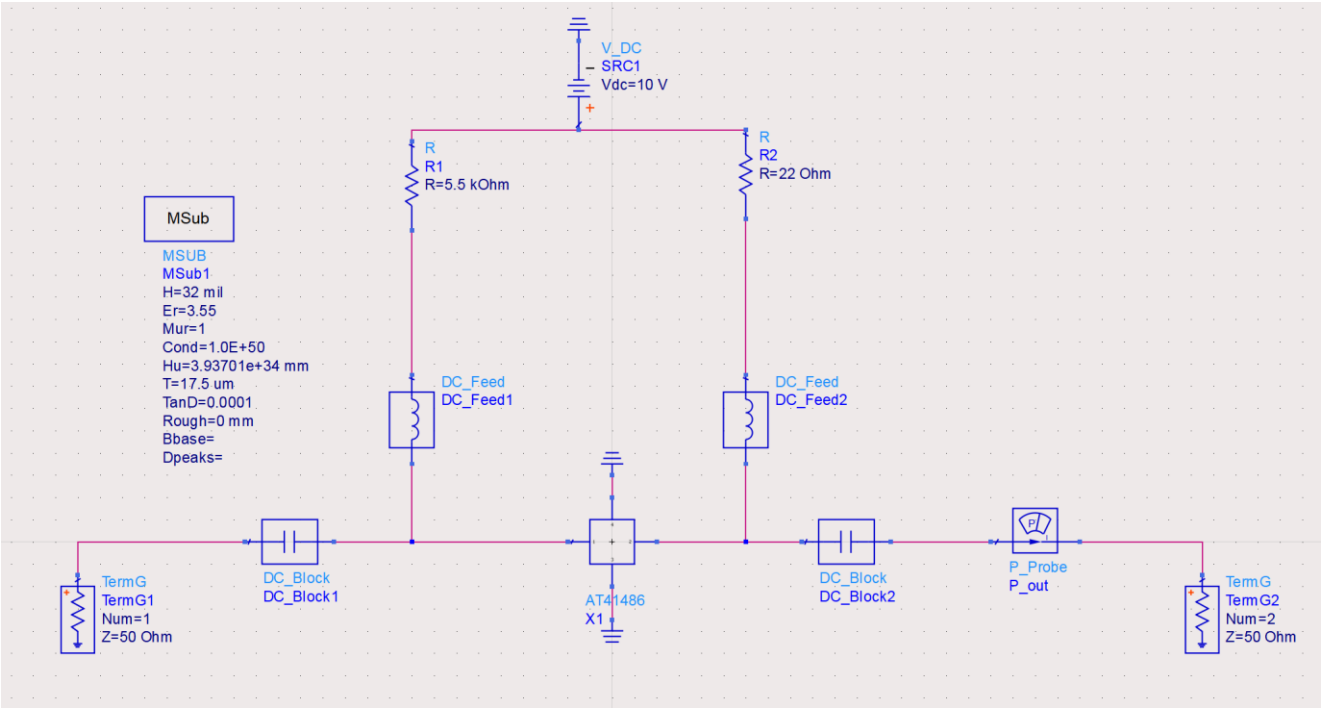


Simplified Model of BJT Device

In the simplified model of the BJT, the reader should observe that amplification is controlled primarily by g_m and the parasitic junction competence: C_π. Now, C_π, is the critical term that determines the operation range of the transistor because regardless of the capacitance of the junction, it will eventually be reduced to a short circuit directly causing V_π to approach zero and as result the amplification provided at the collector port will also decrease. It can be modeled using the following formula that the upper frequency of operation where gain is equal to unity to controlled by C_π in the following manner:

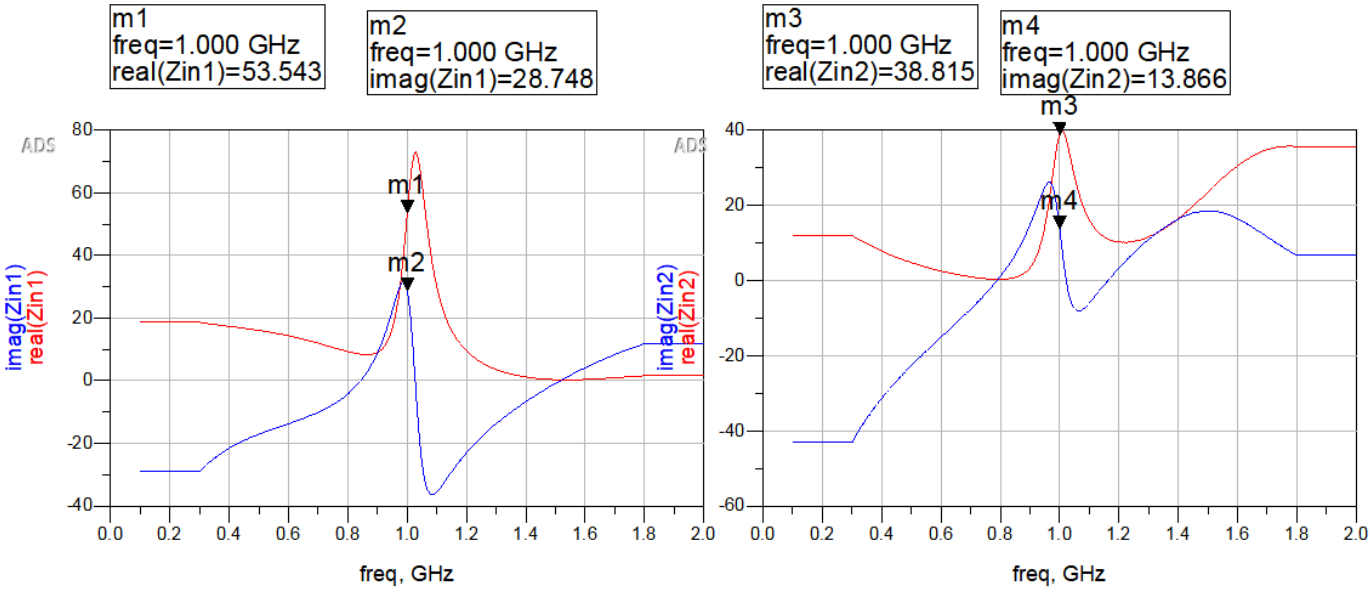
$$f_T = \frac{g_m}{2\pi C_\pi}$$

With the previous setup, we can now place the necessary components in ADS.

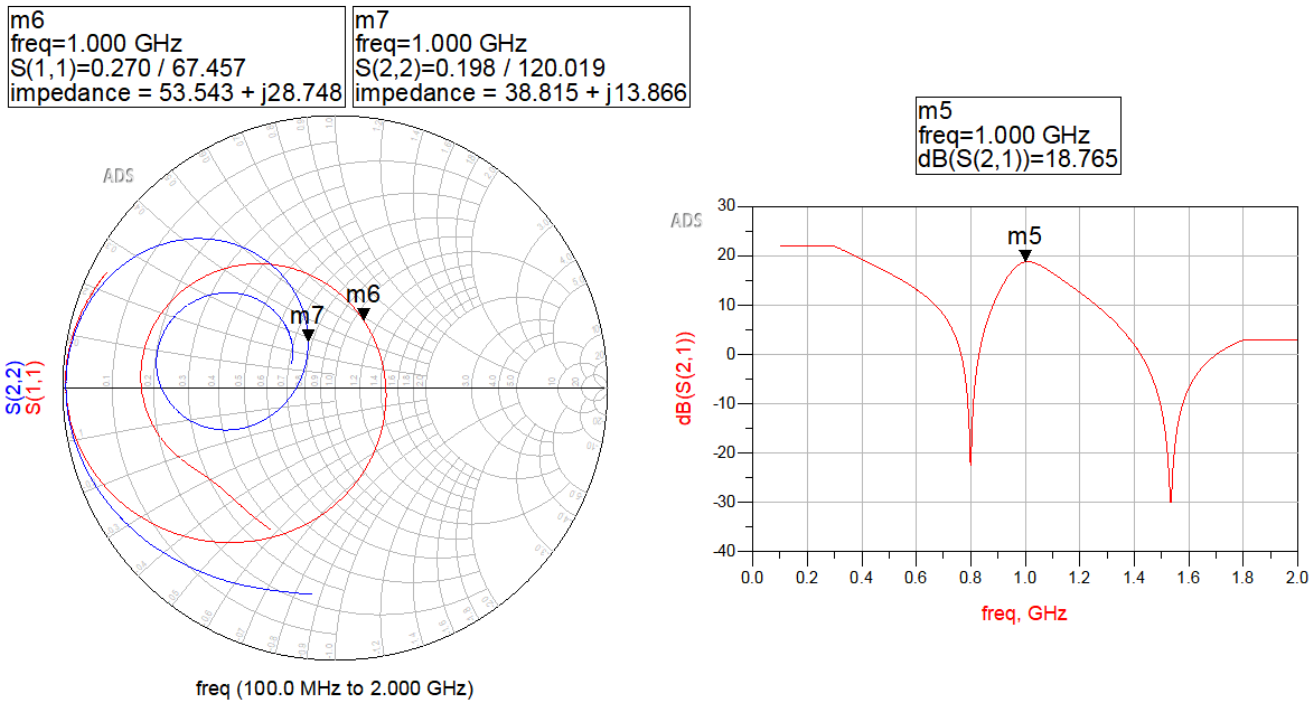


Simplified Schematic of Small Signal PA

The package parasitic must also be considered in the design process because BJT device will have a frequency dependent input and output impedance. For specific gain, we can induce a controlled impedance mismatch at either the input or output port to reduce or increase the gain. To characterize the frequency dependent input and output impedance, we used a VNA to measure the S-parameters of the BJT.



Port 1 and Port 2 Impedance of BJT (Measured)



$S_{21}(dB)$ gain and S_{11} S_{22} on Smith Chart of Measured BJT Device

2.2 Stability Circles

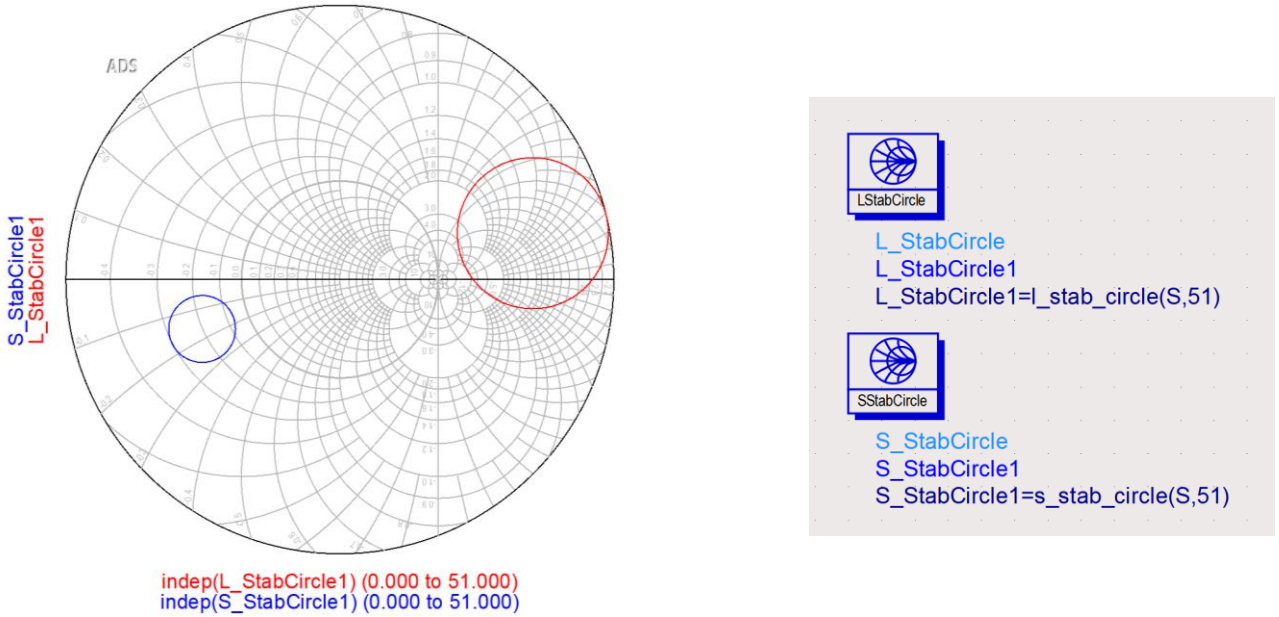
One of the most important design steps in any PA is stability. If the device is not stable it cannot be used in any professional setting. A non-stable PA will resonate which will cause interference with other communication channels. The following are the conditions for stability:

$$|\Gamma_{\text{in}}| = \left| S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} \right| < 1,$$

$$|\Gamma_{\text{out}}| = \left| S_{22} + \frac{S_{12}S_{21}\Gamma_S}{1 - S_{11}\Gamma_S} \right| < 1.$$

These conditions can be used to define stability circles on the smith chart which define the regions of stability and non-stability. These regions determine the possible input and output impedances.

The stability circles can be computed in ADS using the L_StabCircle and S_StabCircle components.



Source and Load Stability Circles at center frequency.

From the stability circles and S_{11} and S_{22} we can determine that the BJT is stable at all passive source/load impedances at the center frequency.

We also must ensure that the PA is also stable around the center frequency, for this we can use the Rollet's condition to test the stability of the device. It is also referred to as K – Δ test.

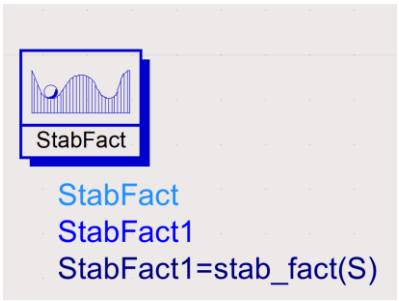
$$K = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} > 1$$

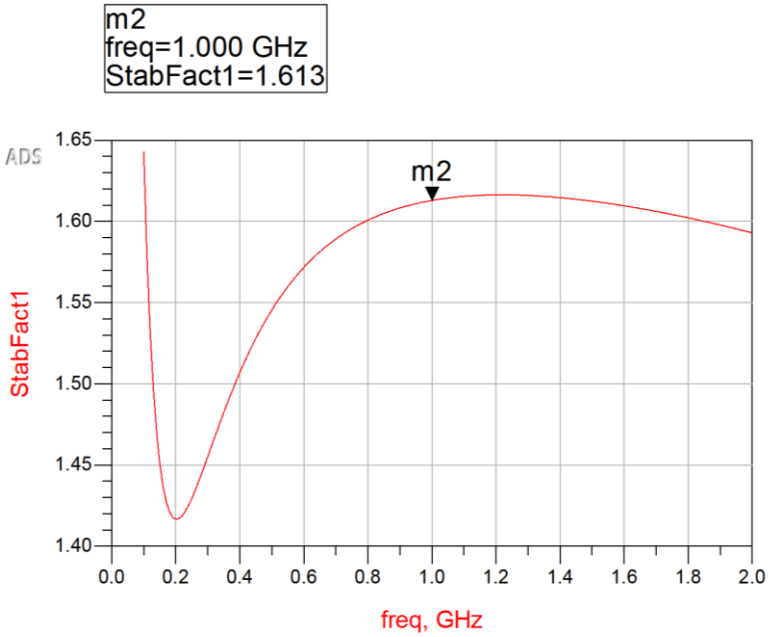
$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| < 1$$

The K – Δ test can be combined into one parameter (called Stability Factor in ADS) with the following equation,

$$\mu = \frac{1 - |S_{11}|^2}{|S_{22} - \Delta S_{11}^*| + |S_{12}S_{21}|} > 1$$

To simulate the stability factor in ADS, we can use the StabFact component.





Simulated Stability Factor

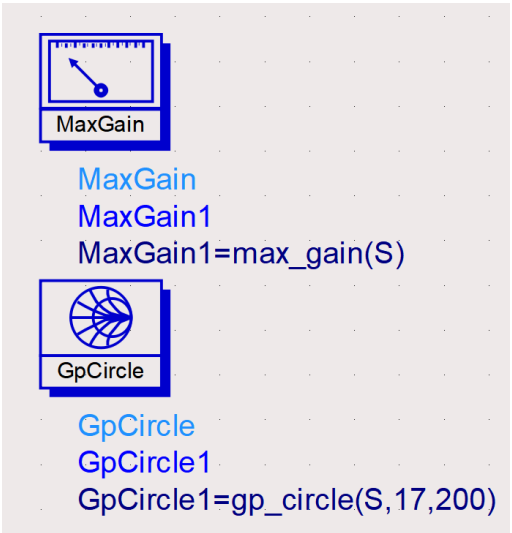
From the stability factor we can conclude that the BJT is stable at the center frequency and the neighboring frequencies.

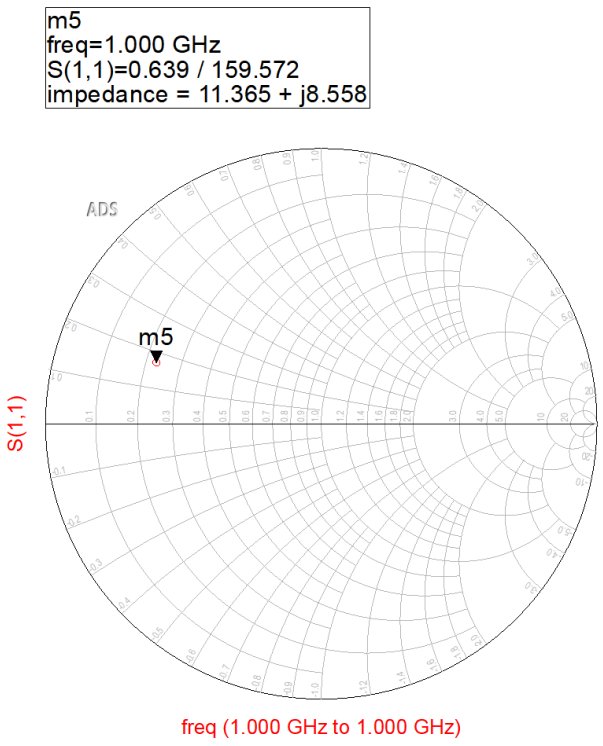
2.4 Specific Gain

The reason to design for a specific gain is for wider bandwidth and to achieve design specification. A higher amount of gain will reduce the available bandwidth. Specific gain can be achieved by controlling the reflection coefficient of the input and output port. Since the total system gain is defined by: $G_S G_0 G_L$ where G_S is gain due to input matching network, G_0 is gain due to transistor (S_{21} in unilateral transistor), and G_L is gain due to output matching network, we can change G_S and G_L to achieve a specific gain. For my design, I chose 12 dB of gain. In accordance with the lab guidance, I used conjugate matching for the input port and used the gain circle of 12 dB at the output port.

To determine the input impedance, we can use the simulated S_{11} parameters.

Since the desired $Z_S = S_{11}^*$, we can determine from Scattering parameter simulation that the desired source impedance is $Z_S = 11.365 - j8.558\ \Omega$. Next, we must also find the output impedance; this can be done through the MaxGain and GpCircle components in ADS.



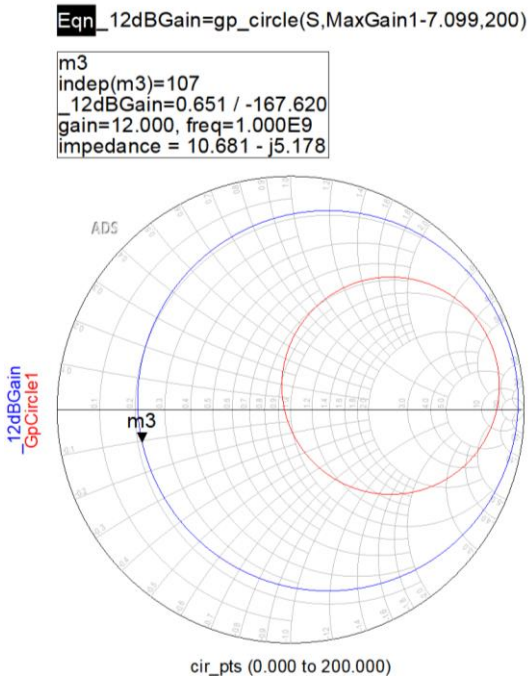


Simulated S_{11} at Center Frequency

The 12 dB gain circle shows all the possible load impedances that would provide the specific gain. The circle can be computed using the following equation, however, in ADS we can find the circle by subtracting 7.1 dB from the MaxGain circle using the equation tool.

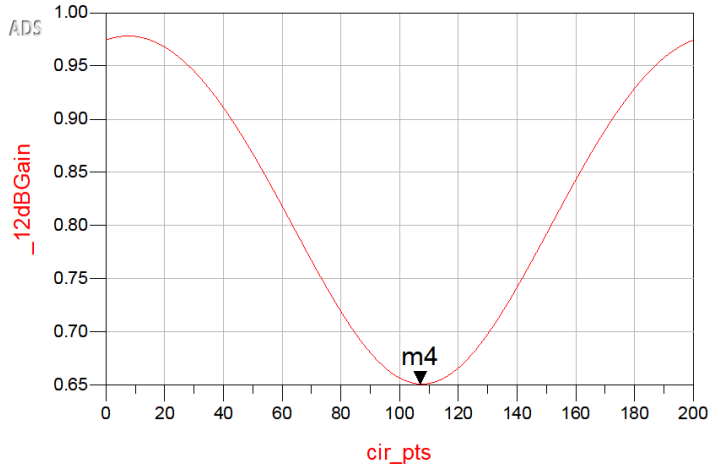
$$C_L = \frac{g_L S_{22}^*}{1-(1-g_L)|S_{22}|^2},$$

$$R_L = \frac{\sqrt{1-g_L}\left(1-|S_{22}|^2\right)}{1-(1-g_L)|S_{22}|^2}.$$



Max Gain Circle and 12 dB Gain Circle.

Although, all the provided impedance will provide the desired gain, the impedance that has shortest distance to Z_0 will have the widest bandwidth because the matching network will have lower dependence on frequency. To find the optimal impedance, I plotted the points on rectangular chart and chose the lowest point.

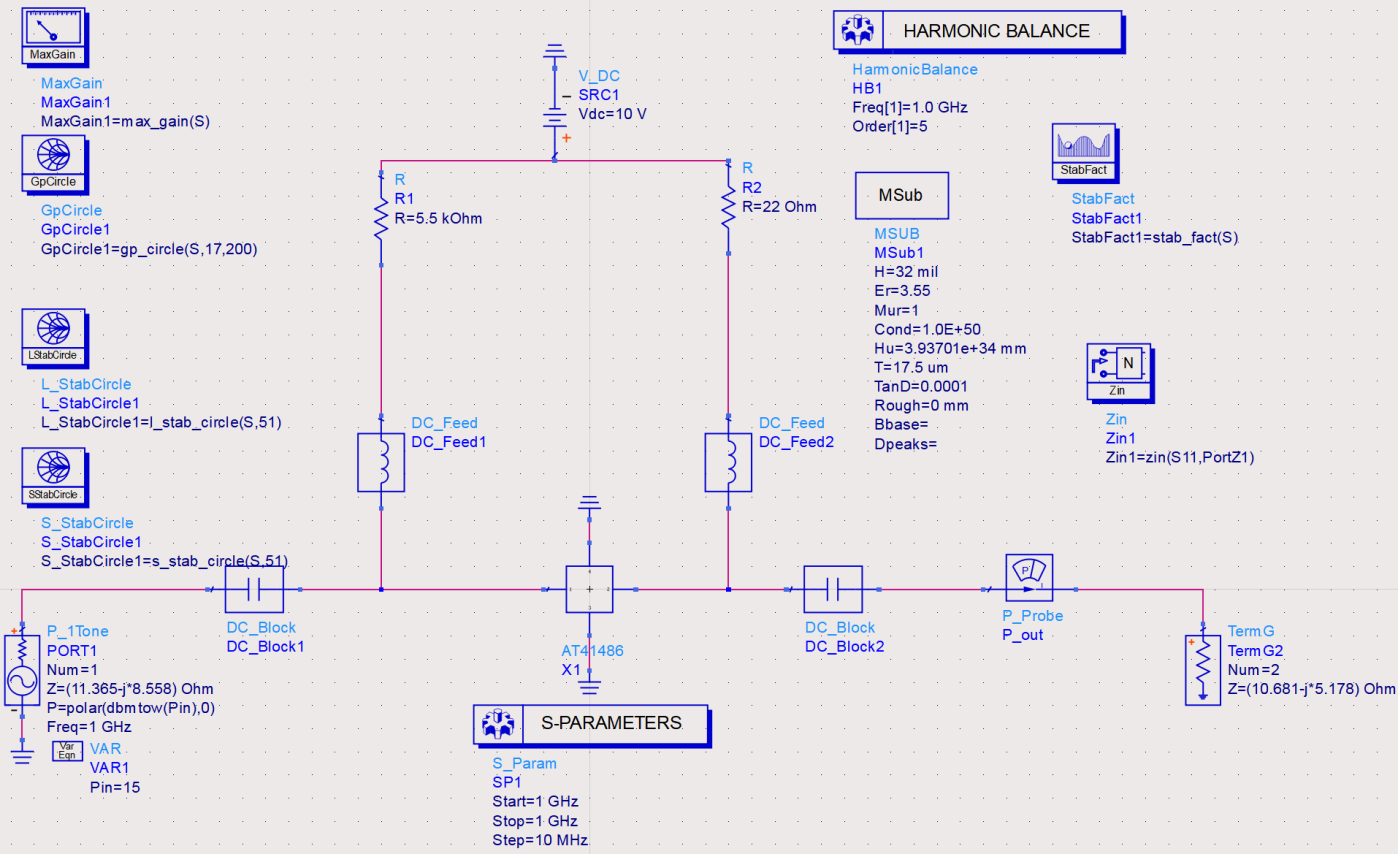


12 dB Gain Circle points vs $|\Gamma_S|$

Therefore, the desired load impedance should be, $Z_L = 10.681 - j5.178\ \Omega$.

2.6 Schematic Simulation with Specific Gain

In this section we will verify the specific gain by providing an ideal source and ideal load impedances to the network. The matching network design will be discussed in the following section. We can simulate the source matching network with P_1Tone power source component in ADS and the load impedances with a TermG component in ADS.



Simulated Schematic with Ideal Impedances

2.8 P1dB Compression Point

The P1dB compression point can be determined by plotting the power output with respect to the power input, from that plot, we can determine the best fit line from the simulated gain. The P1dB is determined at the point which the extrapolated gain is 1 dB higher than the simulated gain. At this point the power amplifer can no longer provide the desired amplification and also is no longer linear and will start introducing distoration to the input RF signal. If the input signal goes beyond the P1dB compression point by a sufficient margin, this could damage the PA.

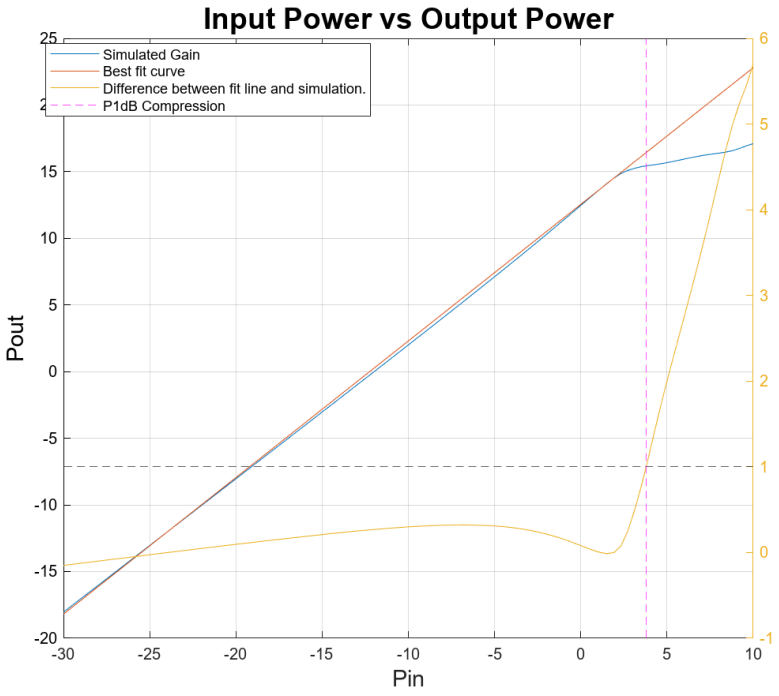
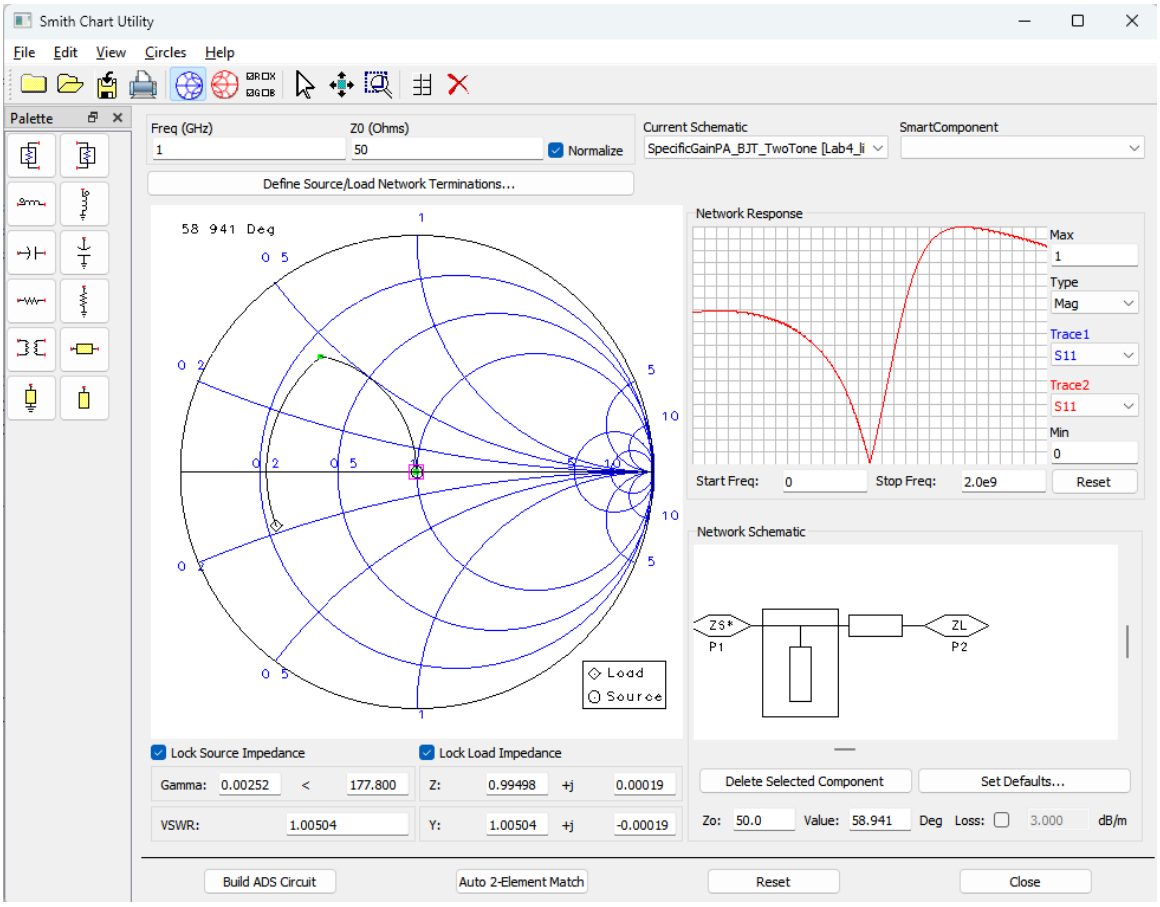


Figure 21: Input Power vs Output Power

3.0 Matching Network Synthesis

Ideal Distributed Element Matching

For ideal distributed element matching, we will use the Smith Chart Utility provided by ADS. It is important to configure the Smith Chart Tool correctly to obtain correct results.



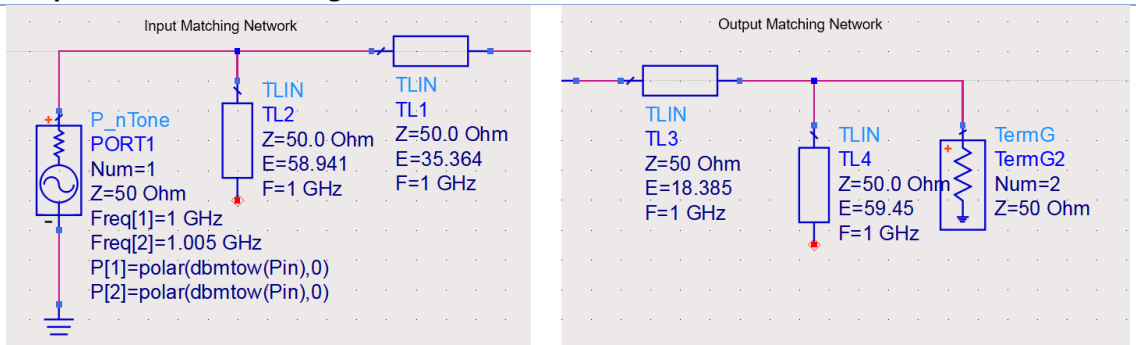
Source Matching Network

From the Smith Chart Tool, we can determine that transmission line properties:

Transmission Line Impedance	**50 Ω**
Series Stub Electrical Length	**35.364**
Open Stub Electrical Length	**58.941**

The same can be done for the load impedance matching network, the following are the transmission line properties:

Transmission Line Impedance	**50 Ω**
Series Stub Electrical Length	**18.385**
Open Stub Electrical Length	**59.450**

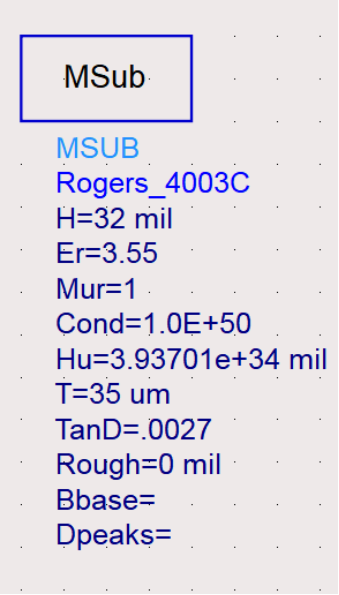


Ideal Matching Networks

Microstrip Matching Network

The matching is almost perfect when using ideal TLIN elements, however, it is not possible to physically realize TLIN elements. For this lab, we used microstrip transmission line to realize this matching network.

To incorporate physical microstrip transmission lines in the schematic we must describe the substrate to ADS. In the microwave laboratory we used Roger's 4003C substrate and configured ADS substrate in the following manner.



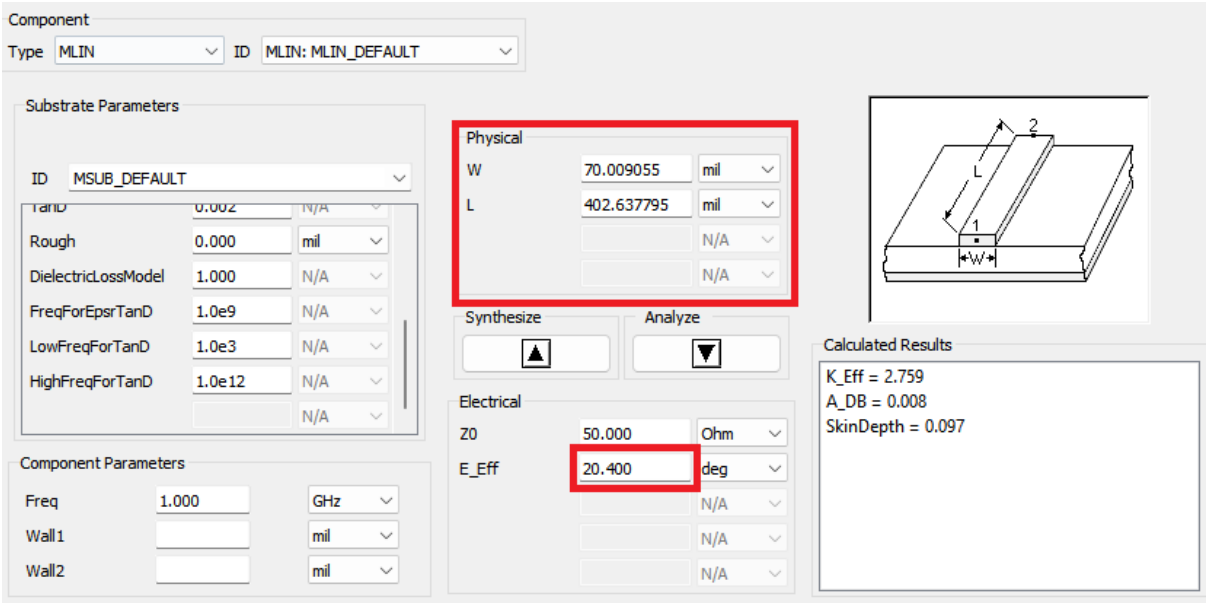
Substrate Configuration

To convert the electrical length of the TLIN to physical length we can utilize the LineCalc tool provided by ADS.

It is important to configure the following properties of the LineCalc before any design parameters are computed.

- Center Frequency, $f_0 = 1\ GHz$
- Relative Permittivity, $\epsilon_r = 3.55$
- Substrate Height, $H = 32$ mil
- Copper Thickness, $T = 35\ \mu m$
- Loss Tangent, $TanD = 0.0027$
- Characteristic Impedance, $Z_0 = 50\ \Omega$

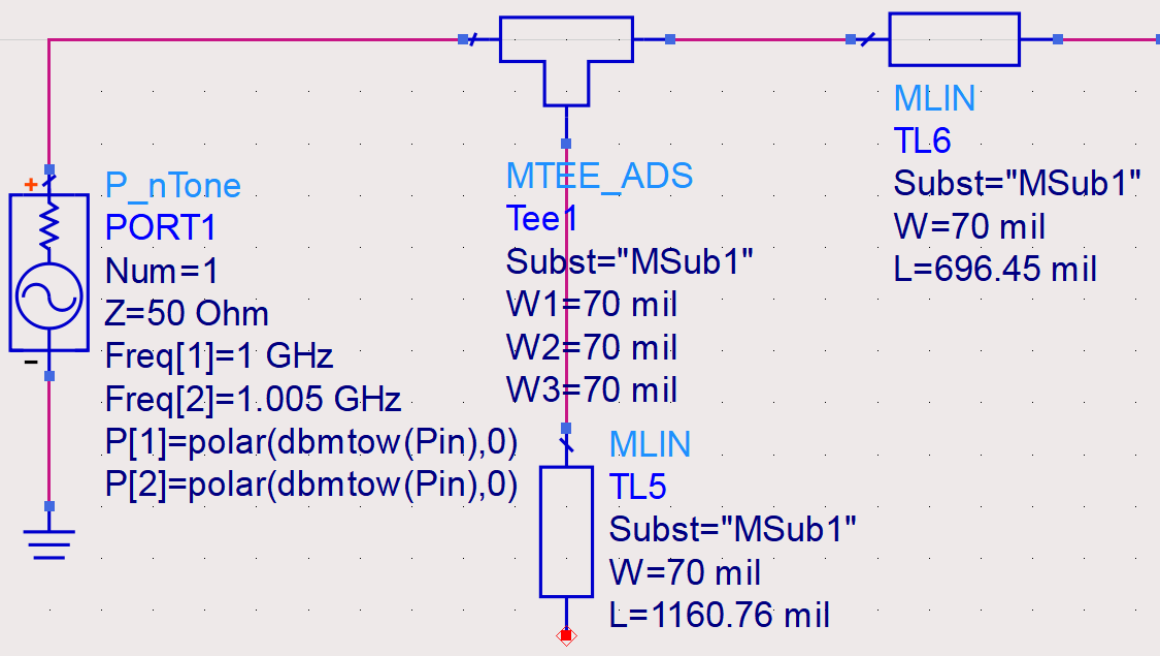
The values used above are the characteristics of Roger's 4003C substrate they will be different for other materials. After the initial configuration, we can use the electrical length from the TLIN example to compute the physical dimensions of the microstrip transmission line.



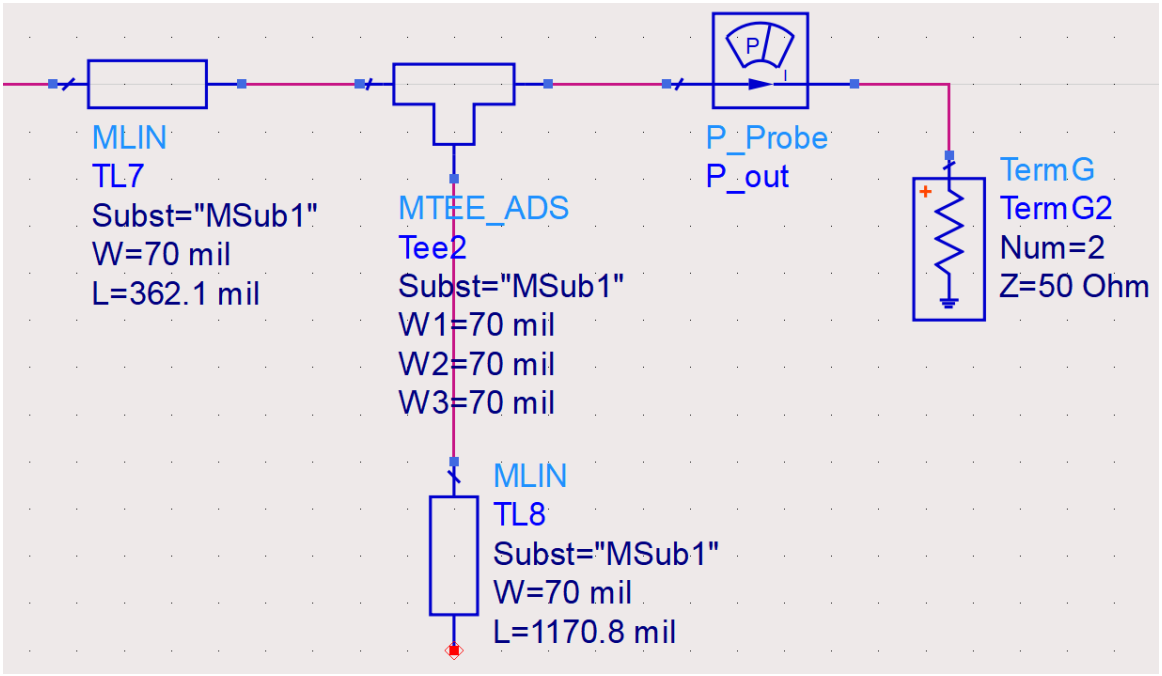
Microstrip Line Design using LineCalc Tool

The illustration above shows how to design the microstrip line using the LineCalc Tool. The input parameters are Z_0 and the effective electrical length and the output values are the physical width and length of the microstrip line. Using these computed values, we can generate the schematic for the matching network using the microstrip transmission line.

A more accurate schematic is to include a T-junction to connect both MLIN elements because it is not possible to connect both MLIN elements at one point on a physical circuit.



Input Matching Network using Microstrip Lines



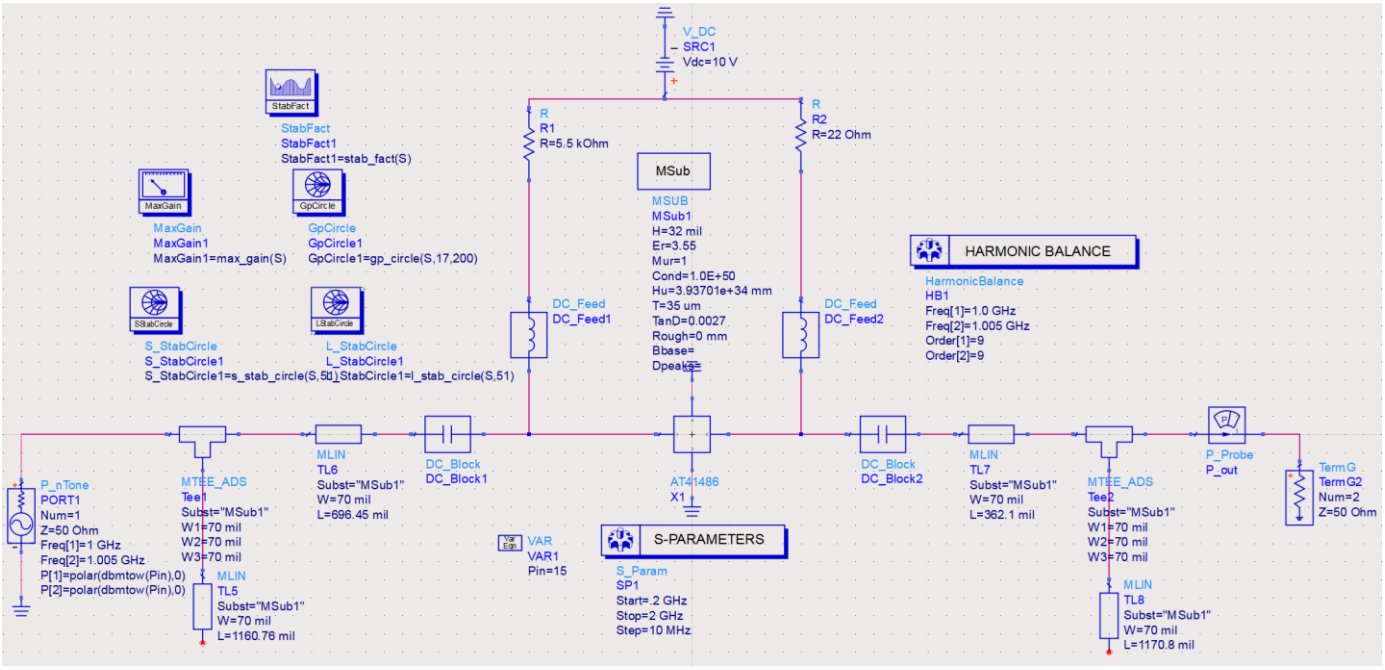
Output Matching Network Using Microstrip Lines

Input Matching Network Dimensions

Transmission Line Impedance	**50 Ω**
Series Stub Electrical Length	**696.45 mil**
Open Stub Electrical Length	**1160.76 mil**

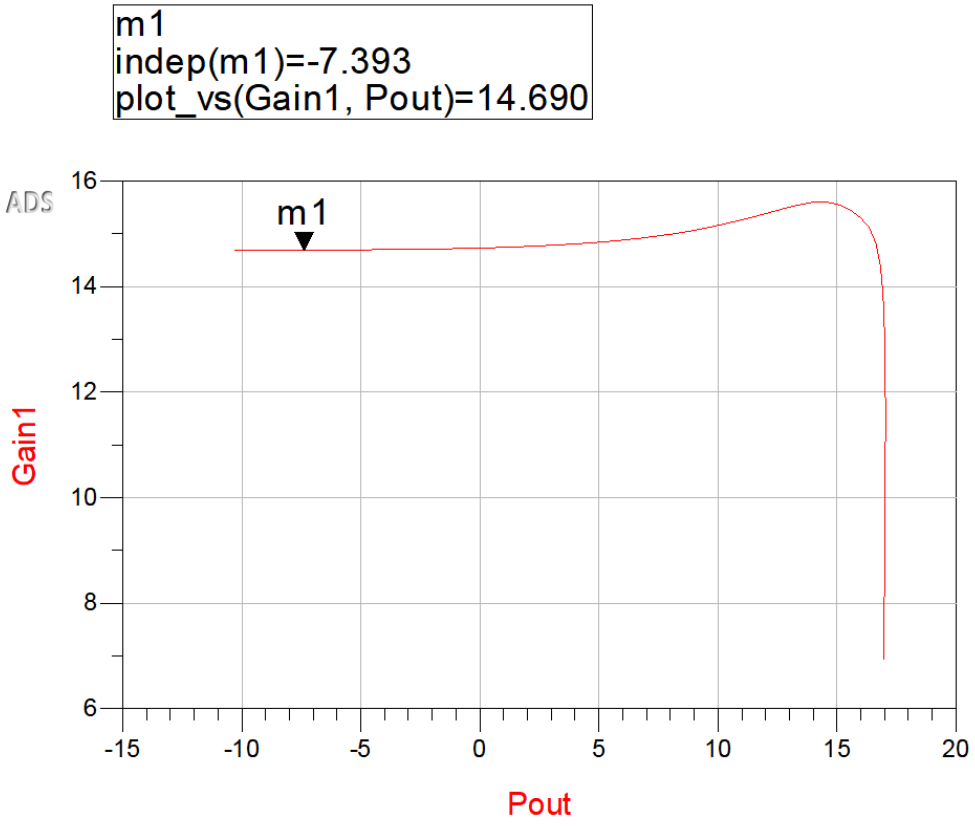
Output Matching Network Dimensions

Transmission Line Impedance	**50 Ω**
Series Stub Electrical Length	**362.1 mil**
Open Stub Electrical Length	**1170.8 mil**

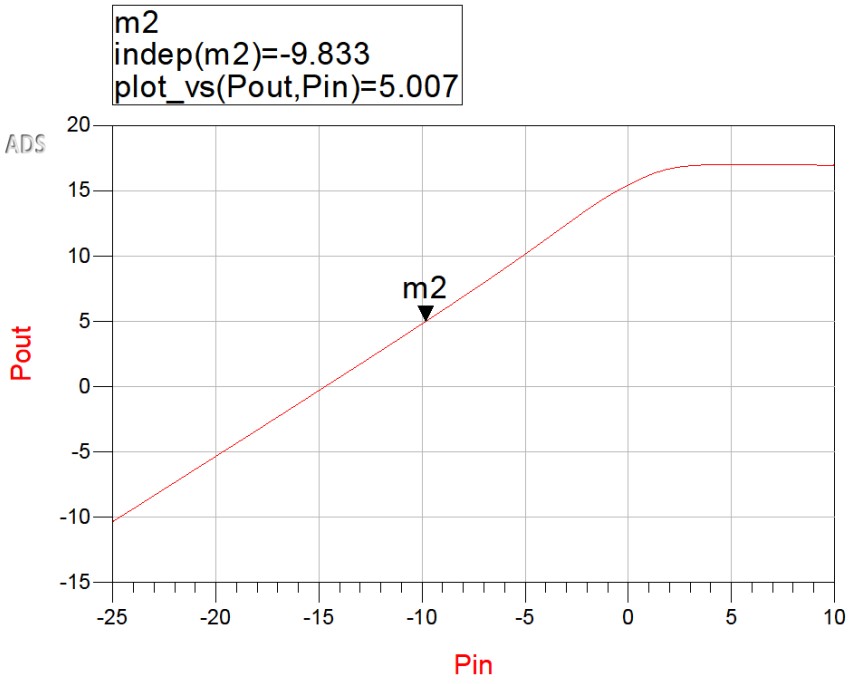


Power Amplifier Schematic w/ MLIN Matching Networks

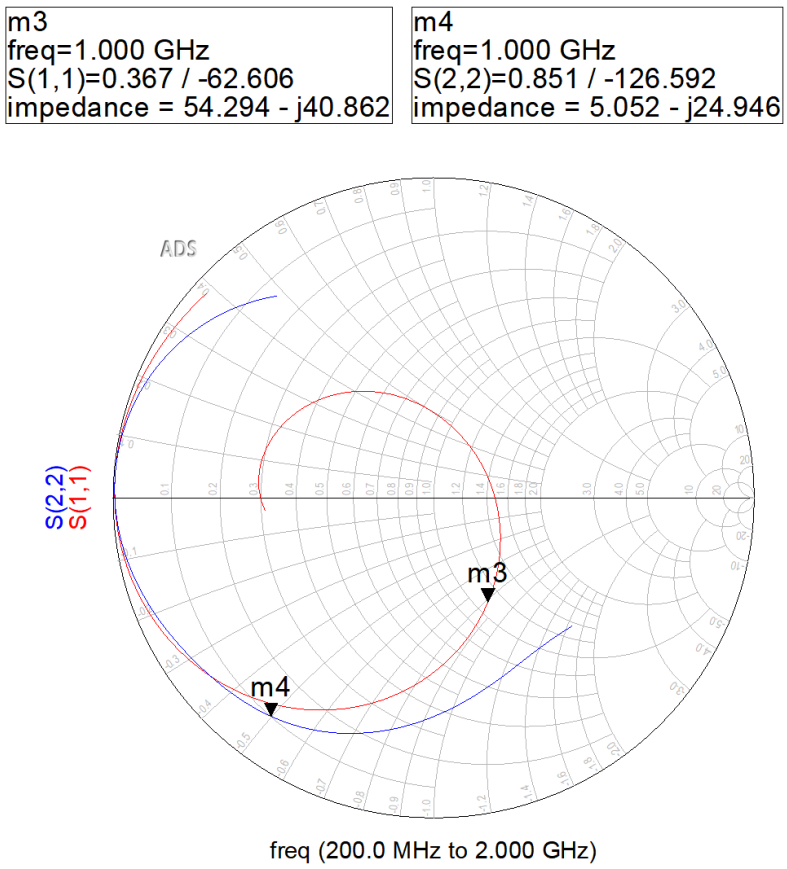
3.2 Scattering Parameter Characterization of Schematic Design w/ MLIN Matching Networks



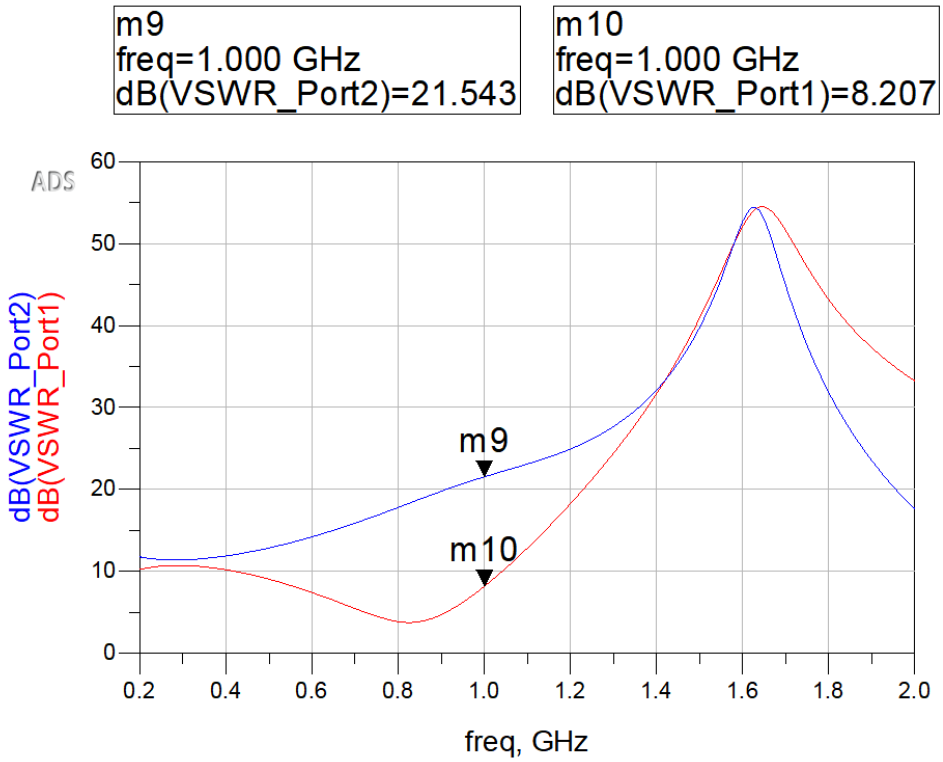
Gain Plot of Schematic w/ MLIN Matching



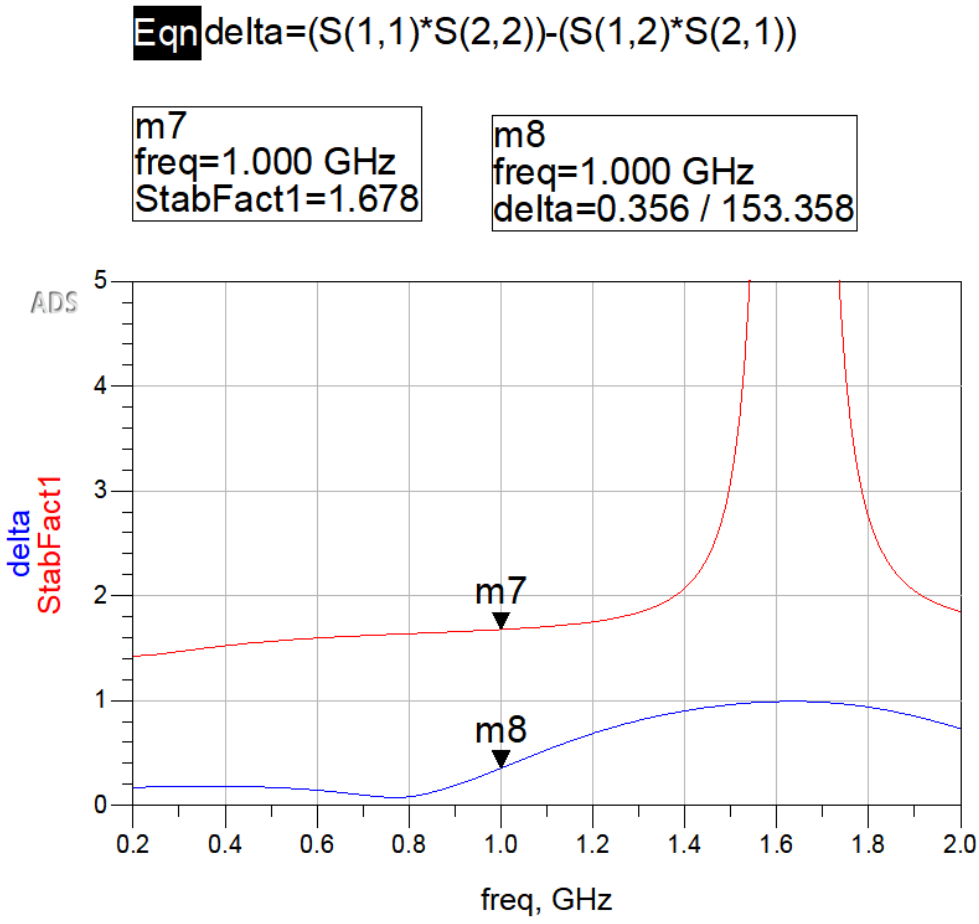
Input Power and Output Power for Schematic w/ MLIN Matching Network



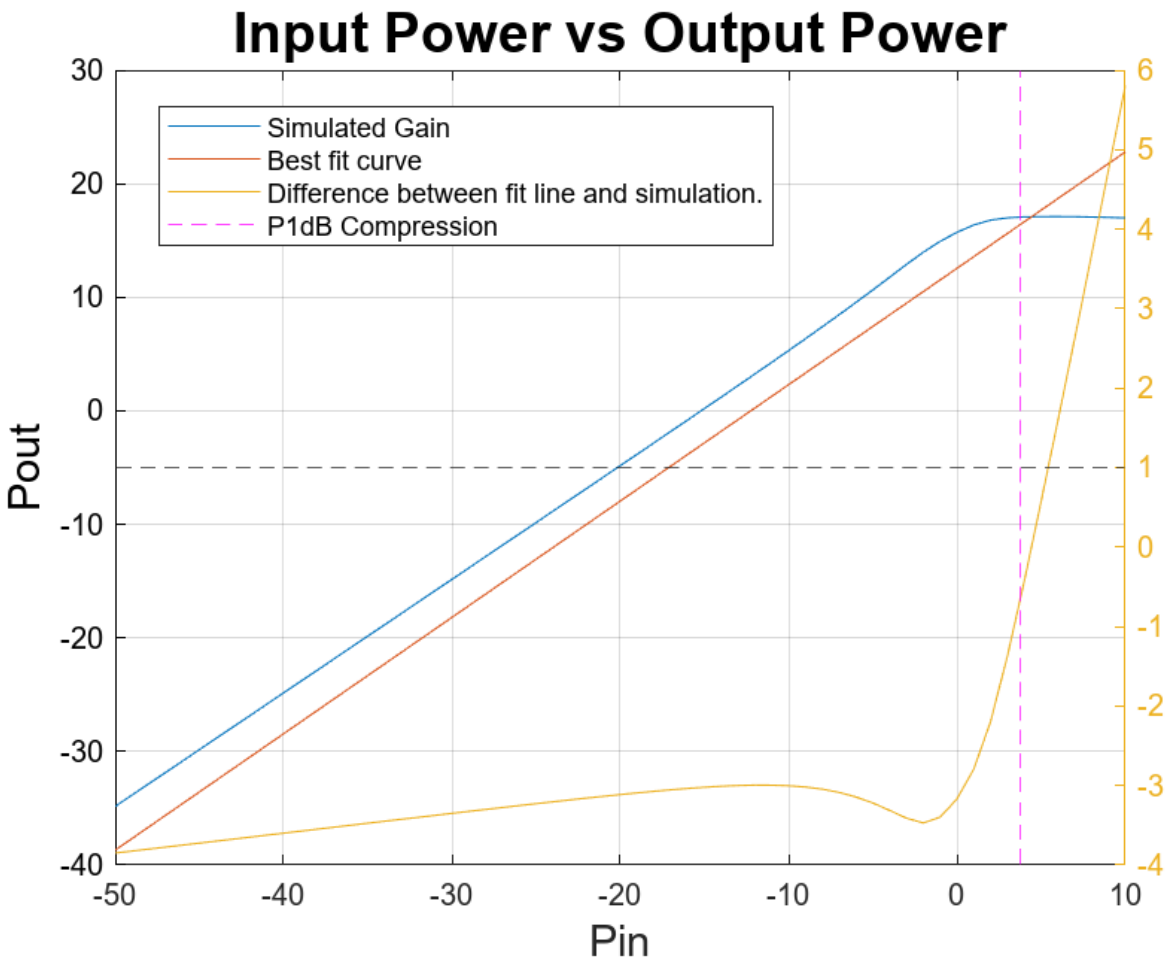
S11 and S22 (including port impedance) w/ MLIN Matching Network



VSWR of Input and Output Port of Schematic w/ MLIN Matching Network

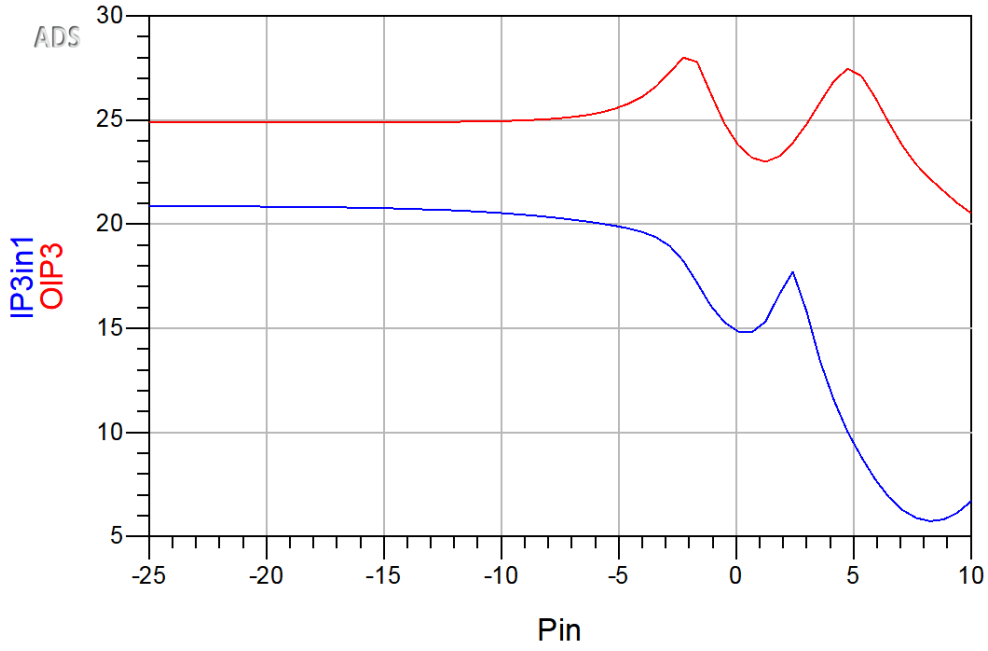


Stability Factor of Schematic w/ MLIN Matching Network

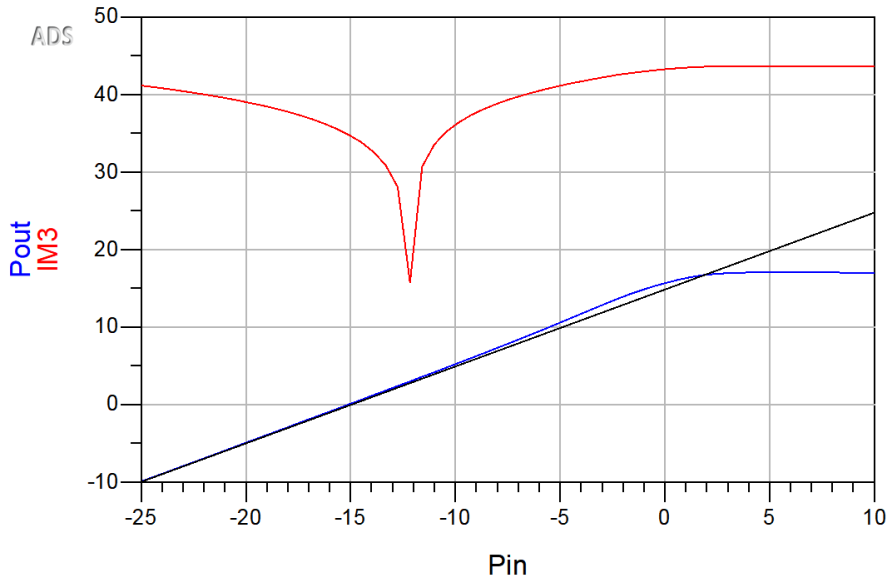


P1dB Compression for Schematic w/ MLIN Matching Network; P1dB=17.1dB

Eqn OIP3=max2(OIP3_Lower,OIP3_Upper)



IP3 and OIP3 of Schematic



IM3 Plot

Eqn OIP3=max2(OIP3_Lower,OIP3_Upper)

Eqn Pout=wtodbm(P_out.p[4]+P_out.p[5])

Eqn IM3_LL=wtodbm(P_out.p[3]-(Pout-3))

Eqn IM3_HH=wtodbm(P_out.p[6]-(Pout-3))

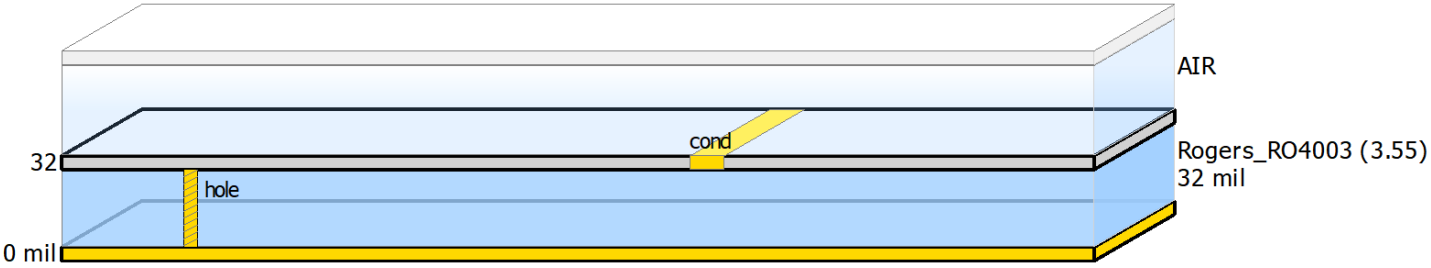
Eqn IM3=max2(IM3_LL,IM3_HH)

Eqn Gain1=Pout-Pin

Plot Equations

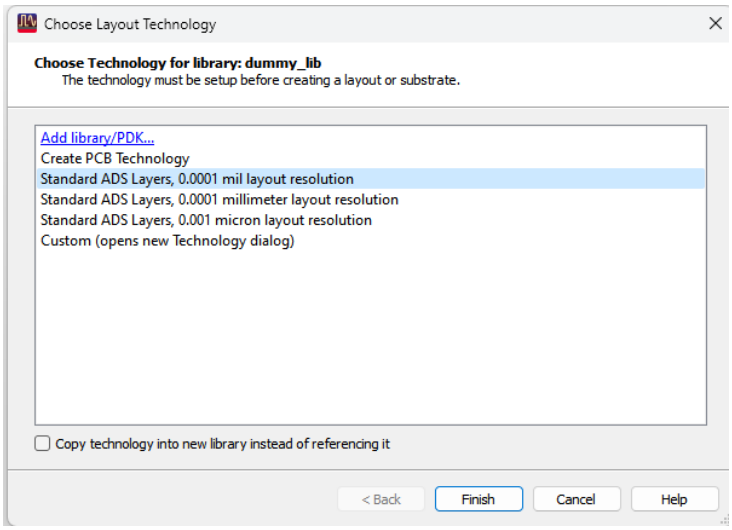
3.4 Realized Layout of Small Signal PA

Before we can design the PA layout, we must first describe the substrate material to ADS, for this design, we will be using the Roger's 4003C substrate material.



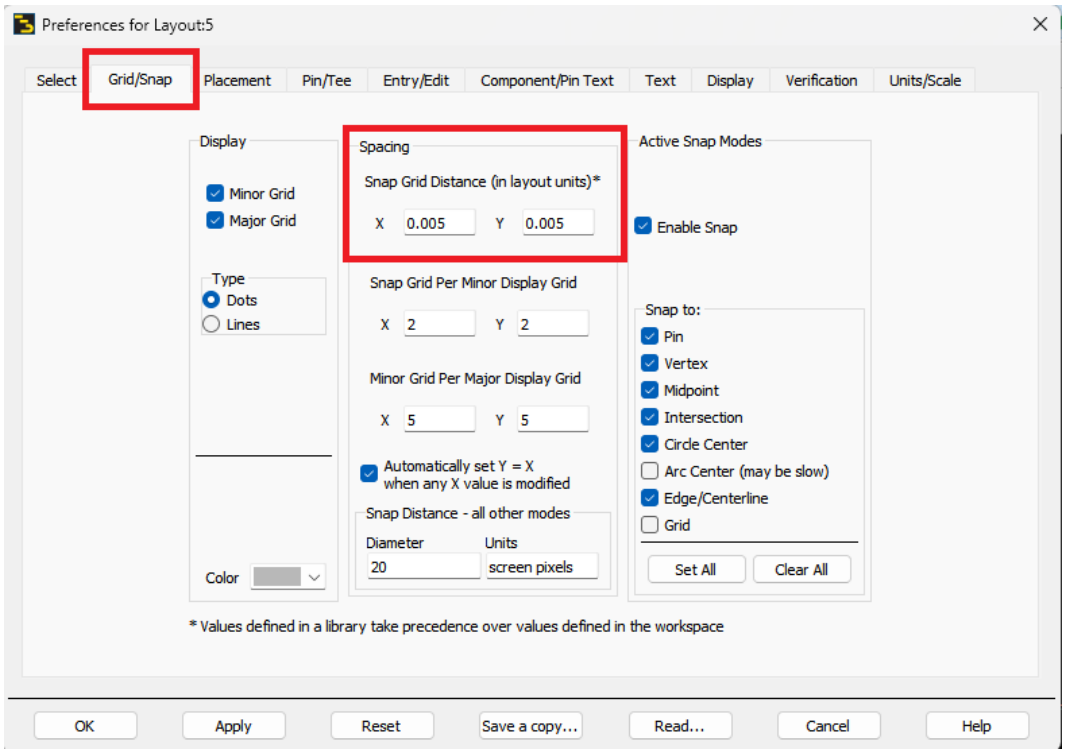
Layout Substrate Material

Additional configuration is required before the layout design process begins. First, we must choose the correct PCB technology.



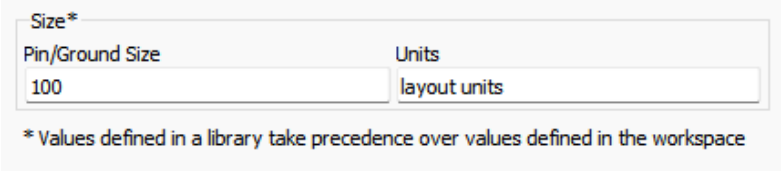
PCB Technology (0.0001 mil layout resolution)

For precision when placing traces and port pins, it is optimal to change the layout grid resolution to a lower value as shown in the following illustration.



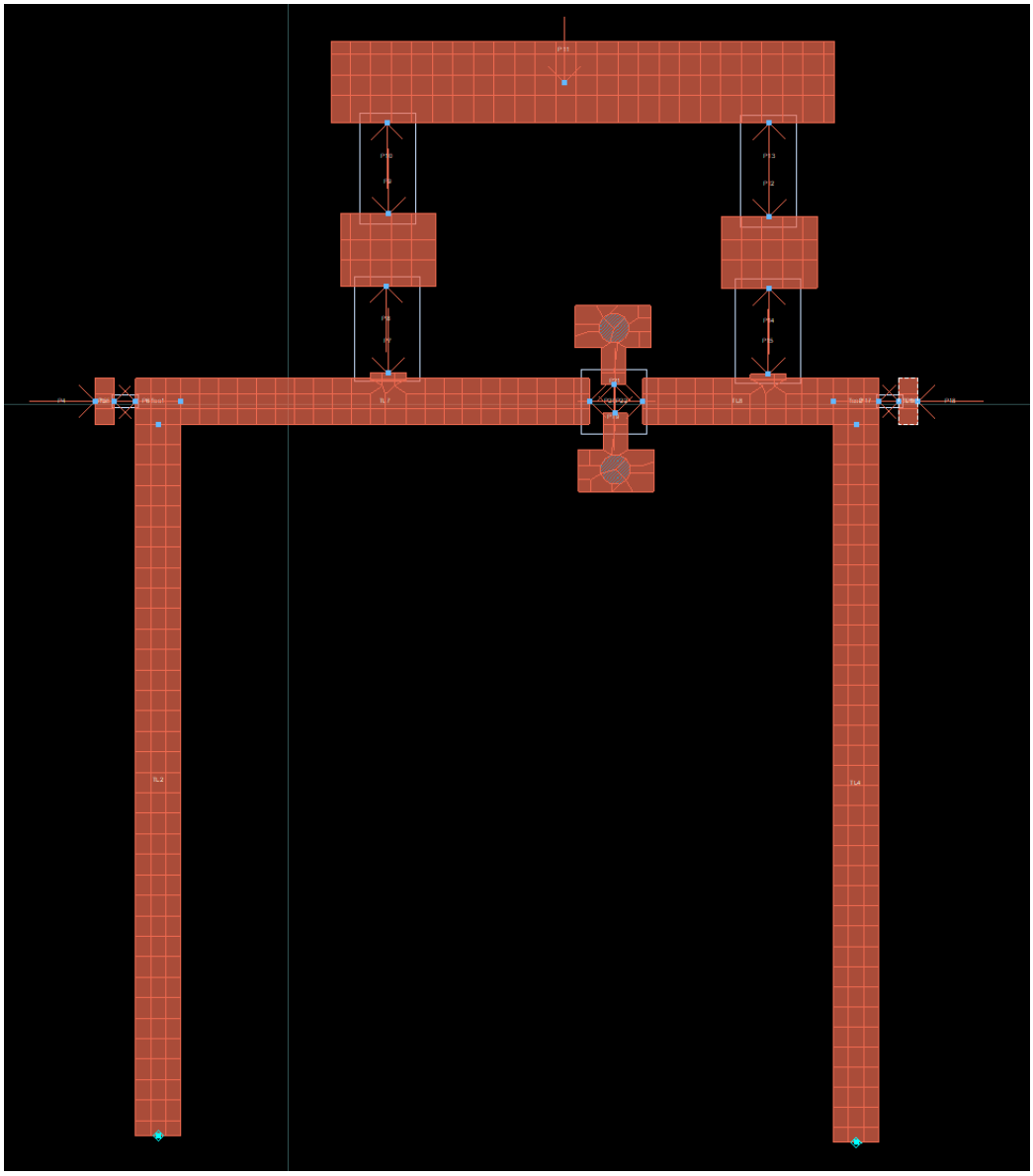
Grid Configuration

Also, under Pin/Tree tab, increase the size of the Pin to 100 mil for ease of use.

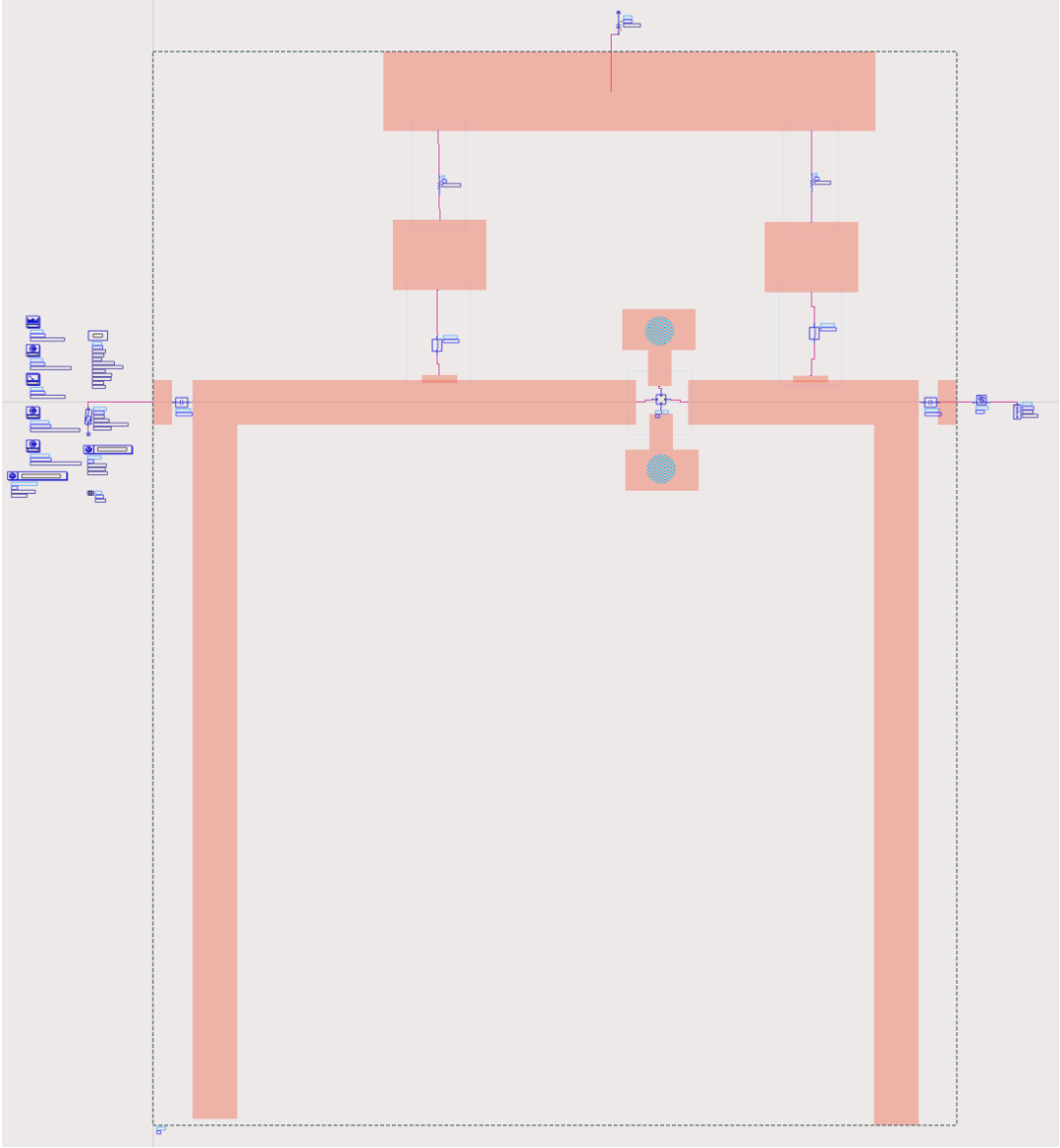


Pin Size

The empty rectangular shapes are placeholders for the lumped element components, it is important to ensure that the dimensions are accurate, otherwise, when fabrication is done, the components will not correctly align. When connecting the MLIN to the lumped elements, make sure to provide some overlap for good electrical connections.

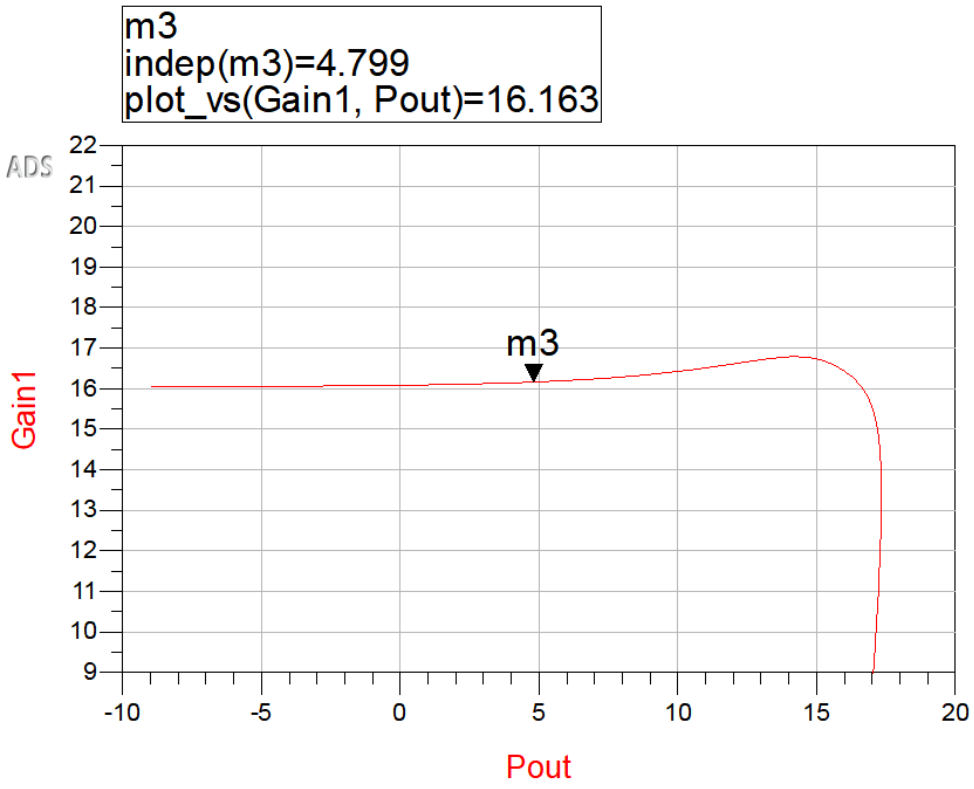


PA Layout Design w/ Port Placement

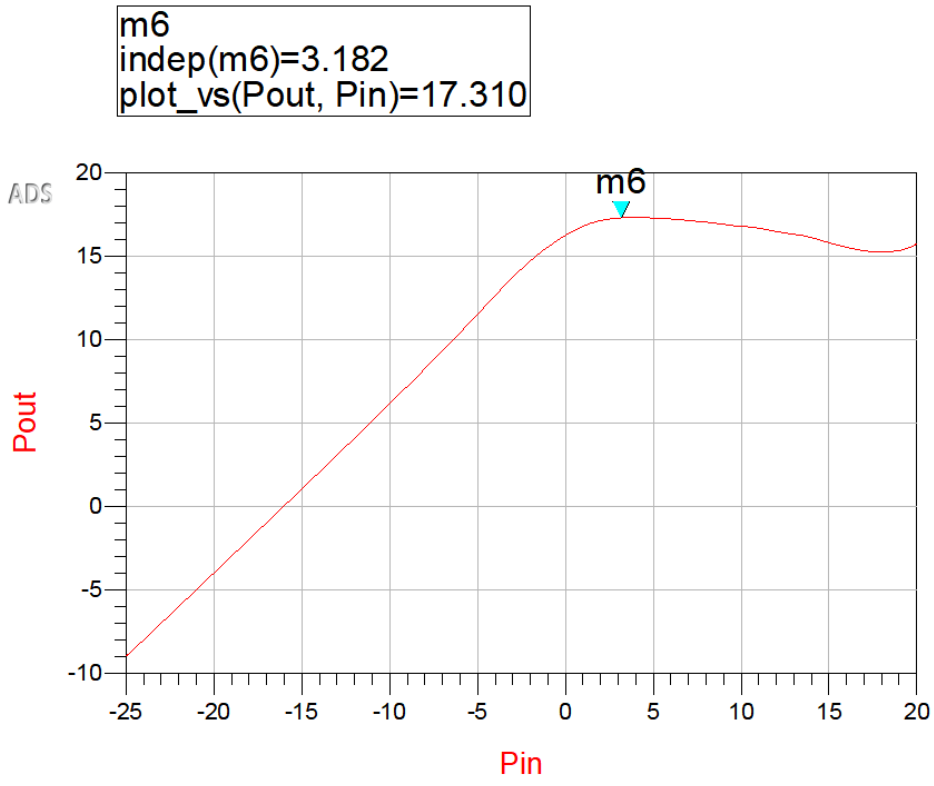


Integrated Layout Model w/ Schematic

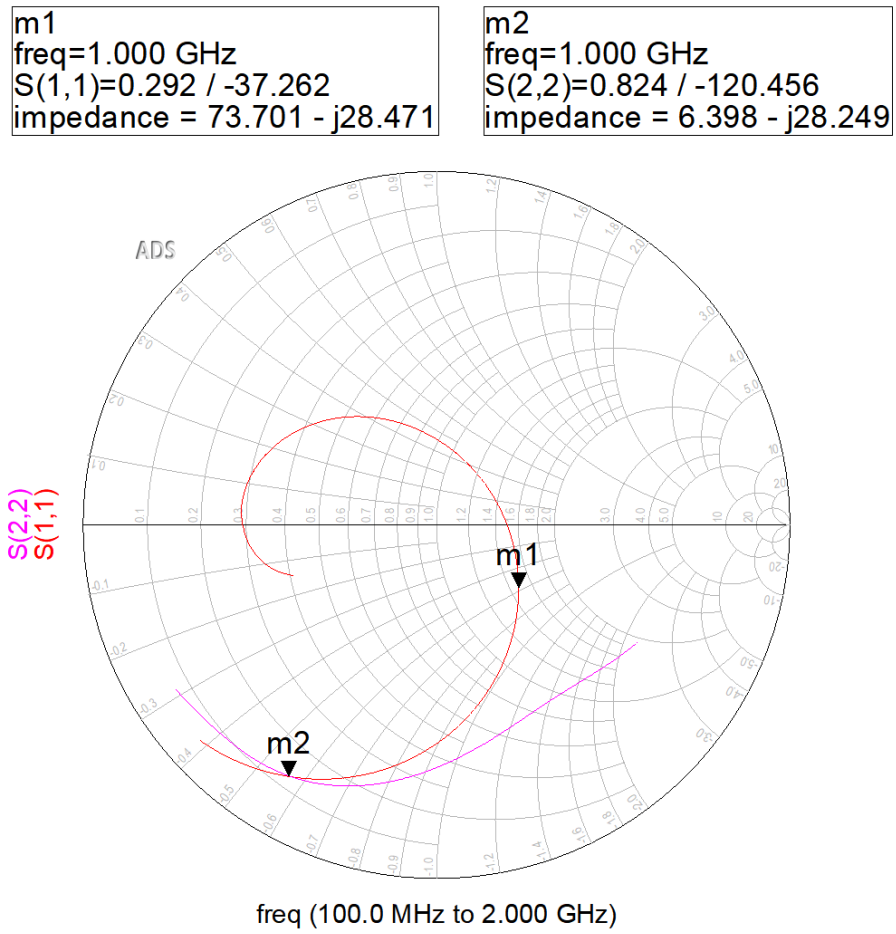
3.6 Physical PA Characteristics and Scattering Parameters using Manufacturer Model



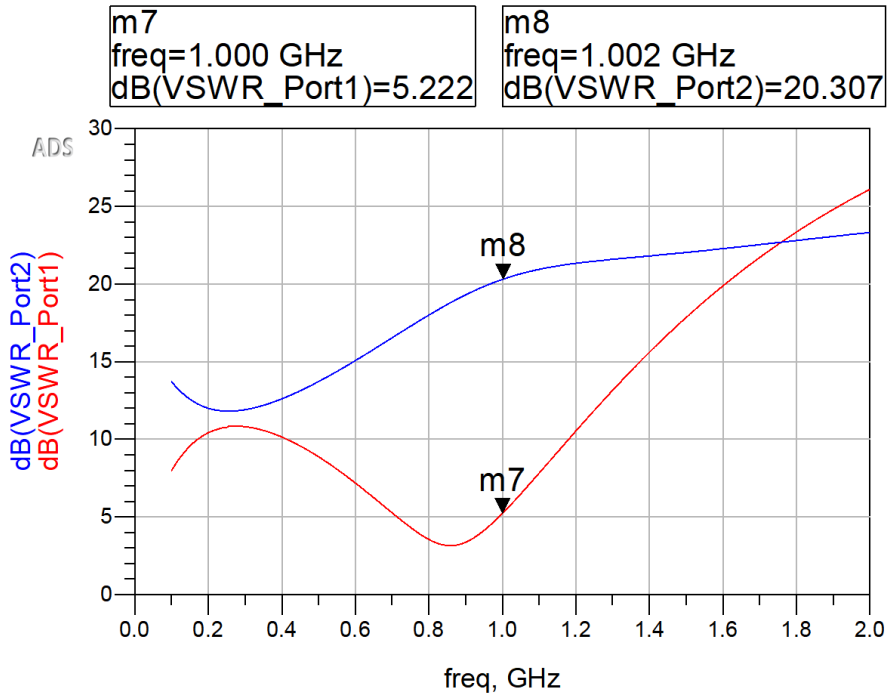
Gain Plot of Layout using Manufacturer Model



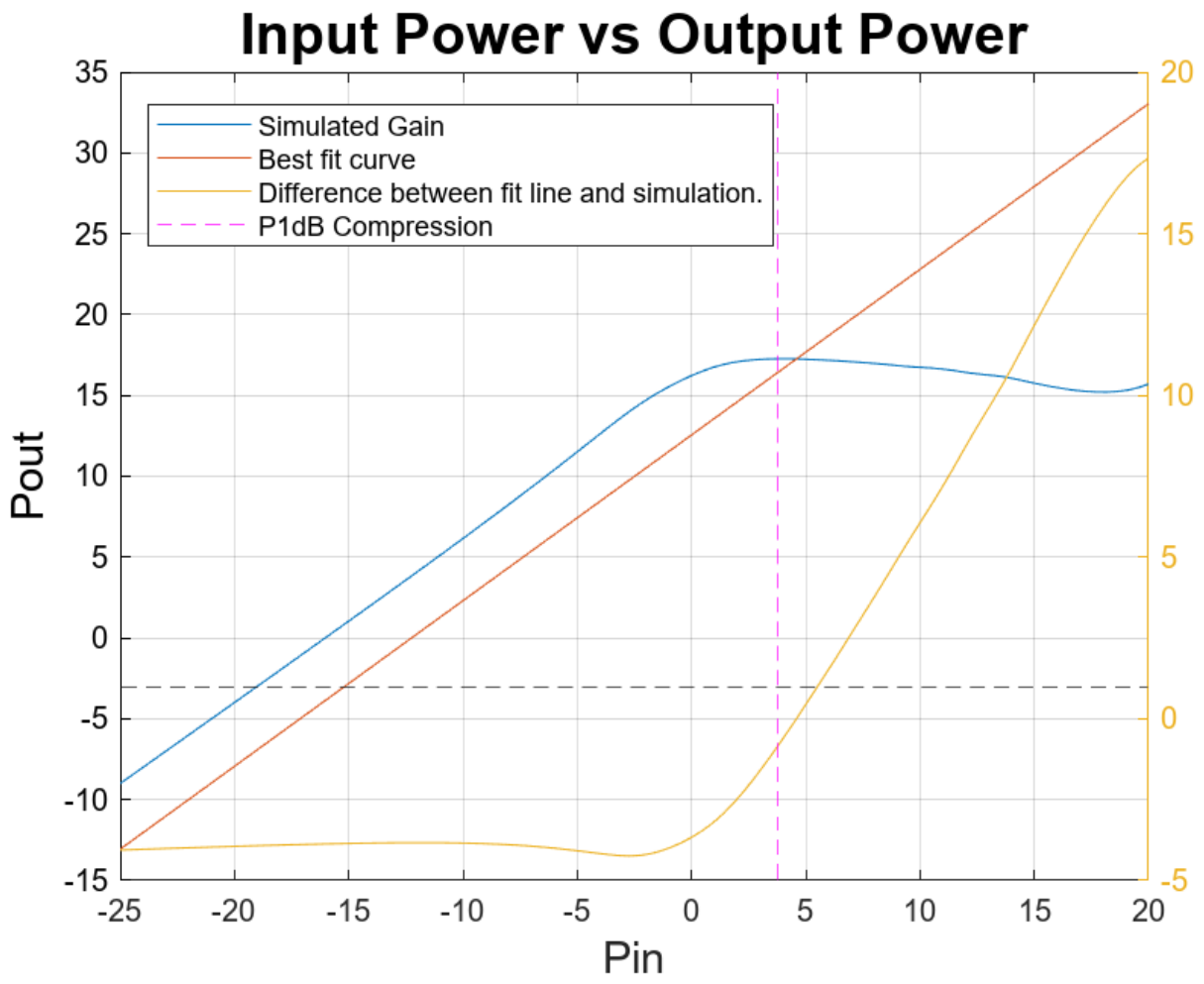
Input Power vs Output Power for Layout using Manufacturer Model



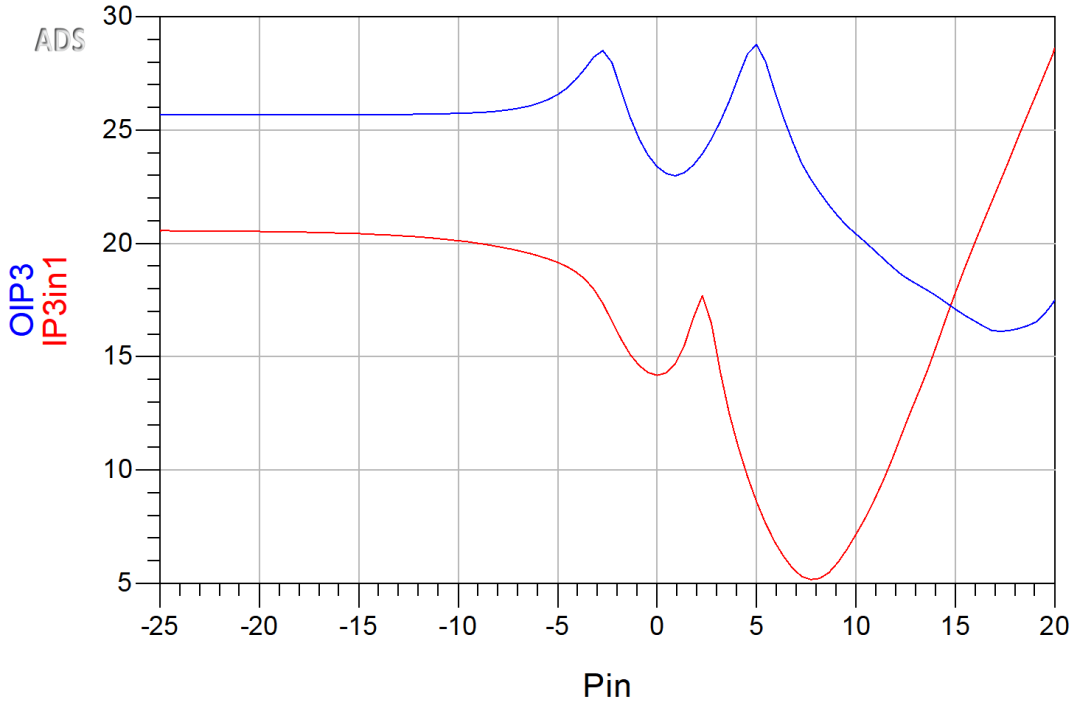
S11 and S22 (including port impedance) for Layout using Manufacturer Model



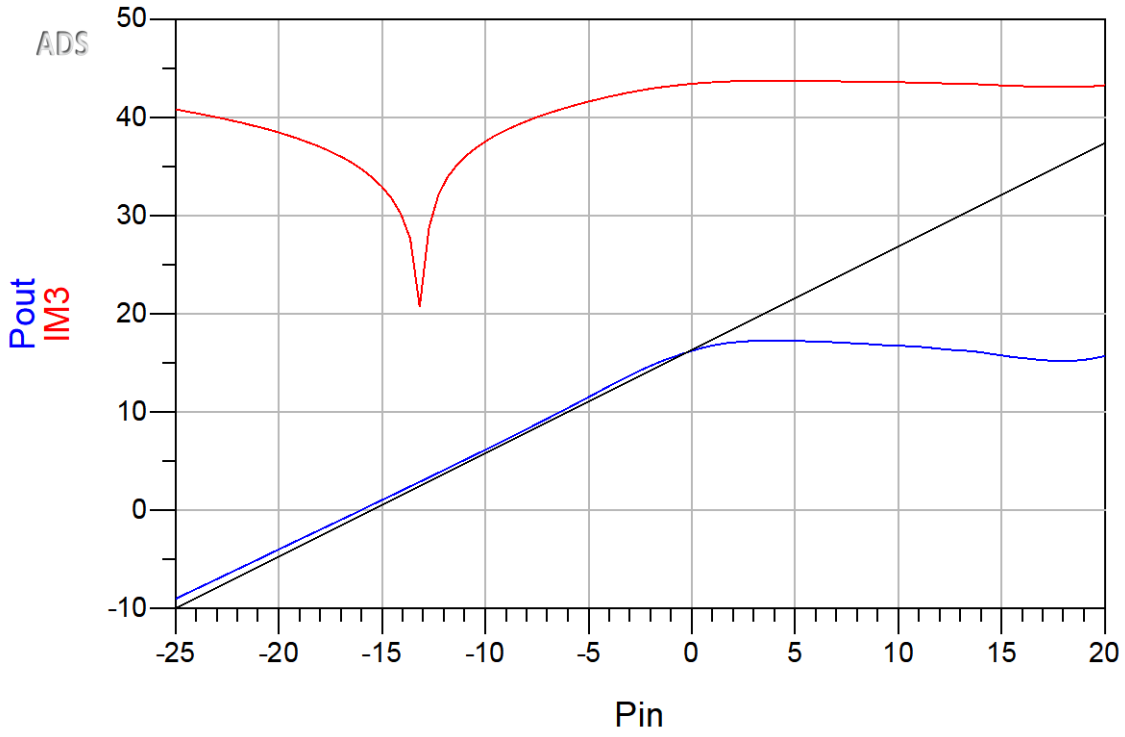
VSWR of Input and Output Port of Layout using Manufacturer Model



P1dB Compression for Layout using Manufacturer Model; P1dB=17.2dB



IP3 and OIP3 of for Layout using Manufacturer Model

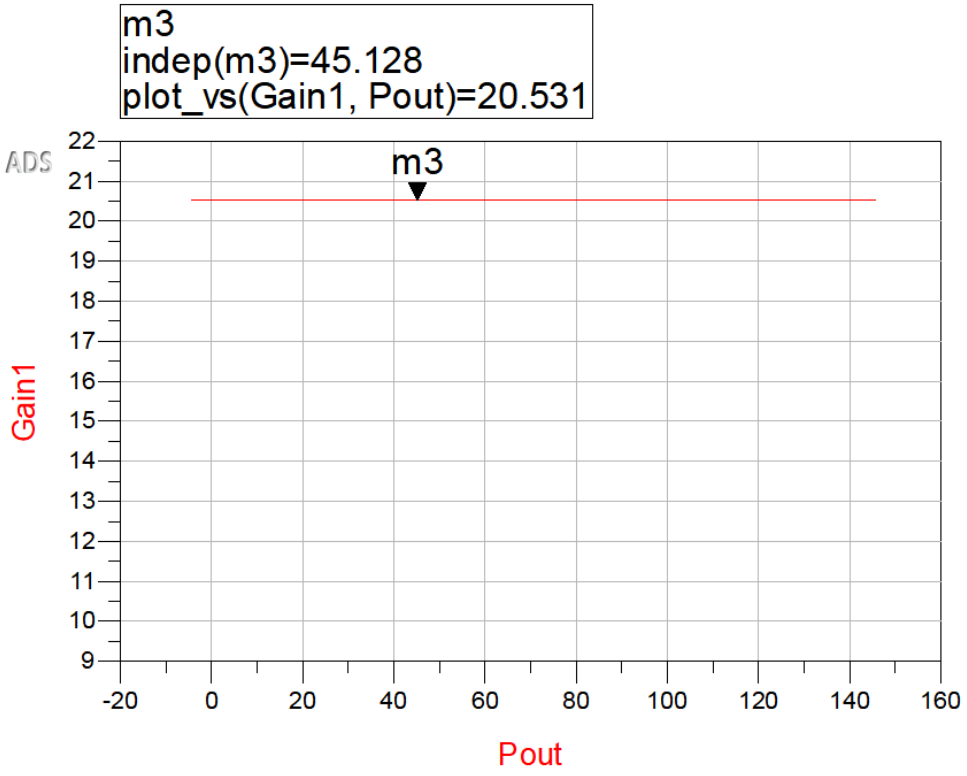


IM3 Plot

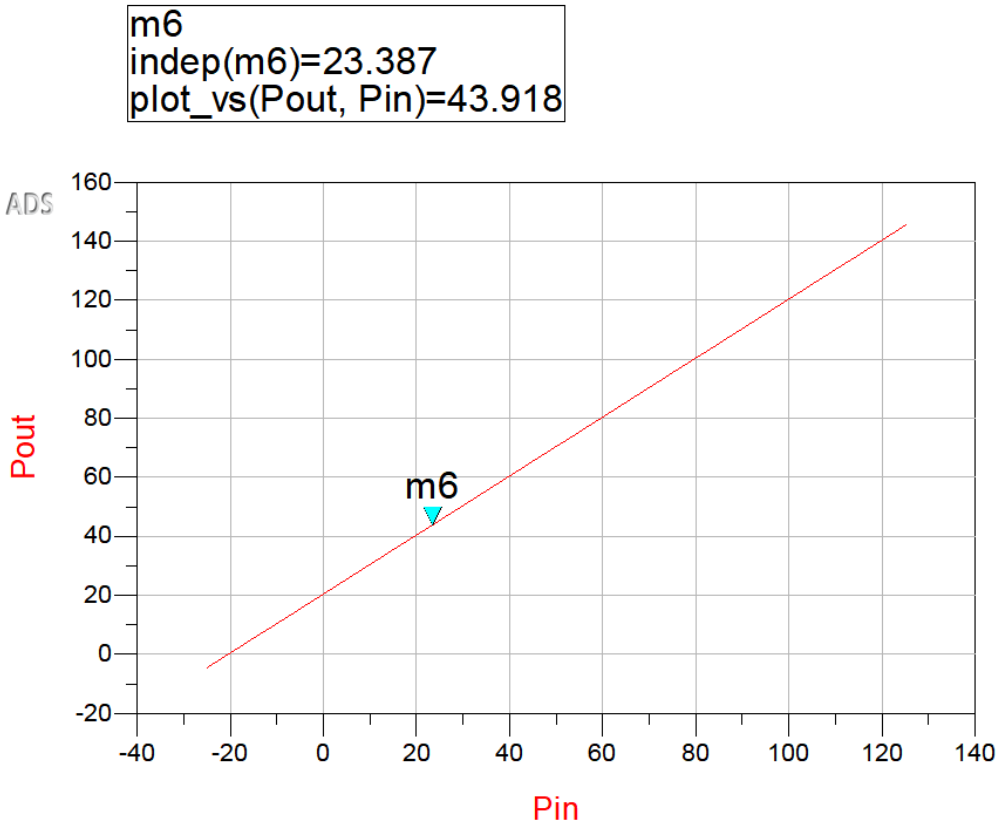
```
Eqn delta=(S(1,1)*S(2,2))-(S(1,2)*S(2,1))

Eqn OIP3=max2(OIP3_Lower,OIP3_Upper)

Eqn Pout=wtodbm(P_out.p[4]+P_out.p[5])

Eqn IM3_LL=wtodbm(P_out.p[3]-(Pout-3))

Eqn IM3_HH=wtodbm(P_out.p[6]-(Pout-3))

Eqn IM3=max2(IM3_LL,IM3_HH)

Eqn Gain1=Pout-Pin
```

Plot Equations

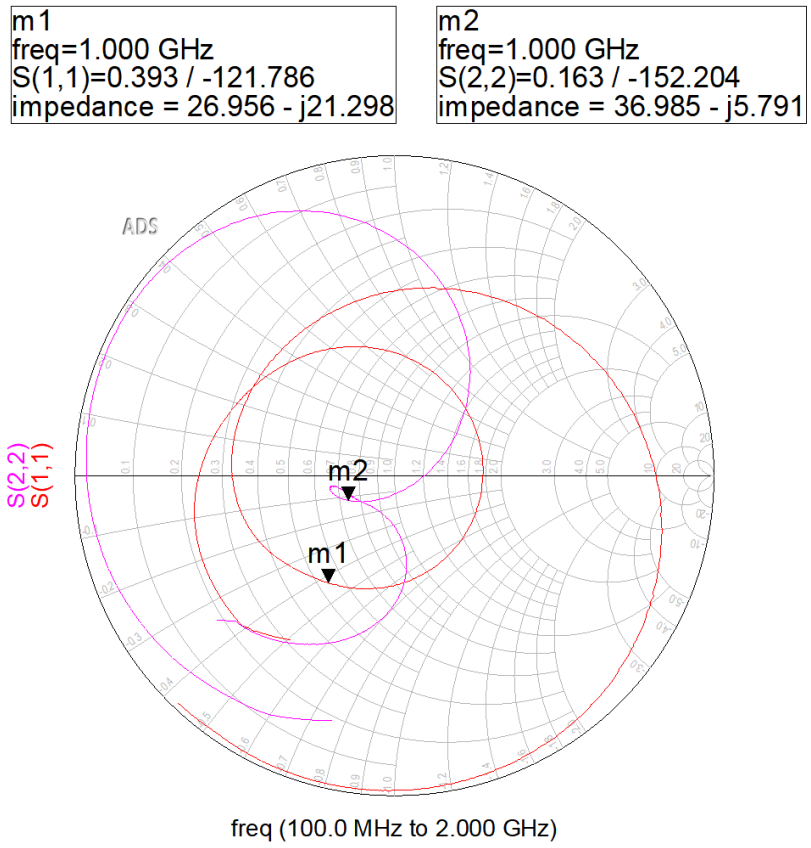
3.8 Physical PA Characteristics and Scattering Parameters using Measured Model



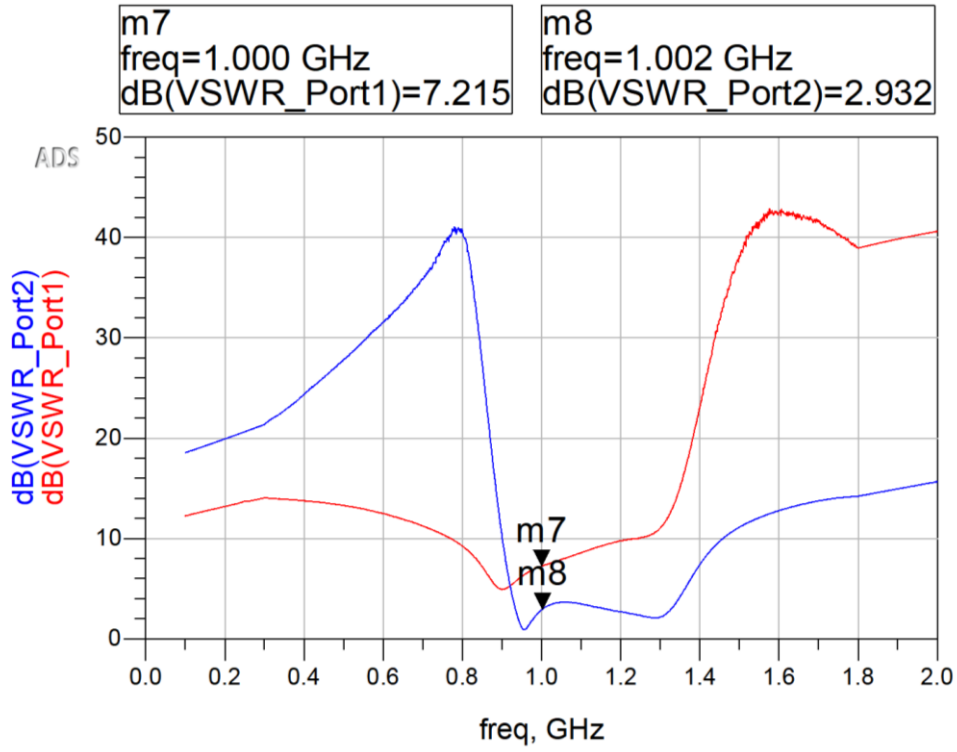
Gain Plot of Layout using Measured Model



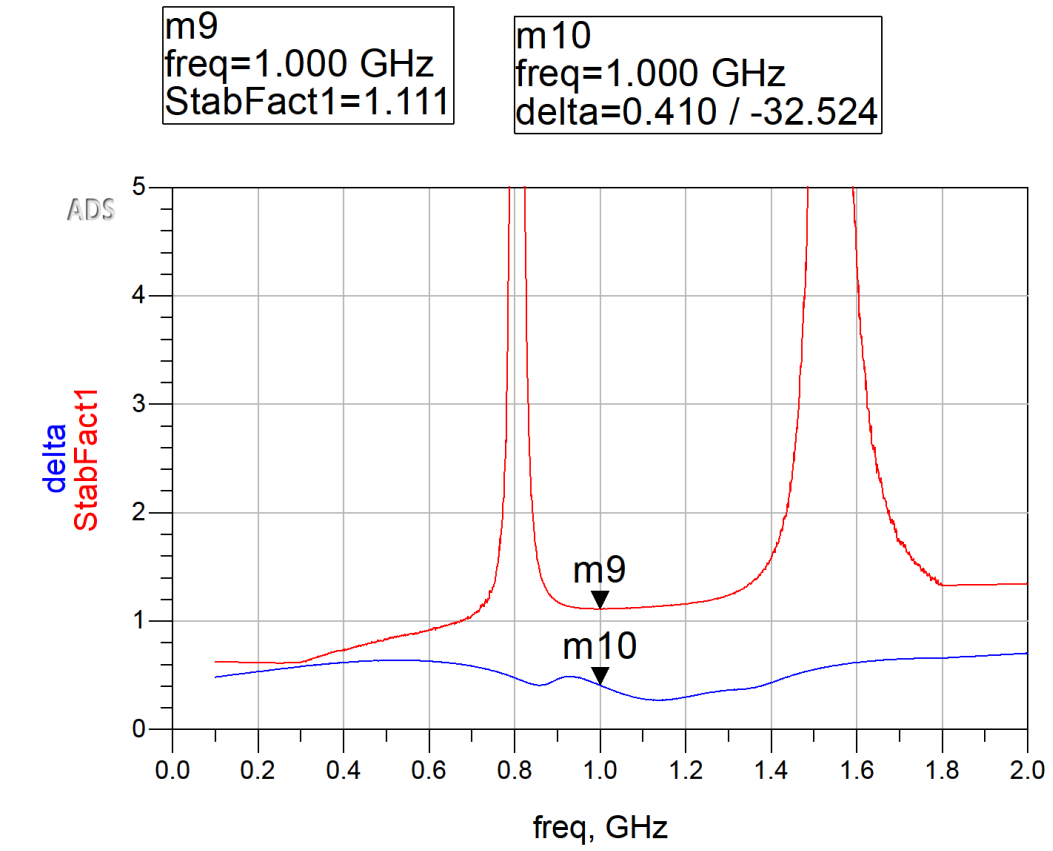
Input Power vs Output Power for Layout using Measured Model



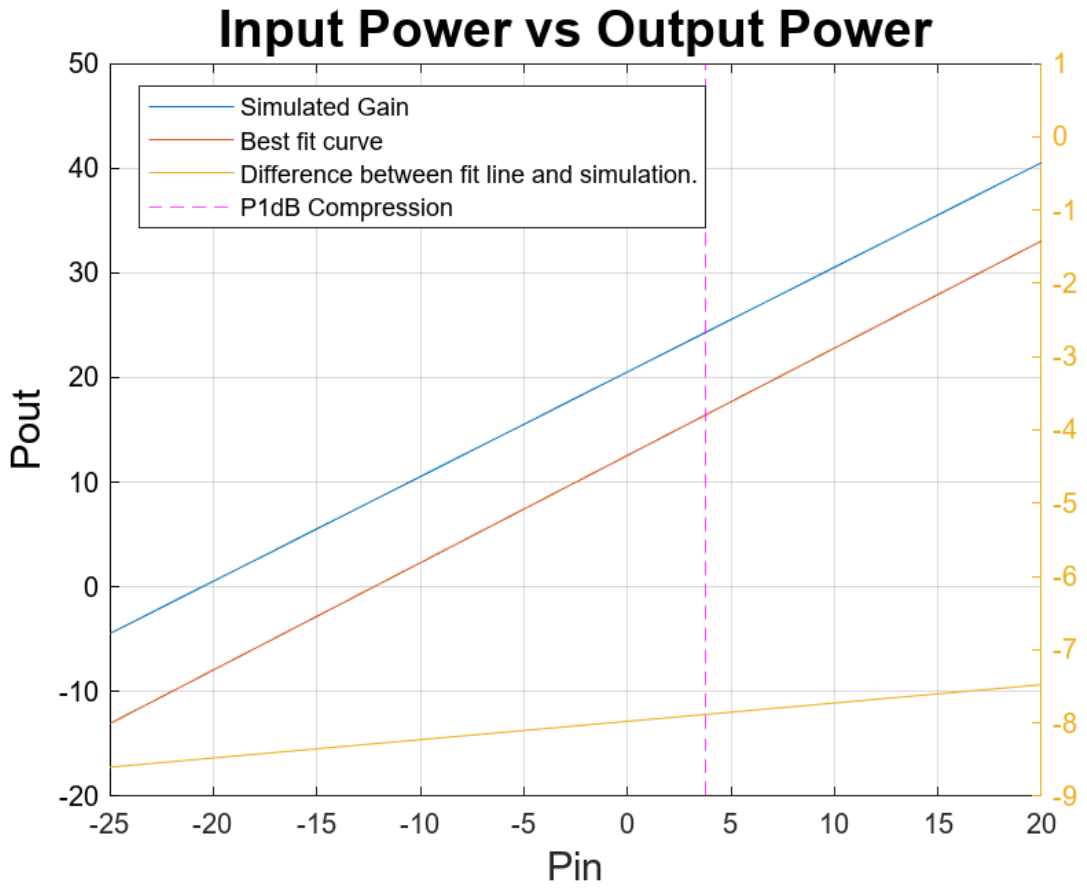
S11 and S22 (including Port Impedance) for Layout using Measured Model



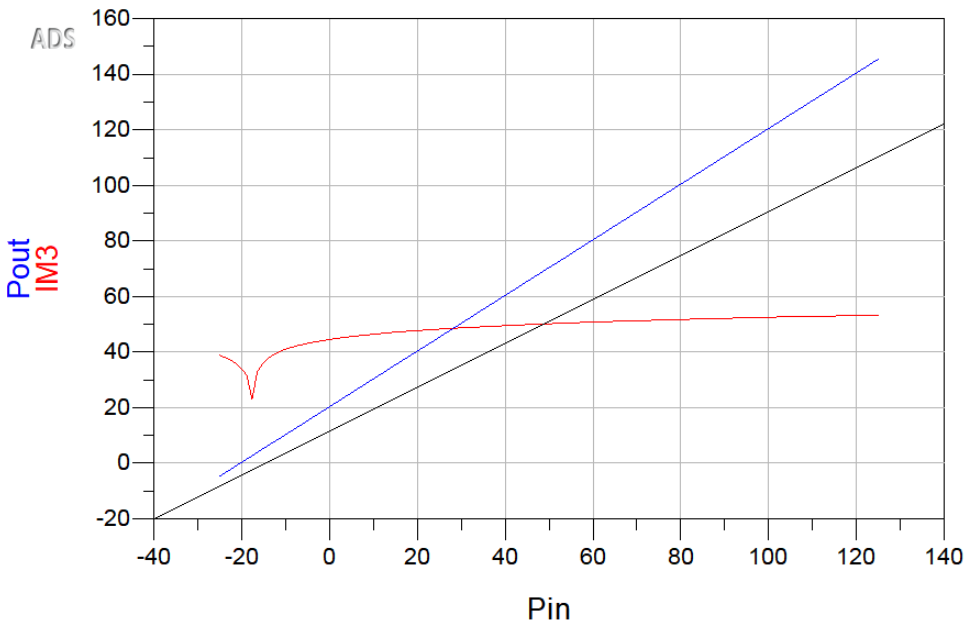
VSWR of Input and Output Port of Layout for Layout using Measured Model



Stability Factor of Layout using Measured Model



P1dB Compression for Layout using Measured Model



IM3 Plot

4.0 Encountered Problems and Issues

1. While I was diagnosing other issues, I accidentally removed the ground via in the substrate which caused simulation issues.

2. I chose the wrong PCB technology which caused simulation issues.

3. I had port connectivity issues which resulted in an S11 of 0 dB, this resulted in negative dB and simulation issues.

4. When designing the matching network, I did not account for the additional length added by MTEE which caused the matching network to drift too much which produced incorrect gain.

5.0 Analysis and Result Comparison

Identify the gain of the amplifier at 1 GHz, compare all cases.

The gain of the amplifier is controlled by the matching network which is the primary reason for deviations. Since, were using microstrip matching networks, the edge effects make the transmission line longer which has provided a better output matching network resulting in higher gain. To achieve the desired gain for the layout, the designer must do another iteration with the goal of optimizing the matching network. Also, the transistor will have variations in impedance due to process variations and temperature fluctuations.

Source	Gain
Schematic w/ Ideal Matching	12 dB
Schematic w/ MLIN Matching	14.7 dB
Layout w/ MLIN Matching	16.16 dB
Layout (Measurement)	20.53 dB

	P1dB	IIP3	OIP3
Schematic w/ MLIN Matching	17.1 dB	25	21
Layout (Manufacturer)	17.2 dB	21	26

6.0 Conclusion

In conclusion, the lab successfully achieved its objective of designing and simulating a microwave amplifier at 1 GHz with a specified gain. Through meticulous schematic design, stability analysis, and matching network synthesis, the amplifier was optimized to meet the desired performance criteria. Despite encountering some challenges such as simulation issues and matching network adjustments, the final amplifier design demonstrated notable improvements in gain and performance when compared across different configurations. The iterative process involved in designing the amplifier underscores the importance of thorough analysis and optimization in achieving desired results. Overall, the lab provided valuable insights into the complexities of RF and microwave circuit design and served as a practical application of theoretical concepts learned in class.