



Final Project Internship

PnR Flow Digital Tx System

Prepared by:

Youssef Mohamed Hatem

Username: asicint25yooahamed

Supervised by:

Eng. Bassant Samir

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0.1 Introduction

This report documents the implementation of the RTL-to-GDS flow for the digital system transmitter RTL, adhering to a comprehensive set of requirements aimed at achieving a fully synthesized design. The process includes synthesis optimization where available, with detailed identification of optimization methods and full synthesis QoR (Quality of Results). A design gate-level netlist schematic is provided, alongside a reasonable floorplan designed for area optimization with suitable utilization. Floorplan snapshots highlight all possible aspects, while detailed documentation covers PnR steps such as place, CTS, and route. The report addresses the cleanup of timing violations, if any, with thorough documentation of the solutions. All requirements, including careful implementation, clear reporting, and understandable documentation, are met, with paths to work areas, scripts, and reports included for reference. In modern digital design, the process of synthesis and place-and-route (PnR) requires careful consideration of multiple design objectives, primarily timing closure, area efficiency, and power consumption. These three aspects are often conflicting: improving timing may increase area, reducing area might worsen timing, and lowering power can sometimes compromise both performance and area. Therefore, electronic design automation (EDA) tools such as Synopsys Design Compiler and IC Compiler II provide different compilation and optimization strategies that allow the designer to prioritize one objective while maintaining acceptable trade-offs in the others. In this report, we investigate three different compilation flows—**Compile for Timing**, **Compile for Area**, and **Compile for Power**. Each flow explores the tool's optimization behavior under different constraints and effort levels, demonstrating how the synthesis engine allocates resources and applies techniques such as exact mapping, effort-driven optimization, and power-aware transformations. By comparing the results of these flows, we gain insight into how design choices impact the final quality of results (QoR), highlighting the trade-offs between performance, silicon utilization, and energy efficiency in design.

Chapter 1

PnR Flow Using Compile for Timing

1.1 Compilation

This stage involves generating the netlist and verifying timing. The objective is to produce a synthesized netlist that meets stringent timing constraints, ensuring the design operates at the desired frequency. The process involves applying timing-driven synthesis techniques to optimize critical paths, using tools to analyze and adjust the design for performance. The explanation focuses on configuring the synthesis tool with timing constraints, balancing performance with other design goals, and generating reports to validate the results. This configuration rep-

```
compile -exact_map -map_effort high -area_effort medium -power_effort none
```

Figure 1.1: Compile For Timing Optimization script

resents a timing-driven synthesis strategy that focuses on meeting critical timing constraints, applies moderate area optimization, and ignores power considerations, making it suitable when performance is the primary design goal.

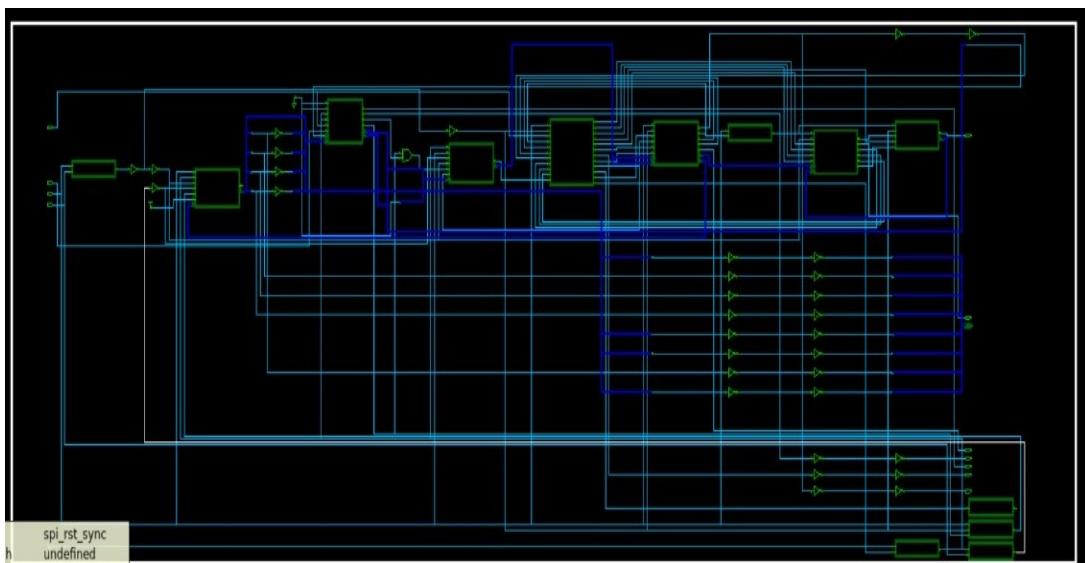


Figure 1.2: Netlist schematic during compilation.

```

Hostname: academysvr02

Compile CPU Statistics
-----
Resource Sharing:           1.06
Logic Optimization:        10.41
Mapping Optimization:      23.98

Overall Compile Time:      59.34
Overall Compile Wall Clock Time: 60.63

-----
Design  WNS: 6.42  TNS: 108.21  Number of Violating Paths: 175

Design (Hold)  WNS: 0.12  TNS: 21.51  Number of Violating Paths: 334

```

Figure 1.3: QoR Timing Report

Number of ports:	493
Number of nets:	2271
Number of cells:	1725
Number of combinational cells:	1322
Number of sequential cells:	378
Number of macros/black boxes:	0
Number of buf/inv:	444
Number of references:	20
Combinational area:	458.474400
Buf/Inv area:	127.205999
Noncombinational area:	391.963205
Macro/Black Box area:	0.000000
Net Interconnect area:	1046.442871
Total cell area:	850.437605
Total area:	1896.880476

Figure 1.4: Area Report

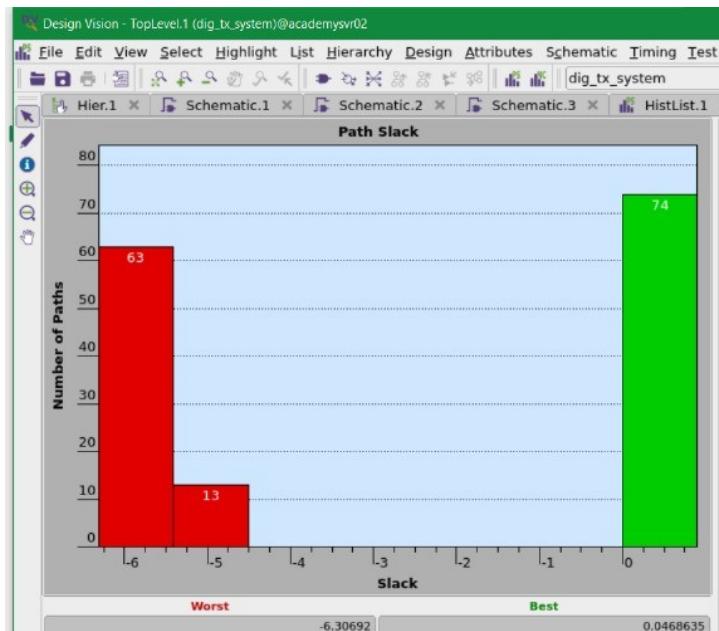


Figure 1.5: Timing Histogram after Compilation

1.2 Modifications

Common.tcl Modification on Paths for Timing Compilation. The objective is to adjust the tool's configuration files to ensure accurate path definitions, enabling precise timing analysis and synthesis. The explanation involves modifying the Common.tcl script to update library paths, timing constraints, and design files, ensuring the tool processes the correct data for timing optimization.

```

set DESIGN_NAME      "dig_tx_system"
set Constraints_file    "/home/svasicint25yoohamed/labs_modified/GP/cons/cons_v2.tcl"
set Constraints_file_sdc "/home/svasicint25yoohamed/labs_modified/GP/work_2/timing_dig_tx_system.sdc"
set Core_compile      "/home/svasicint25yoohamed/labs_modified/GP/work_2/timing_dig_tx_system.v"
set Warning_file      "${ROOT_DIR}/common/warnings_to_ignore.tcl"
##### outputs
set Svf_file          "/home/svasicint25yoohamed/labs_modified/GP/output/${DESIGN_NAME}_timing.svf"
set ARC_TOP           "/home/svasicint25yoohamed/labs_modified/GP/output/${DESIGN_NAME}_timing.ndm"
set Top_design_pt     "/home/svasicint25yoohamed/labs_modified/GP/output/${DESIGN_NAME}_timing_pt.v"
#####

```

Figure 1.6: Modification on Paths

```

#####
create_pg_ring_pattern \
    ring_pattern \
    -vertical_layer M7 -horizontal_layer M6 \
    -vertical_width 1 -horizontal_width 1 \
    -vertical_spacing 3 -horizontal_spacing 3
#####

```

Figure 1.7: Powerplan script modified

1.3 Setup Data

Preparation of libraries, constraints, and input files. The objective is to establish a solid foundation for the design flow by preparing all necessary data, ensuring compatibility and accuracy in subsequent steps. The explanation covers selecting appropriate timing libraries, defining design constraints, and organizing input files to support timing-driven synthesis.

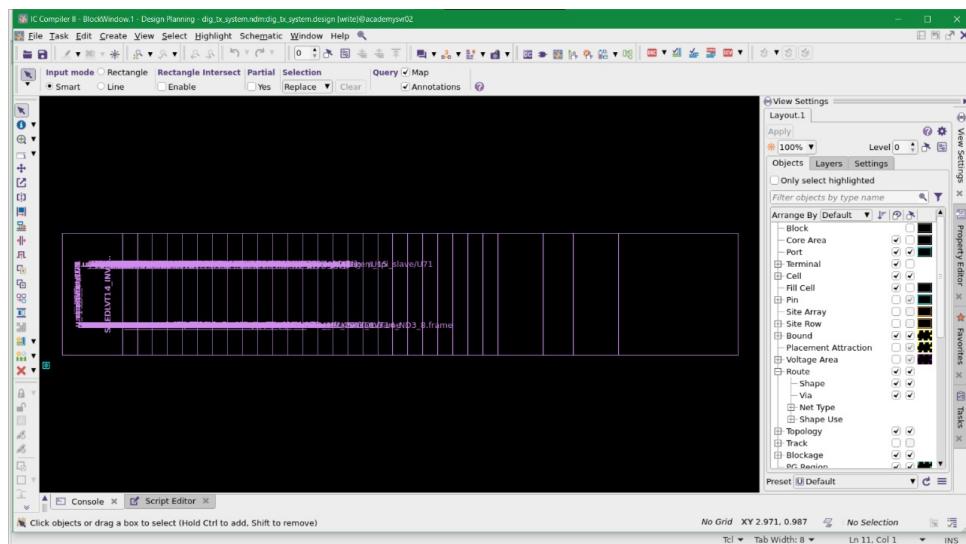


Figure 1.8: Data setup for timing optimization.

1.4 Floor Plan

Creating the chip outline and placing macros. The objective is to define the physical layout of the chip, optimizing for timing by strategically placing macros to minimize signal delays. The explanation includes determining core dimensions, aspect ratios, and macro placement to support high-speed operation.

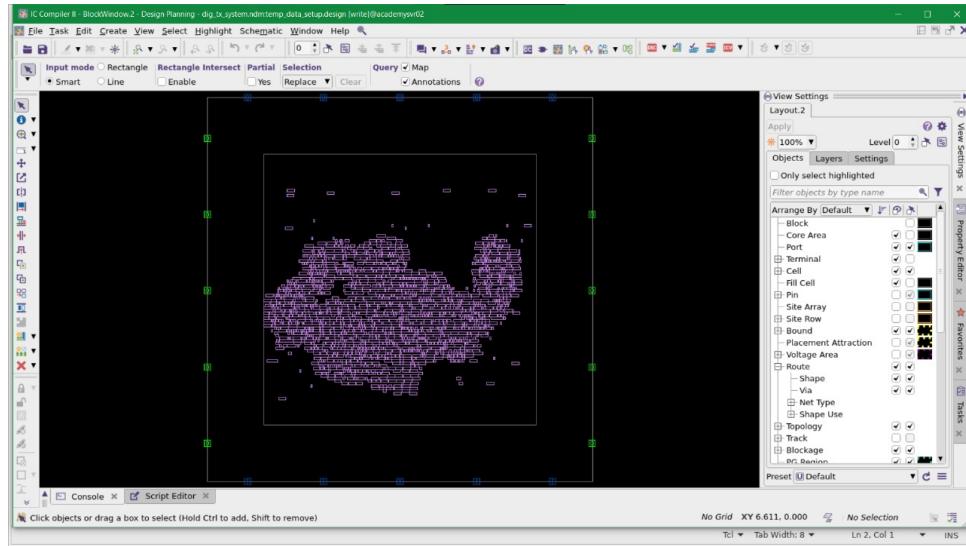


Figure 1.9: Floorplan layout.

1.5 Power Plan

Power distribution network design. The objective is to design a power grid that ensures stable voltage levels, minimizing IR drop to support timing performance. The explanation covers the creation of power rings, stripes, and connections to maintain reliability across the chip.

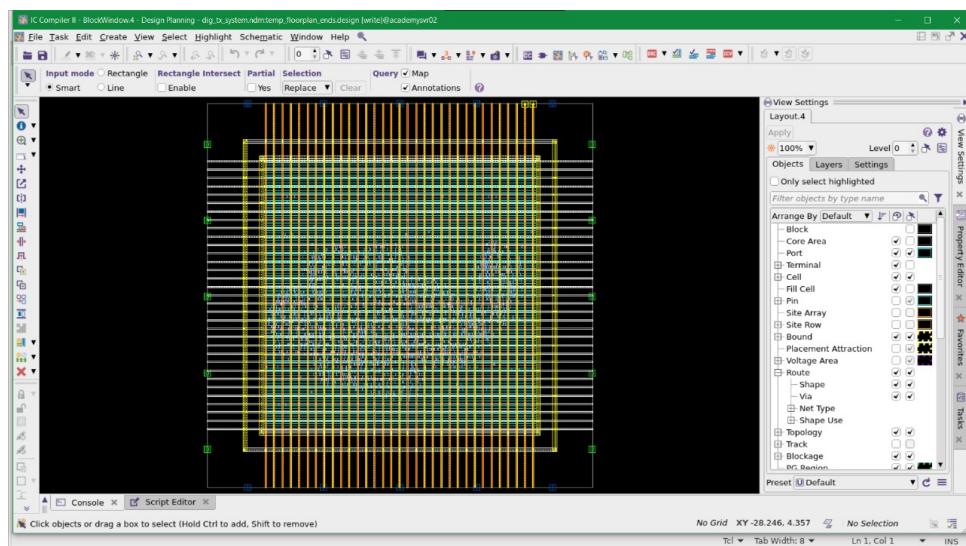


Figure 1.10: Power plan

1.6 Placement

The objective is to position standard cells to optimize timing by reducing critical path lengths and ensuring efficient cell density. The explanation details the use of timing-driven placement algorithms to arrange cells, balancing performance with layout constraints.

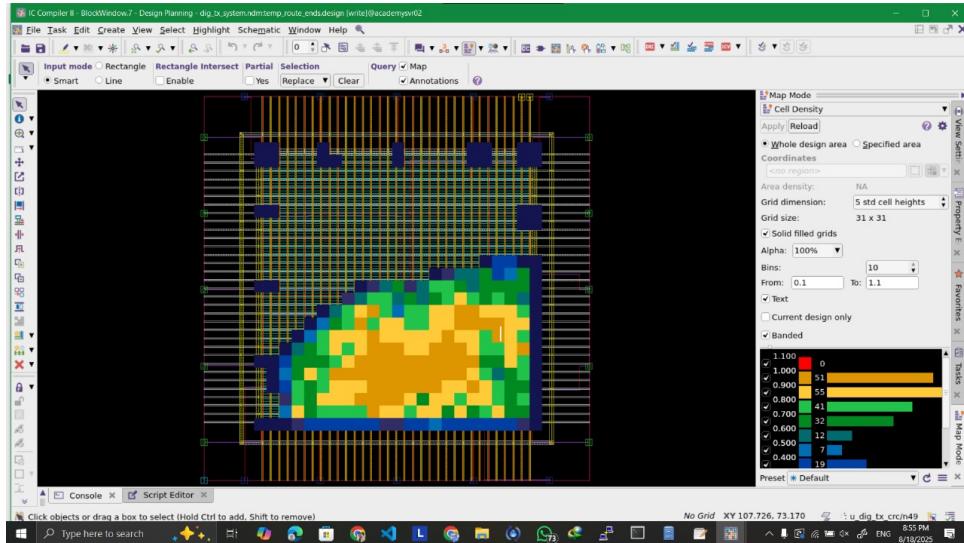


Figure 1.11: Cell density map.

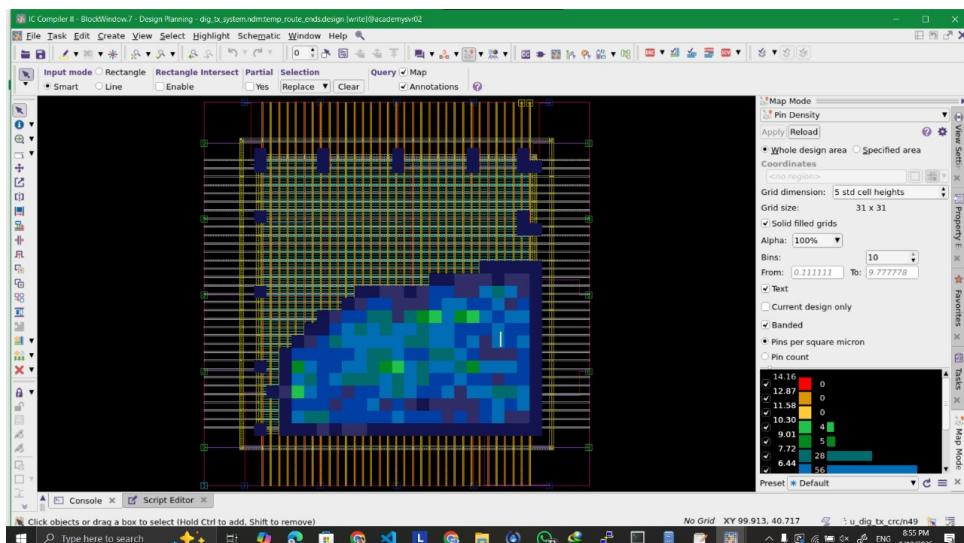


Figure 1.12: Pin density map.

```

Report : global timing
         -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date   : Mon Aug 18 20:05:32 2025
*****



Setup violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----
NNS     -7.051      0.000     -0.045     -7.051     -6.232
TNS     -93.072      0.000     -0.783    -86.056     -6.232
VUM       42          0          27          14          1
-----


Hold violations
-----
      Total    reg->reg    in->reg    reg->out    in->out
-----
NNS     -0.161      -0.161      0.000      0.000      0.000
TNS     -38.804     -38.804      0.000      0.000      0.000
VUM      362        362          0          0          0
-----
```

Figure 1.13: Global Timing Report for Placement

Area	
Combinational Area:	392.98
Noncombinational Area:	390.36
Buf/Inv Area:	86.22
Total Buffer Area:	11.41
Total Inverter Area:	74.81
Macro/Black Box Area:	0.00
Net Area:	0
Net XLength:	4028.89
Net YLength:	4068.06
Cell Area (netlist):	783.35
Cell Area (netlist and physical only):	783.35
Net Length:	8096.95

Design Rules	
Total Number of Nets:	1684
Nets with Violations:	865
Max Trans Violations:	15
Max Cap Violations:	15

Figure 1.14: QoR after Placement

1.7 Clock Tree Synthesis (CTS)

Balancing clock paths to reduce skew. The objective is to synthesize a clock tree that minimizes skew and latency, ensuring synchronized operation across the design. The explanation covers the insertion of buffers and optimization of clock paths to meet timing constraints.

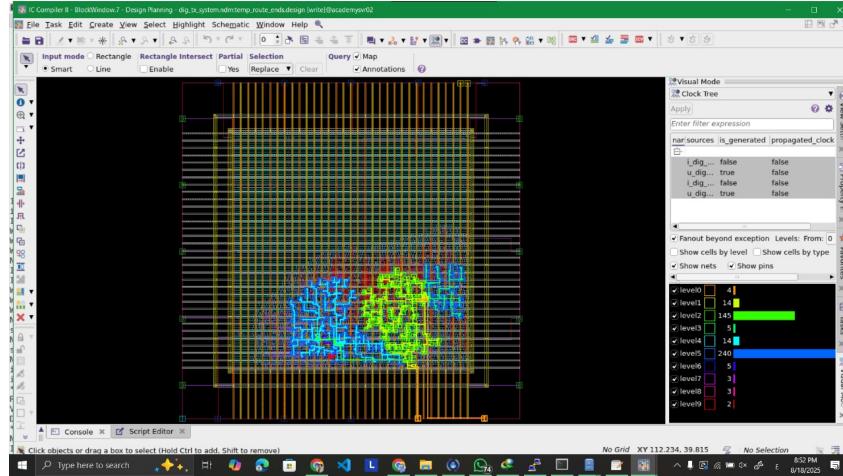


Figure 1.15: Clock Tree Synthesis (Step 1)

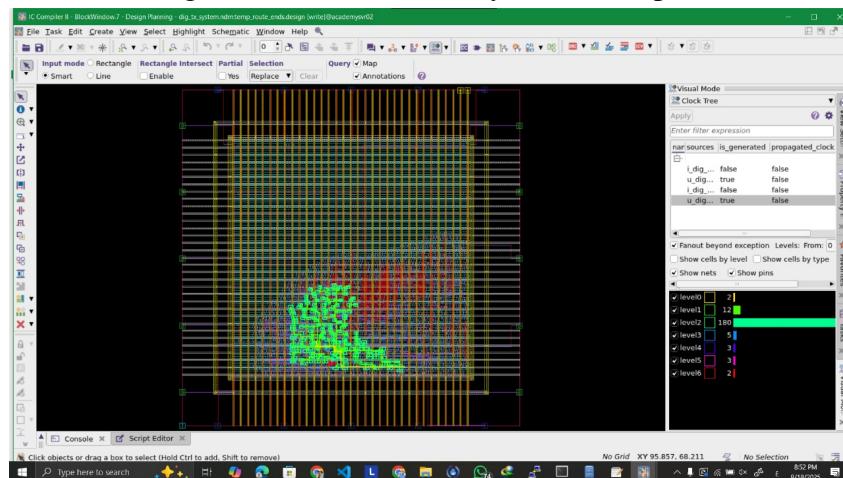


Figure 1.16: Clock Tree Synthesis (Step 2)

Setup violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-6.864	0.000	-0.197	-6.864	-6.237
TNS	-97.184	0.000	-4.974	-85.974	-6.237
NUM	42	0	27	14	1

Hold violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.137	-0.137	0.000	0.000	0.000
TNS	-0.397	-0.397	0.000	0.000	0.000
NUM	10	10	0	0	0

Figure 1.17: Global Timing After CTS

1.8 Routing

Connecting the placed standard cells and macros. The objective is to establish electrical connections that meet timing requirements while ensuring signal integrity. The explanation involves global and detailed routing strategies to minimize congestion and optimize path delays.

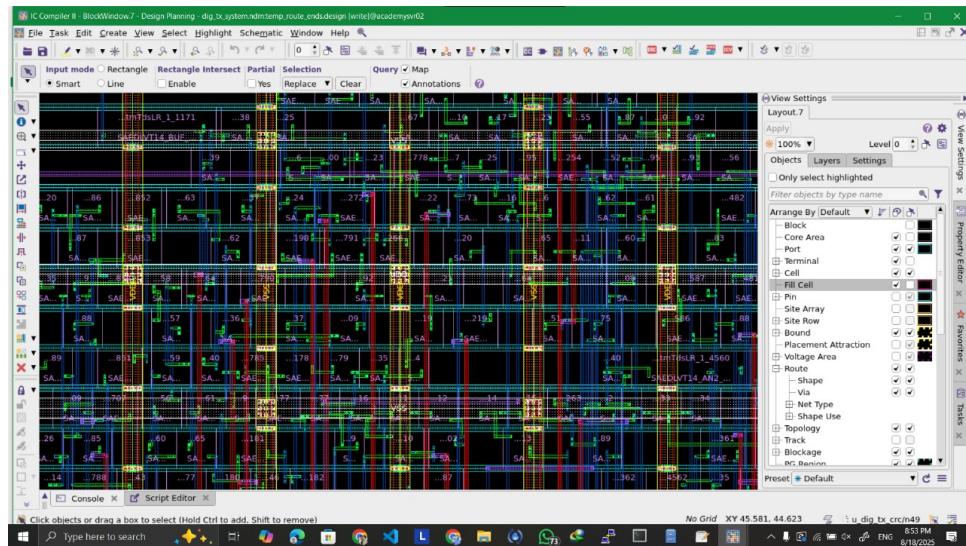


Figure 1.18: Routing stage.

Setup violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-6.775	0.000	-0.214	-6.775	-6.190
TNS	-96.929	0.000	-5.580	-85.159	-6.190
NUM	42	0	27	14	1

Hold violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.126	-0.126	0.000	0.000	0.000
TNS	-0.380	-0.380	0.000	0.000	0.000
NUM	21	21	0	0	0

Figure 1.19: global timing after Routing

1.9 Chip Finishing

Filler cell insertion, metal fill, and DRC checks. The objective is to finalize the layout by adding filler cells and metal fill to meet design rules, ensuring manufacturability while preserving timing. The explanation includes the process of inserting fillers and verifying the design against DRC. Detected short violation between filler cells, so the following command was used to

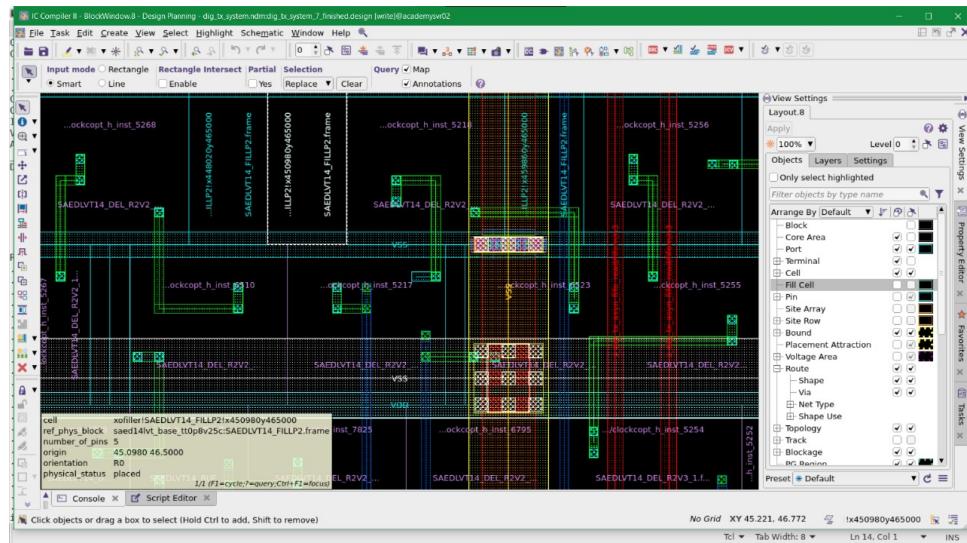


Figure 1.20: Chip finishing with filler cells.

```
=====
Maximum number of violations is set to 20
Abort checking when more than 20 violations are found
All violations might not be found.
=====
Total number of input nets is 3761.
Total number of short violations is 20.
Total number of open nets is 0.
Total number of floating route violations is 0.

Elapsed = 0:00:01, CPU = 0:00:01
1
```

Figure 1.21: LVS Check Report

```
set_attribute -objects [get_nets VDD] -name net_type -value power
set_attribute -objects [get_nets VSS] -name net_type -value ground

connect_pg_net -net VDD [get_pins -physical_context */VDD]
connect_pg_net -net VSS [get_pins -physical_context */VSS]
remove_stdcell_filters_with_violation
check_mv_design
```

Figure 1.22: Filler Short Removal Command

solve it.

1.10 STA and StarRC (PrimeTime)

Static timing analysis and parasitic extraction for sign-off. The objective is to validate the design's timing performance and extract parasitics for accurate analysis. The explanation covers running STA with StarRC to identify critical paths and ensure timing closure.

```

The file "/home/vasakint2yoohame... sta/sta_globalbefore.tim" changed on disk.

*****
Report : global_timing
        -format { narrow }
Design : dig_tx_system
Version: W-2024.09-SP5
Date   : Mon Aug 18 21:43:31 2025
*****


Setup violations
-----
Total reg->reg in->reg reg->out in->out
-----
WNS  -5.508  0.000  -0.213  -5.508  -5.179
TNS  -79.906  0.000  -5.551  -69.176  -5.179
NUM   42      0       27      14      1

Hold violations
-----
Total reg->reg in->reg reg->out in->out
-----
WNS  -0.126  -0.126  0.000  0.000  0.000
TNS  -4.652  -4.652  0.000  0.000  0.000
NUM   174     174     0       0       0

1

```

Figure 1.23: Global timing report before PrimeTime.

```
pt shell> insert_buffer -new_cell_names "clk1_buf_capture156" -new_net_names "cl32k_net_delayed155" [get_pins u_dig_tx_reg_file/reg_file_reg[0][0]/Q] [get_lib_cells */|]
SAEDLVT14 BUF 1]
```

Figure 1.24: fixing the hold violations using insert buffer

```

noТИcim2$yoohame@academyin0:~/lab_modified/C9/a0_st
File Edit View Search Terminal Help
u_spi_slave/U48/X (SAEDLVT14_AN3_4)          0.01 &  0.59 f
u_spi_slave/U41/X (SAEDLVT14_OR2_MM_12)        0.01 &  0.66 f
clockgen_mt_INV_384_f_inst_7085/X (SAEDLVT14_INV_S_20)
o_dig_tx_system_miso [out]
data arrival time                                3.36 &  3.97 r
data required time                               1.84 &  5.81 r
data arrival time                                5.81
data required time                               5.81

clock spi_gated_clk (rise edge)                 1.00
clock network delay (ideal)                     0.00
clock reconvergence pessimism                  0.00
clock uncertainty                                0.30
output external delay                           0.40
data required time                               0.30

data required time                                0.30
data arrival time                                5.81
-----
slack (VIOLATED)                                -5.51

1
pt shell> report_global_timing
*****
Report : global_timing
        -format { narrow }
Design : dig_tx_system
Version: W-2024.09-SP5
Date   : Mon Aug 18 21:59:34 2025
*****


Setup violations
-----
Total reg->reg in->reg reg->out in->out
-----
WNS  -5.51    0.00  -0.21  -5.51    -5.18
TNS  -79.91   0.00  -5.55  -69.18   -5.18
NUM   42      0     27     14      1

No hold violations found.
1
pt shell>
```

Figure 1.25: Global timing report after PrimeTime.

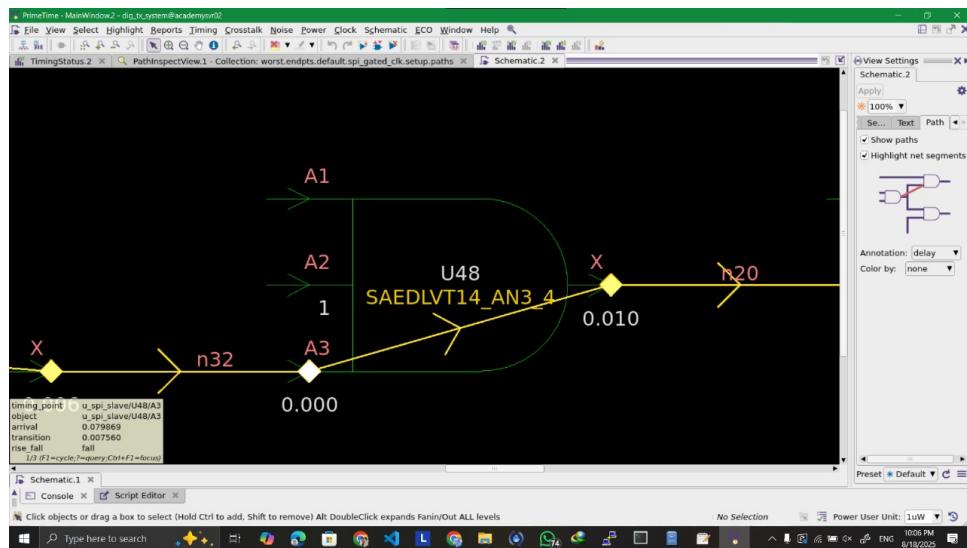


Figure 1.26: Cell path schematic for STA.

PrimeTime - MainWindow2 - dig_tx_system@academy037

File View Select highlight Reports Timing Crosstalk Noise Power Clock Schematic ECO Window Help

TimingStatus.2 x PathInsightsView.1 - Collection: worst.endpts.default.spi_gated_clk.setup.paths x Schematic.2 x

Error: unknown option '-from(u_spi_slave/U4B/A3)' (CMD_010)
Error: unknown option '-to(u_spi_slave/U4B/X)' (CMD_010)
pt_shells> report_delay calculation from {u_spi_slave/U4B/A3} to {u_spi_slave/U4B/X}

Report : delay_calculation
Design : dig_tx_system
Version: W-2024.09 SP5
Date : Mon Aug 18 22:05:13 2025

From pin: u_spi_slave/U4B/A3
To pin: u_spi_slave/U4B/X
Main Library Units: lns 1pf 1kOhm

Library: 'saedlvt_base_tt0pBv25c'
Library Units: lns 1pf 1kOhm
Library Cell: 'SAEDLV14_AN3_4'
arc sense: positive_unate
arc type: cell

RC network on pin 'u_spi_slave/U4B/X' :

Number of elements = 3 Capacitances + 2 Resistances
Total capacitance = 0.000511 pF
Total capacitance = 0.000511 (in library unit)
Total Resistance = 0.010000 Kohm

Figure 1.27: Delay calculation report 1.

```

* Endpoints Materialized: u_spl_slave448/X
File View Select Highlight Reports Timing Crosstalk Noise Power Clock Schematic ECO Window Help
TimingStatus.2 <--> PathpectorView1 - Collection: worst.endpts.default.spi_gated_clk.setup.paths <--> Schematic.2
Schematic.2
View Settings Apply 100% Se Text Path
Library: "cadliblvt_base_110p025c"
Library Units: lns lpf 1kohm
Library Cell: "SADLV14_AN3_4"
arc type: positive_uate
arc type: cell
RC network on pin "u_spl_slave448/X" :
Number of elements = 3 Capacitances + 2 Resistances
Total capacitance = 0.0002511 pF
Total capacitance = 0.0002511 (in library unit)
Total resistance = 0.010000 Kohn
Total resistance = 0.010000 (in library unit)
Cell delay = 0.015613 0.015613 (in library unit)

Rise Fall
Input transition time = 0.007395 0.007540 (in library unit)
Effective capacitance = 0.0002511 0.0002511 (in pF)
Effective capacitance = 0.0002511 0.0002511 (in library unit)
Drive resistance = 0.010000 0.010000 (in Kohm)
Output transition time = 0.004216 0.003677 (in library unit)
Cell delay = 0.015613 0.015613 (in library unit)

From pin: u_spl_slave448/X
To pin: u_spl_slave448/X
Main Library Units: lns lpf 1kohm
Log History
Console Script Editor
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Family/Out ALL levels
u_spl_slave448/X Power User Unit: 1uW 1007 PM 8/18/2025
Type here to search

```

Figure 1.28: Delay Calculation Report 2

```

* Endpoints Materialized: u_spl_slave448/X
File View Select Highlight Reports Timing Crosstalk Noise Power Clock Schematic ECO Window Help
TimingStatus.2 <--> PathpectorView1 - Collection: worst.endpts.default.spi_gated_clk.setup.paths <--> Schematic.2
Schematic.2
View Settings Apply 100% Se Text Path
Library: "cadliblvt_base_110p025c"
Library Units: lns lpf 1kohm
Library Cell: "SADLV14_AN3_4"
arc type: positive_uate
arc SDP condition: Al=1|BldA2=1|Bl
arc type: cell
RC network on pin "u_spl_slave448/X" :
Number of elements = 3 Capacitances + 2 Resistances
Total capacitance = 0.0002511 pF
Total capacitance = 0.0002511 (in library unit)
Total resistance = 0.010000 Kohn
Total resistance = 0.010000 (in library unit)
Cell delay = 0.015613 0.015613 (in library unit)

Rise Fall
Input transition time = 0.007395 0.007540 (in library unit)
Effective capacitance = 0.0002511 0.0002511 (in pF)
Effective capacitance = 0.0002511 0.0002511 (in library unit)
Drive resistance = 0.010000 0.010000 (in Kohm)
Output transition time = 0.004216 0.003677 (in library unit)
Cell delay = 0.015613 0.015613 (in library unit)

1 pt shell>
Log History
Console Script Editor
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Family/Out ALL levels
u_spl_slave448/X Power User Unit: 1uW 1007 PM 8/18/2025
Type here to search

```

Figure 1.29: Delay Calculation Report 3

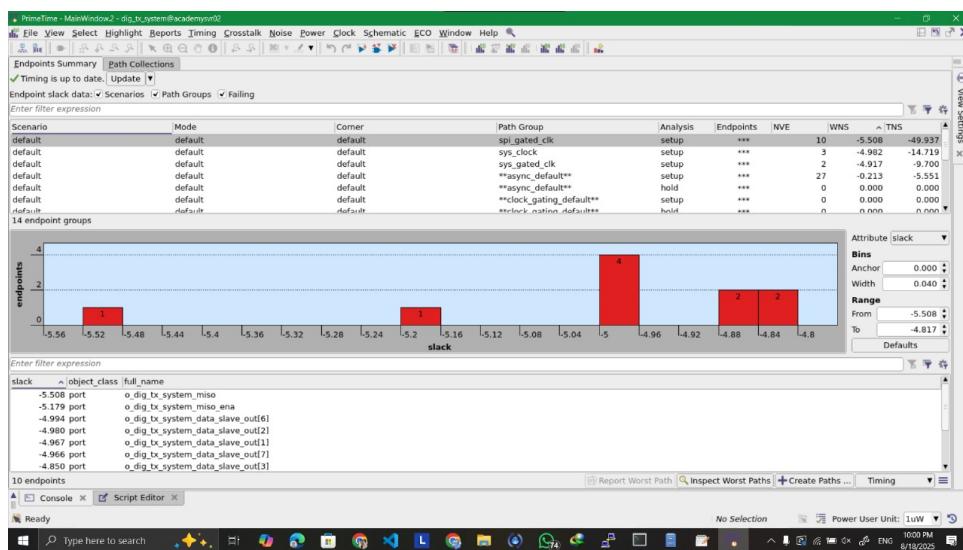
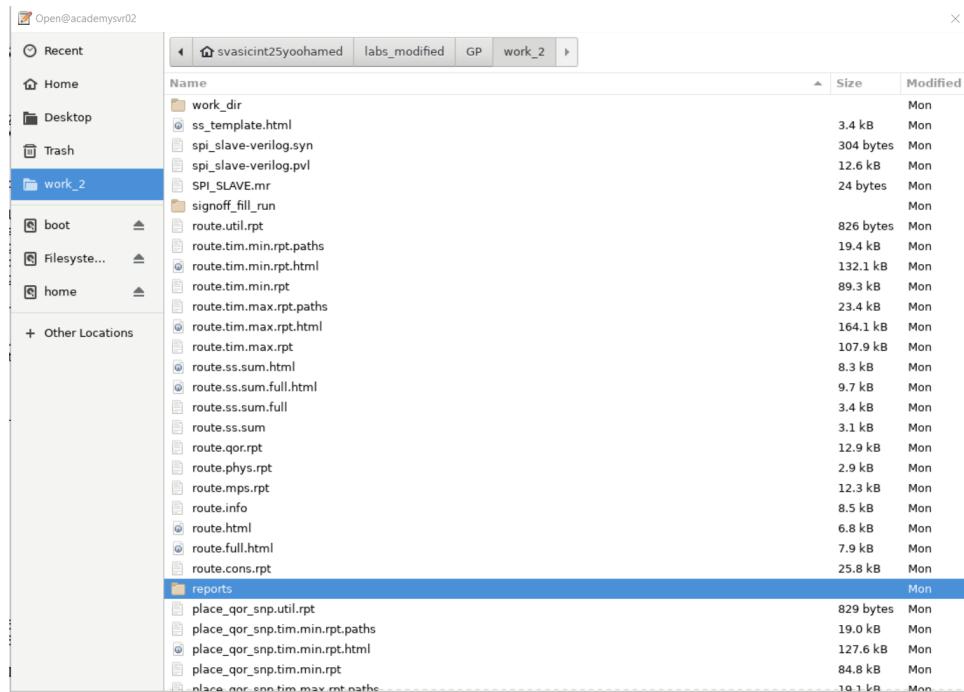


Figure 1.30: PrimeTime Histogram of Slack Time Slots

1.11 Notes1

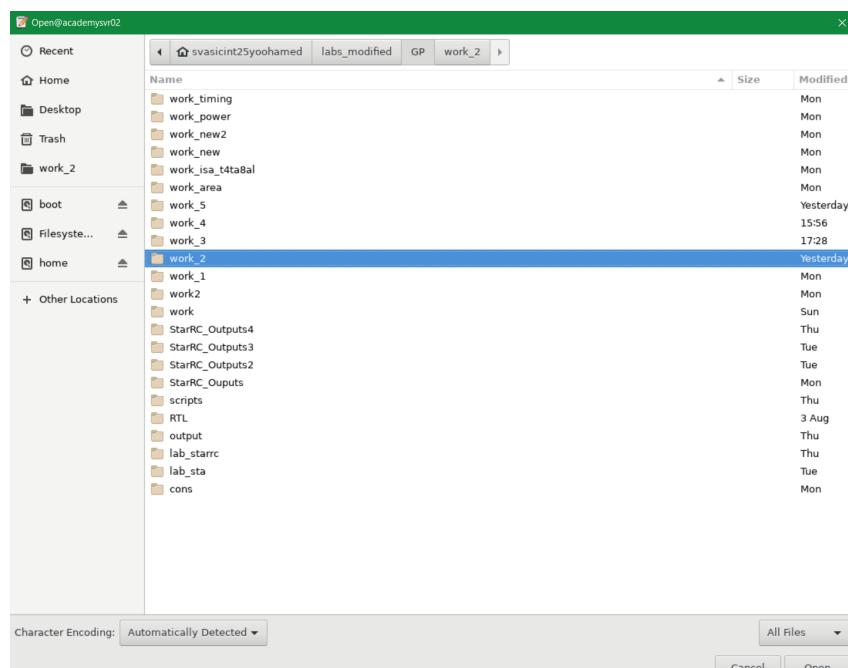
The reports documented in the previous chapter can be found at the following destination:

/home/svasicint25yoohamed/labs_modified/GP/Work_2/reports



Name	Size	Modified
work_dir	3.4 kB	Mon
ss_template.html	304 bytes	Mon
spi_slave-verilog.syn	12.6 kB	Mon
spi_slave-verilog.pvl	24 bytes	Mon
SPI_SLAVE.mr		
signoff_fill_run		
route.util.rpt	826 bytes	Mon
route.tim.min.rpt.paths	19.4 kB	Mon
route.tim.min.rpt.html	132.1 kB	Mon
route.tim.min.rpt	89.3 kB	Mon
route.tim.max.rpt.paths	23.4 kB	Mon
route.tim.max.pt.html	164.1 kB	Mon
route.tim.max.rpt	107.9 kB	Mon
route.ss.sum.html	8.3 kB	Mon
route.ss.sum.full.html	9.7 kB	Mon
route.ss.sum.full	3.4 kB	Mon
route.ss.sum	3.1 kB	Mon
route.qor.rpt	12.9 kB	Mon
route.phys.rpt	2.9 kB	Mon
route.mps.rpt	12.3 kB	Mon
route.info	8.5 kB	Mon
route.html	6.8 kB	Mon
route.full.html	7.9 kB	Mon
route.cons.rpt	25.8 kB	Mon
reports		Mon
place_qor_snp.util.rpt	829 bytes	Mon
place_qor_snp.tim.min.rpt.paths	19.0 kB	Mon
place_qor_snp.tim.min.rpt.html	127.6 kB	Mon
place_qor_snp.tim.min.rpt	84.8 kB	Mon
place_qor_snp.tim.max.rpt.paths	10.1 kB	Mon

Figure 1.31: Reports Path Destination



Name	Size	Modified
work_timing		Mon
work_power		Mon
work_new2		Mon
work_new		Mon
work_isa_t4ta8al		Mon
work_area		Mon
work_5		Yesterday
work_4		15:56
work_3		17:28
work_2		Yesterday
work_1		Mon
work2		Sun
work		Thu
StarRC_Outputs4		Tue
StarRC_Outputs3		Tue
StarRC_Outputs2		Mon
StarRC_Outputs		Thu
scripts		Thu
RTL		3 Aug
output		Thu
lab_starrc		Thu
lab_sta		Tue
cons		Mon

Figure 1.32: Work_2 Destination Path

Chapter 2

PnR Flow Using Compile for Area

2.1 Compilation

The aim of this stage is to generate a netlist optimized primarily for area, balancing timing so that the design remains functional but compact. The objective is to reduce silicon footprint by prioritizing cell packing and area-efficient libraries while still maintaining timing closure. The process involves area-driven synthesis strategies, validation with QoR reports, and analysis of area trade-offs against timing.

```
compile -map_effort medium -area_effort high -power_effort none
```

Figure 2.1: Compile For Area Optimization Script

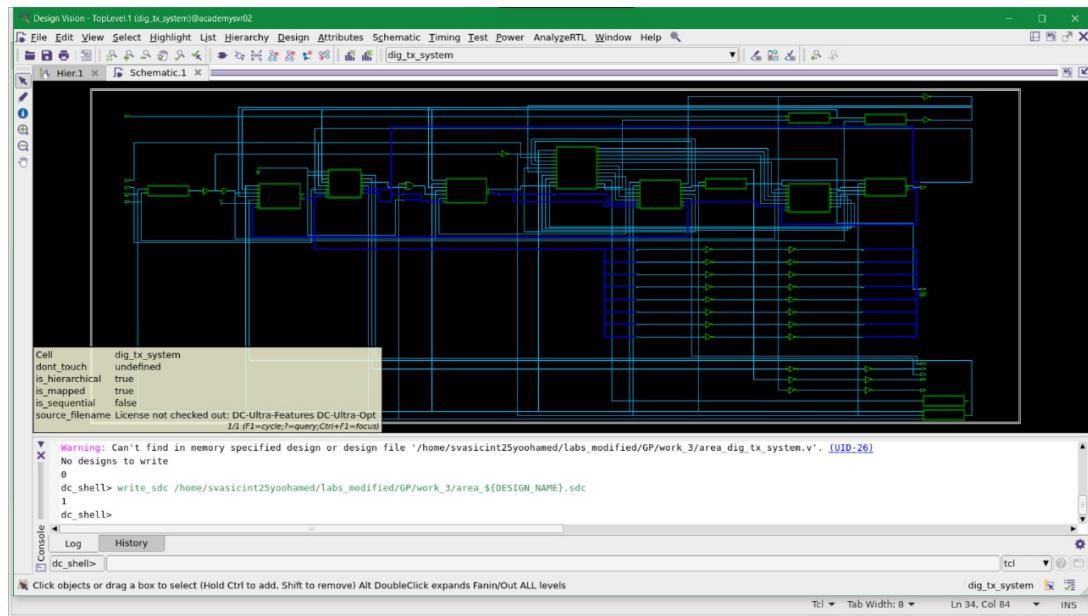


Figure 2.2: Netlist schematic during area compilation.

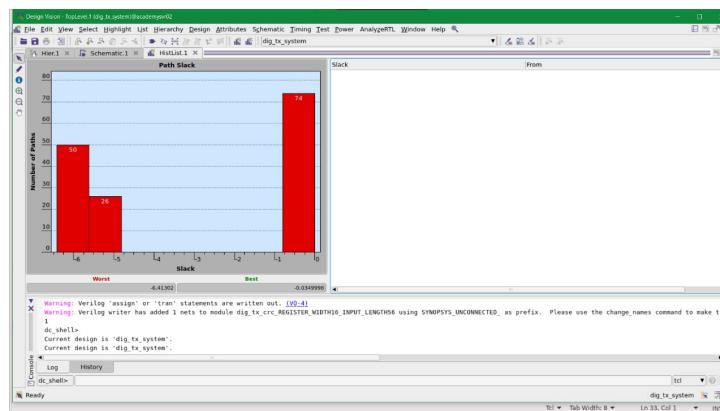


Figure 2.3: Histogram for Slack report

Number of ports:	493
Number of nets:	2255
Number of cells:	1700
Number of combinational cells:	1297
Number of sequential cells:	378
Number of macros/black boxes:	0
Number of buf/inv:	428
Number of references:	20
Combinational area:	452.036400
Buf/Inv area:	123.254399
Noncombinational area:	392.806805
Macro/Black Box area:	0.000000
Net Interconnect area:	1040.905167
Total cell area:	844.843205
Total area:	1885.748372

Figure 2.4: Area Report in Area Compilation

```
Compile CPU Statistics
-----
Resource Sharing:          0.95
Logic Optimization:        8.12
Mapping Optimization:      21.43
-----
Overall Compile Time:      50.70
Overall Compile Wall Clock Time: 52.22
-----
Design  WNS: 6.41  TNS: 110.97  Number of Violating Paths: 200
Design (Hold)  WNS: 0.12  TNS: 21.29  Number of Violating Paths: 331
```

Figure 2.5: QoR Report

2.2 Setup Data

The aim here is to prepare input data with a focus on minimizing chip area. The objective is to use compact cell libraries, set utilization targets, and configure constraints that enable area-efficient synthesis and placement. This ensures that subsequent steps operate under area-aware conditions.

```
##### VARIABLES TO MODIFY #####
set ROOT_DIR      "/home/svasicint25yoohamed/labs_modified/GP/scripts"
set DESIGN_REF_PATH "/home/tools/PDK/SAED14_EDK"

set VERILOG_DIR    "/home/svasicint25yoohamed/labs_modified/GP/RTL"

#####
set DESIGN_NAME     "dig_tx_system"
set Constraints_file "/home/svasicint25yoohamed/labs_modified/GP/cons/cons_v2.tcl"
set Constraints_file_sdc "/home/svasicint25yoohamed/labs_modified/GP/work_3/area_dig_tx_system.sdc"
set Core_compile   "/home/svasicint25yoohamed/labs_modified/GP/work_3/area_dig_tx_system.v"
set Warning_file   "${ROOT_DIR}/common/warnings_to_ignore.tcl"
#####
outputs
set Svf_file        "/home/svasicint25yoohamed/labs_modified/GP/output/${DESIGN_NAME}_area.svf"
set ARC_TOP         "/home/svasicint25yoohamed/labs_modified/GP/output/${DESIGN_NAME}_area.ndm"
set Top_design_pt  "/home/svasicint25yoohamed/labs_modified/GP/output/${DESIGN_NAME}_area_pt.v"
#####

```

Figure 2.6: compilation Paths

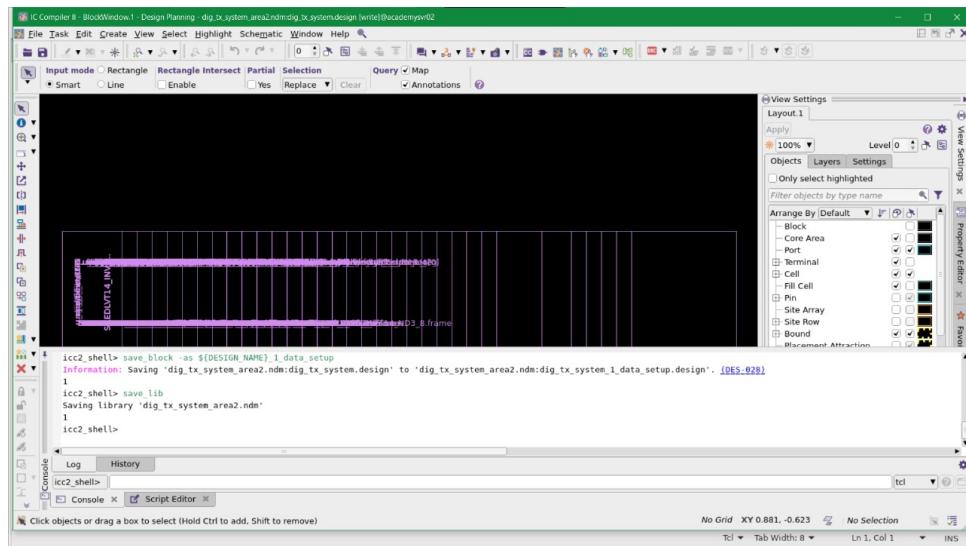


Figure 2.7: data setup.

2.3 Floor Plan

The aim is to design a compact floorplan that minimizes wasted area. The objective is to place macros tightly while avoiding routing congestion. This step sets the physical framework for area-driven optimization.

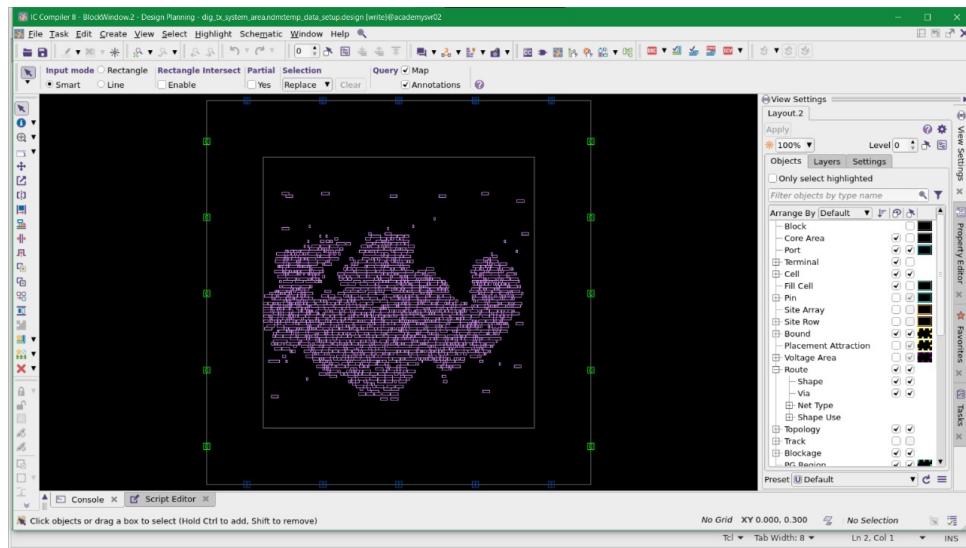


Figure 2.8: Floorplan for Area Optimization.

2.4 Power Plan

The aim is to create a power distribution network with minimal area overhead. The objective is to ensure adequate power integrity while maintaining high utilization efficiency.

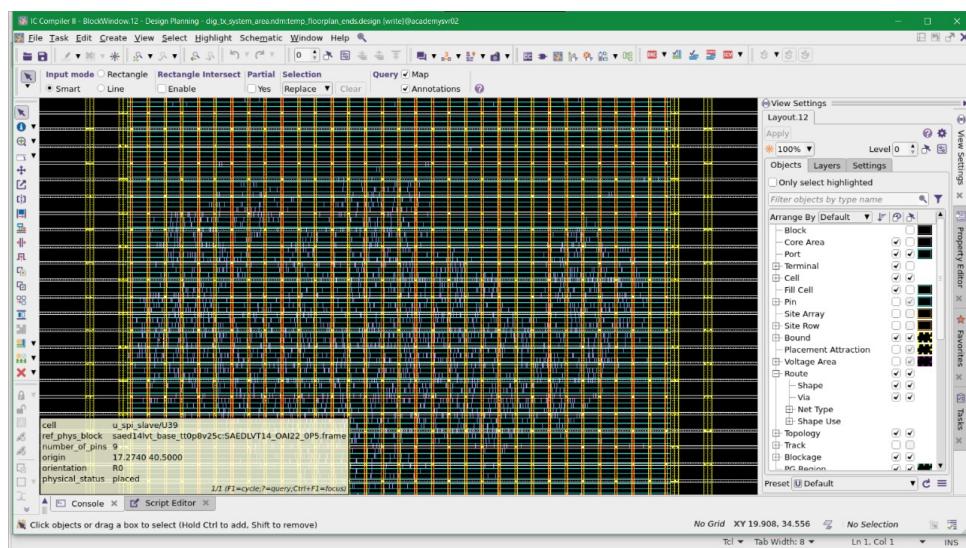


Figure 2.9: Power plan for Area Optimization.

2.5 Placement

Placement in area-optimized compilation aims at maximizing density while keeping routing feasible. The objective is to pack cells tightly without creating hotspots or violations.

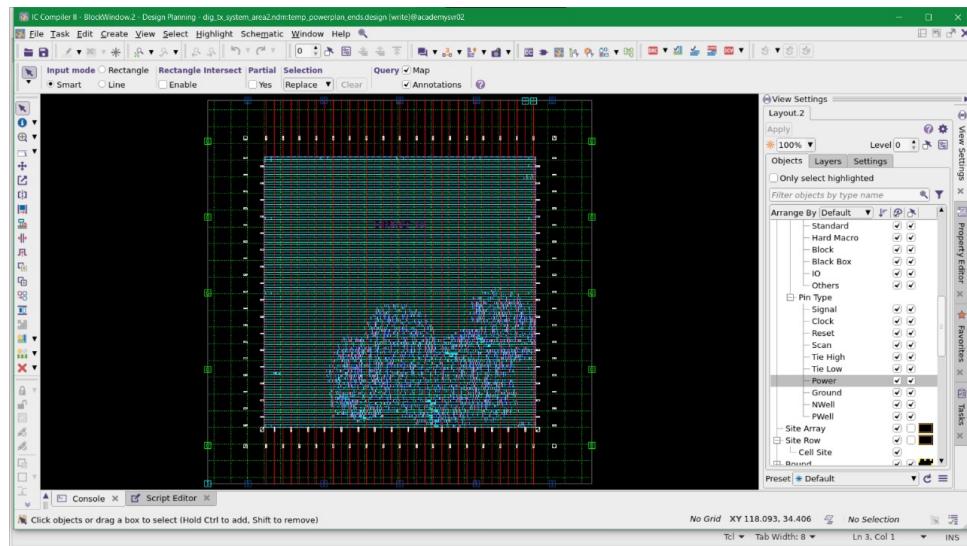


Figure 2.10: Placement view during area compilation.

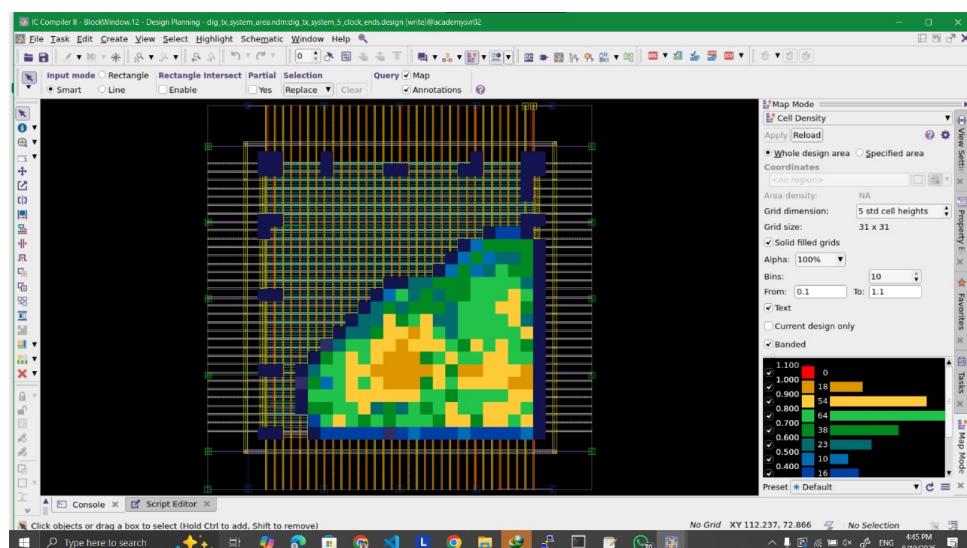


Figure 2.11: Cell density in area-optimized placement.

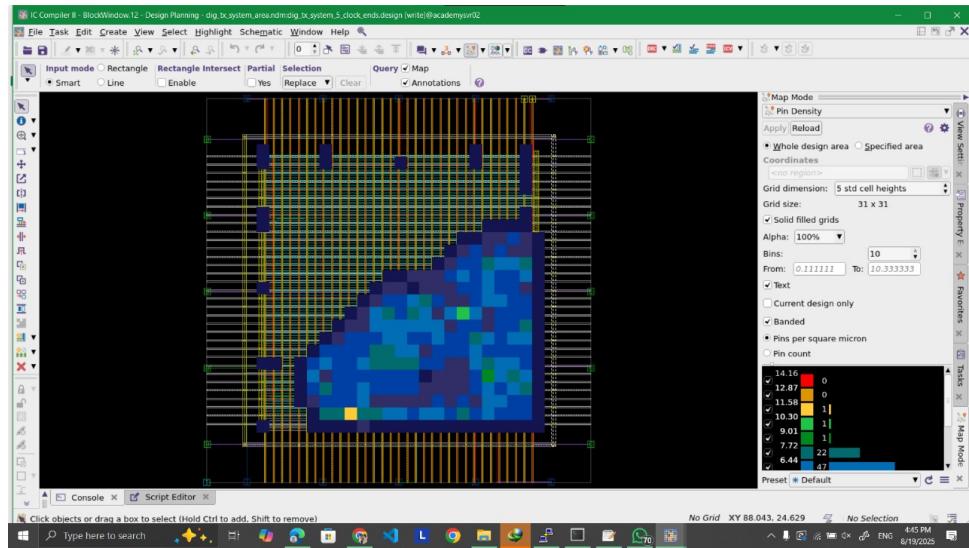


Figure 2.12: Pin density distribution in area optimization.

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-7.159	0.000	-0.057	-7.159	-5.940
TNS	-92.016	0.000	-0.865	-85.210	-5.940
NUM	42	0	27	14	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.180	-0.180	0.000	0.000	0.000
TNS	-39.108	-39.108	0.000	0.000	0.000
NUM	370	370	0	0	0

1

Figure 2.13: Global timing report after placement

2.6 Clock Tree Synthesis (CTS)

The aim of CTS in area optimization is to minimize buffer count and routing overhead. The objective is to distribute the clock with minimal area cost while keeping skew and latency within limits.

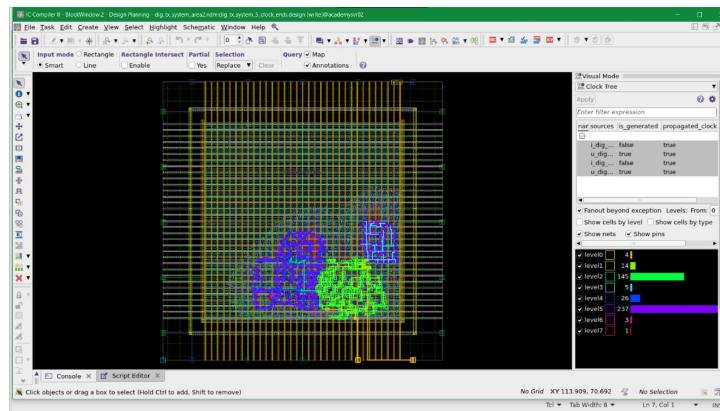


Figure 2.14: CTS Highlighted (Step 1).

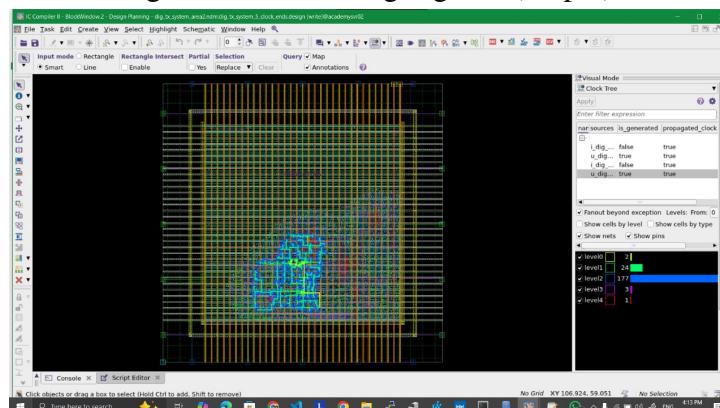


Figure 2.15: CTS Step 2.

```

Warning: Invalid user port delay or slew threshold setting, use default setting. (TIM-205)
*****
Report : global timing
  -format { narrow }
Design : dig_tx_system
Version: V-2023.12-SP5
Date  : Sat Aug 23 00:27:53 2025
*****



Setup violations
-----
      Total   reg->reg   in->reg   reg->out   in->out
WNS    -6.69     0.00    -0.21    -6.69    -6.44
TNS    -96.24    0.00    -5.54   -84.26    -6.44
NUM      42        0       27       14        1

Hold violations
-----
      Total   reg->reg   in->reg   reg->out   in->out
WNS    -0.13    -0.13     0.00     0.00     0.00
TNS    -0.37    -0.37     0.00     0.00     0.00
NUM      12        12        0        0        0
  
```

Figure 2.16: CTS Global timing report

2.7 Routing

Routing in area optimization focuses on minimizing metal track usage. The objective is to ensure complete connectivity without excessive wirelength that would increase chip area.

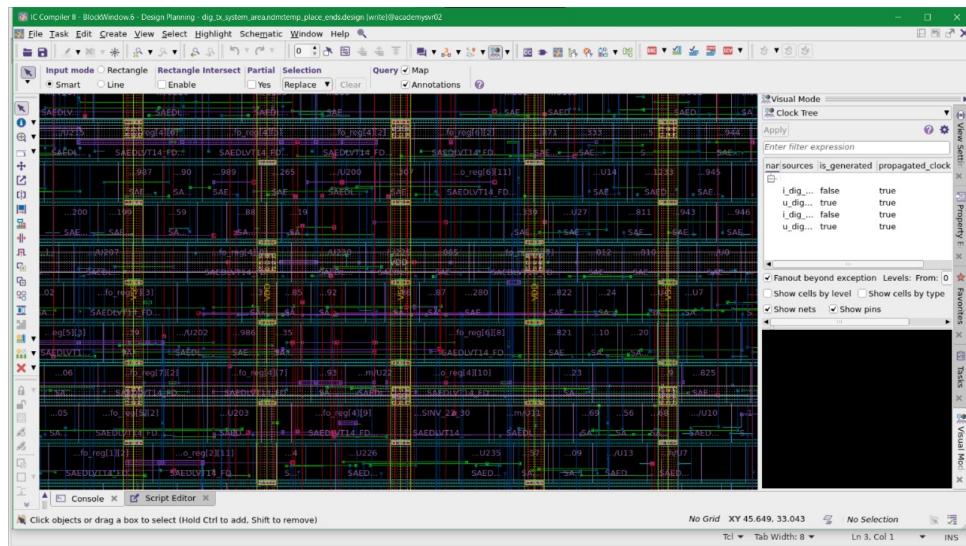


Figure 2.17: Routing under area-driven constraints.

Setup violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-6.754	0.000	-0.205	-6.754	-6.444
TNS	-96.928	0.000	-5.537	-84.947	-6.444
NUM	42	0	27	14	1

Hold violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.126	-0.126	0.000	0.000	0.000
TNS	-0.381	-0.381	0.000	0.000	0.000
NUM	17	17	0	0	0

Figure 2.18: Global Timing after Routing Report

2.8 Chip Finishing

Chip finishing in area optimization aims at reducing filler usage and metal fill while still meeting DRC and LVS checks. The objective is to preserve compactness while ensuring manufacturability.

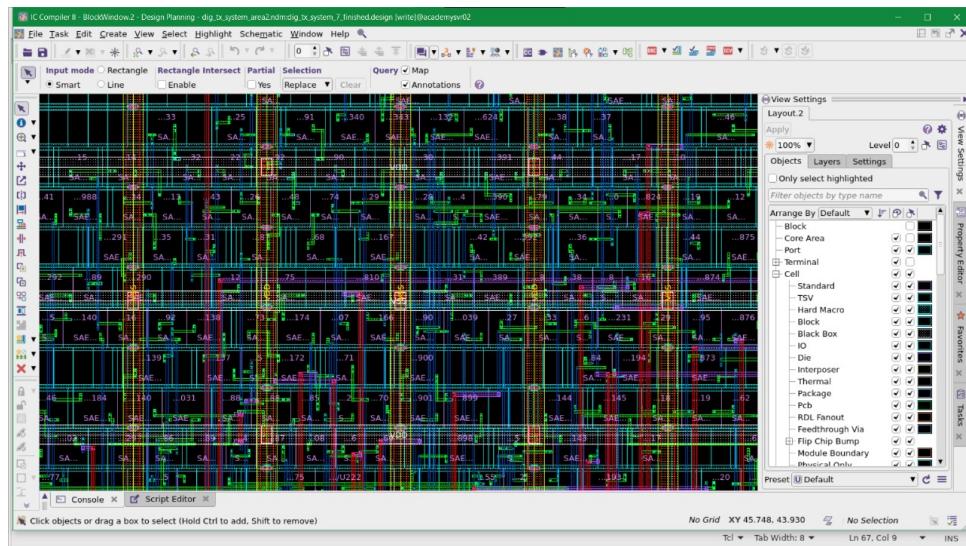


Figure 2.19: Chip finishing along with metal fill in area compilation.

```

dig_tx_system.lvs.rpt
Save   E   x
dig_tx_system.lvs.rpt
The file "/home/avaskin7/syohame_rts/dig_tx_system.lvs.rpt" changed on disk.
Reload  x

Information: Detected short violation. Cell1: xofiller!SAEDLV14_FILLP2!x165340y135000. Cell2: xofiller!SAEDLV14_FILLP2!x168300y135000. BBox: (16.7888 13.5570)(16.8720
13.6430). Layer: M2 (RT-S86)
Information: Detected short violation. Cell1: xofiller!SAEDLV14_FILLP2!x161640y141000. Cell2: xofiller!SAEDLV14_FILLP2!x164600y141000. BBox: (16.4188 14.5570)(16.5020
14.6430). Layer: M2 (RT-S86)
Information: Detected short violation. Cell1: xofiller!SAEDLV14_FILLP2!x158680y141000. Cell2: xofiller!SAEDLV14_FILLP2!x161640y141000. BBox: (16.1220 14.5570)(16.2060
14.6430). Layer: M2 (RT-S86)
Information: Detected short violation. Cell1: xofiller!SAEDLV14_FILLP2!x155720y141000. Cell2: xofiller!SAEDLV14_FILLP2!x158600y141000. BBox: (15.8260 14.5570)(15.9100
14.6430). Layer: M2 (RT-S86)
Information: Detected short violation. Cell1: xofiller!SAEDLV14_FILLP2!x152760y141000. Cell2: xofiller!SAEDLV14_FILLP2!x155720y141000. BBox: (15.5390 14.5570)(15.6140
14.6430). Layer: M2 (RT-S86)
Information: Detected short violation. Cell1: xofiller!SAEDLV14_FILLP2!x149880y141000. Cell2: xofiller!SAEDLV14_FILLP2!x152760y141000. BBox: (15.2340 14.5570)(15.3180
14.6430). Layer: M2 (RT-S86)
Information: Detected short violation. Cell1: xofiller!SAEDLV14_FILLP2!x146840y141000. Cell2: xofiller!SAEDLV14_FILLP2!x149800y141000. BBox: (14.9380 14.5570)(15.1340
14.6430). Layer: M2 (RT-S86)
Information: Detected short violation. Cell1: xofiller!SAEDLV14_FILLP2!x162380y135000. Cell2: xofiller!SAEDLV14_FILLP2!x165340y135000. BBox: (16.4920 13.5570)(16.5760
13.6430). Layer: M2 (RT-S86)
Information: Detected short violation. Cell1: xofiller!SAEDLV14_FILLP2!x159420y135000. Cell2: xofiller!SAEDLV14_FILLP2!x162380y135000. BBox: (16.1960 13.5570)(16.2880
13.6430). Layer: M2 (RT-S86)
Information: Detected short violation. Cell1: xofiller!SAEDLV14_FILLP2!x156460y135000. Cell2: xofiller!SAEDLV14_FILLP2!x159420y135000. BBox: (15.9080 13.5570)(15.9840
13.6430). Layer: M2 (RT-S86)
Information: Detected short violation. Cell1: xofiller!SAEDLV14_FILLP2!x153500y135000. Cell2: xofiller!SAEDLV14_FILLP2!x156460y135000. BBox: (15.6640 13.5570)(15.6880
13.6430). Layer: M2 (RT-S86)
Information: Detected short violation. Cell1: xofiller!SAEDLV14_FILLP2!x143880y141000. Cell2: xofiller!SAEDLV14_FILLP2!x146840y141000. BBox: (14.6420 14.5570)(14.7260
14.6430). Layer: M2 (RT-S86)
Information: Detected short violation. Cell1: xofiller!SAEDLV14_FILLP2!x140920y141000. Cell2: xofiller!SAEDLV14_FILLP2!x143880y141000. BBox: (14.3400 14.5570)(14.4300
14.6430). Layer: M2 (RT-S86)
Information: Detected floating route violation. Cell1: xofiller!SAEDLV14_FILLP2!x137960y141000. Cell2: xofiller!SAEDLV14_FILLP2!x140920y141000. BBox: (14.0500 14.5570)(14.1340
14.6430). Layer: M2 (RT-S86)

Maximum number of violations is set to 20
Abort checking when more than 20 violations are found
All violations might not be found.

Total number of input nets is 3711.
Total number of short violations is 20.
Total number of floating nets is 0.
Total number of floating route violations is 0.

Plain Text  Tab Width: 8  Ln 1, Col 1  INS

```

Figure 2.20: LVS Check Report for Area Compilation.

ErrorSet	Total	Visible	Fixed	Ignored	Waived	NULL Net	Detected
...2.ndm:temp_powerplan_ends.design	20	20	0	0	0	20	20
...overplan_ends_check_legality.err	0	0	0	0	0	0	0
dig_tx_system_dpinassgn.err	0	0	0	0	0	0	0
dig_tx_system_dplace.err	0	0	0	0	0	0	0
..._2_floorplan_ends_floatingPG.err	0	0	0	0	0	0	0
temp_powerplan_ends_lvs.err	20	20	0	0	0	20	20
Short	20	20	0	0	0	20	20
zroute.err	0	0	0	0	0	0	0

#	ID	Status	Color	Type	Layer	Cell Type	Magnitude	Error File Name	Information
6	6		Short	M2 (21)	Physical Only	xofiller		temp_powerpla...	Cell1: xofille
7	7		Short	M2 (21)	Physical Only	xofiller		temp_powerpla...	Cell1: xofille
8	8		Short	M2 (21)	Physical Only	xofiller		temp_powerpla...	Cell1: xofille
9	9		Short	M2 (21)	Physical Only	xofiller		temp_powerpla...	Cell1: xofille
10	10		Short	M2 (21)	Physical Only	xofiller		temp.powerpla...	Cell1: xofille
11	11		Short	M2 (21)	Physical Only	xofiller		temp.powerpla...	Cell1: xofille
12	12		Short	M2 (21)	Physical Only	xofiller		temp.powerpla...	Cell1: xofille
13	13		Short	M2 (21)	Physical Only	xofiller		temp.powerpla...	Cell1: xofille
14	14		Short	M2 (21)	Physical Only	xofiller		temp.powerpla...	Cell1: xofille
15	15		Short	M2 (21)	Physical Only	xofiller		temp.powerpla...	Cell1: xofille
16	16		Short	M2 (21)	Physical Only	xofiller		temp.powerpla...	Cell1: xofille
17	17		Short	M2 (21)	Physical Only	xofiller		temp.powerpla...	Cell1: xofille
18	18		Short	M2 (21)	Physical Only	xofiller		temp.powerpla...	Cell1: xofille
19	19		Short	M2 (21)	Physical Only	xofiller		temp.powerpla...	Cell1: xofille

8: Layer: M2 (21) Type: Short
Cell type: Physical Only
Obj Info :

Figure 2.21: Error Report during Chip Finishing.

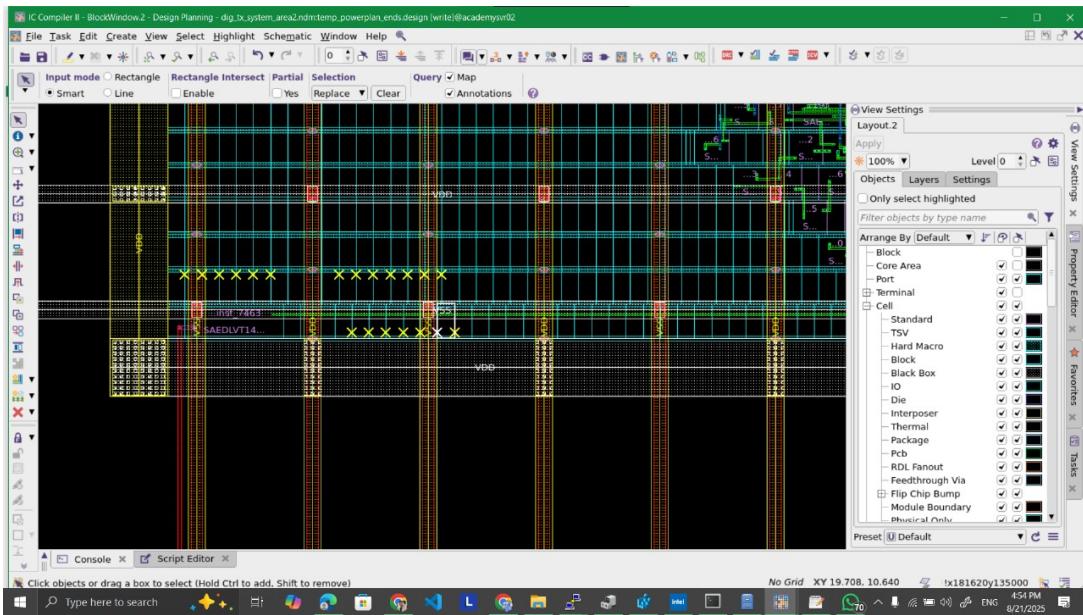


Figure 2.22: DRCs Shorts

```
#####
#####Insert_Filler
set pnr_std_fillers "SAEDLVT14_FILL"
set std_fillers ""
foreach filler $pnr_std_fillers { lappend std_fillers "*${filler}" }
create_stdcell_fillers \
    -lib_cells $std_fillers
#####
#####Use correct ICV version |
set app_options -name signoff.create_metal_fill.runset -value "${icv_mfill_runset}"
signoff_create_metal_fill -select_layers {M2 M6}
#####
#####Preroute_Standard_Cells
set_attribute -objects [get_nets VDD] -name net_type -value power
set_attribute -objects [get_nets VSS] -name net_type -value ground

connect_pg_net -net VDD [get_pins -physical_context */VDD]
connect_pg_net -net VSS [get_pins -physical_context */VSS]
remove_stdcell_fillers_with_violation
check_mv_design
```

Figure 2.23: command for Fixing DRCs

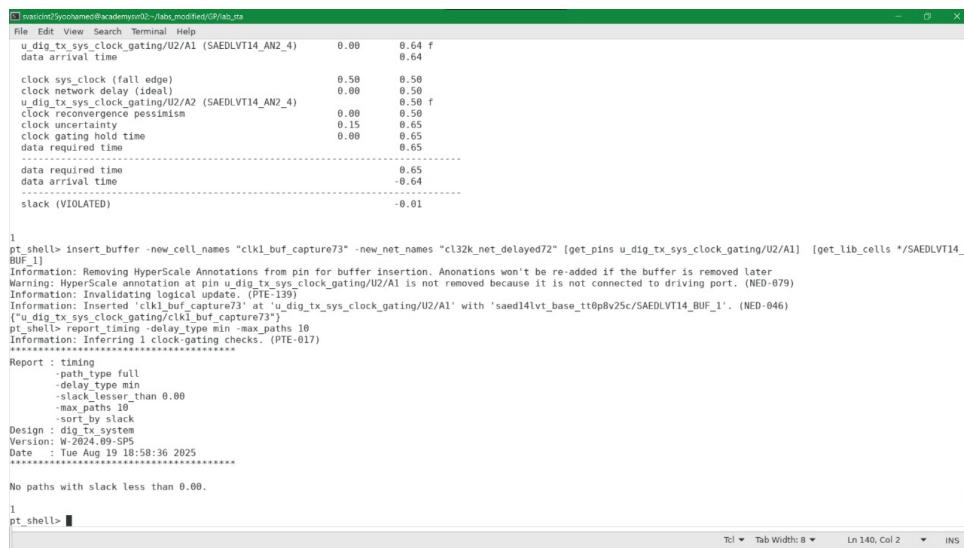
```
1
Information: Detected open violation for Net VDD. BBox: (0.0000 0.0000)(91.9720 91.8000). (RT-585)
Total number of input nets is 3721.
Total number of short violations is 0.
Total number of open nets is 1.
Open nets are VDD
Total number of floating route violations is 0.

Elapsed = 0:00:02, CPU = 0:00:02
1
icc2 shell> □
```

Figure 2.24: LvS after Fixing DRCs

2.9 STA and StarRC (PrimeTime)

The final stage validates timing and parasitics under an area-optimized design. The aim is to ensure that despite minimized area, timing closure is still achieved. The objective is to extract parasitics, run STA, and verify slack.



```

File Edit View Search Terminal Help
u_dig_tx.sys_clock_gating/U2/A1 (SAEDLVT14_AN2_4) 0.00 0.64 f
data arrival time 0.64

clock sys_clock (fall edge) 0.50 0.50
clock network delay (ideal) 0.00 0.50
u_dig_tx.sys_clock_gating/U2/A2 (SAEDLVT14_AN2_4) 0.00 0.50 f
clock reconvergence pessimism 0.00 0.50
clock uncertainty 0.15 0.65
clock gating hold time 0.00 0.65
data required time 0.65
-----
data required time 0.65
data arrival time -0.64
-----
slack (VIOLATED) -0.01

1
pt_shell> insert_buffer -new_cell_names "clk1_buf_capture73" -new_net_names "c132k_net_delayed72" [get_pins u_dig_tx.sys_clock_gating/U2/A1] [get_lib_cells */SAEDLVT14_BUF_1]
Information: Removing HyperScale Annotations from pin for buffer insertion. Annotations won't be re-added if the buffer is removed later
Warning: HyperScale annotation at pin u_dig_tx.sys_clock_gating/U2/A1 is not removed because it is not connected to driving port. (NED-879)
Information: Invalidating logical update. (PTE-139)
Information: Inserted 'clk1_buf_capture73' at 'u_dig_tx.sys_clock_gating/U2/A1' with 'saedl4vt_base_t10p8v25c/SAEDLVT14_BUF_1'. (NED-046)
("u_dig_tx.sys_clock_gating/U2/A1" buf capture73)
pt_drc -report -unitns 1 -minslack 0.00 -max_paths 10
Information: Inferring 1 clock-gating checks. (PTE-017)
*****
Report : timing
    -delay_type full
    -delay_type min
    -slack_lesser_than 0.00
    -max_paths 10
    -sort_by slack
Design : dig_tx_system
Version : 1.0
Date : Tue Aug 19 18:58:36 2025
*****
No paths with slack less than 0.00.

1
pt_shell>

```

Figure 2.25: PrimeTime validation after solving timing in area compilation.

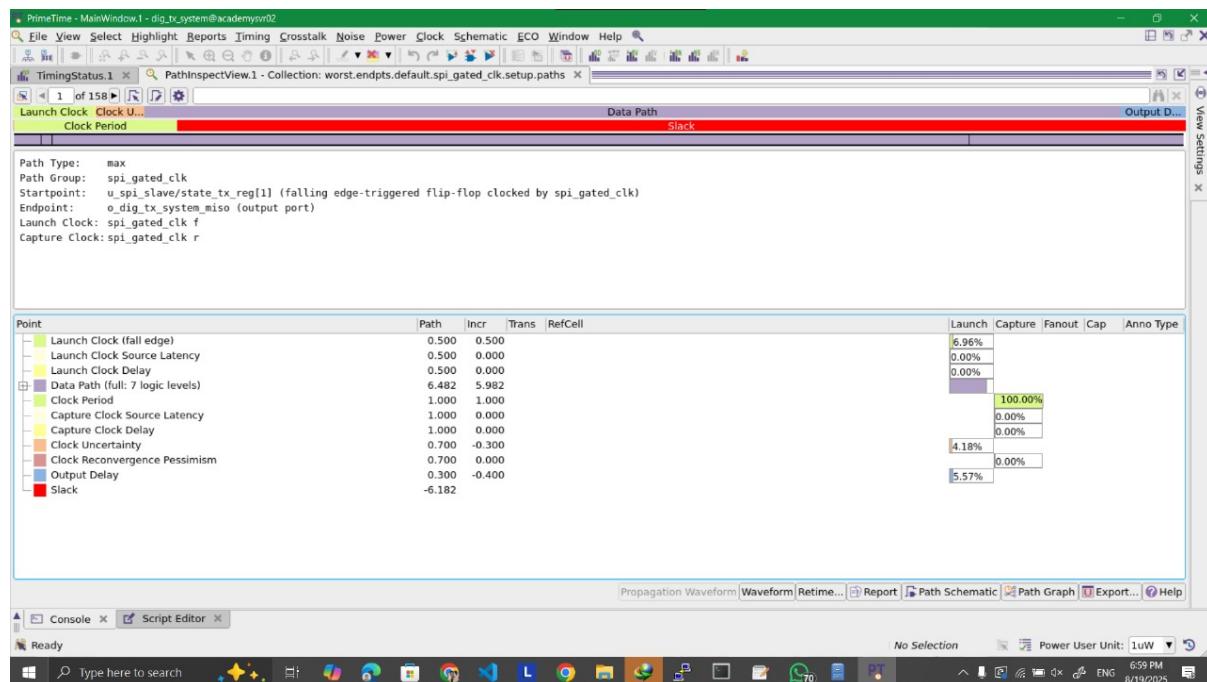


Figure 2.26: Insert Buffer Command

Prime Time was solved by Inserting buffers and fixing hold violations

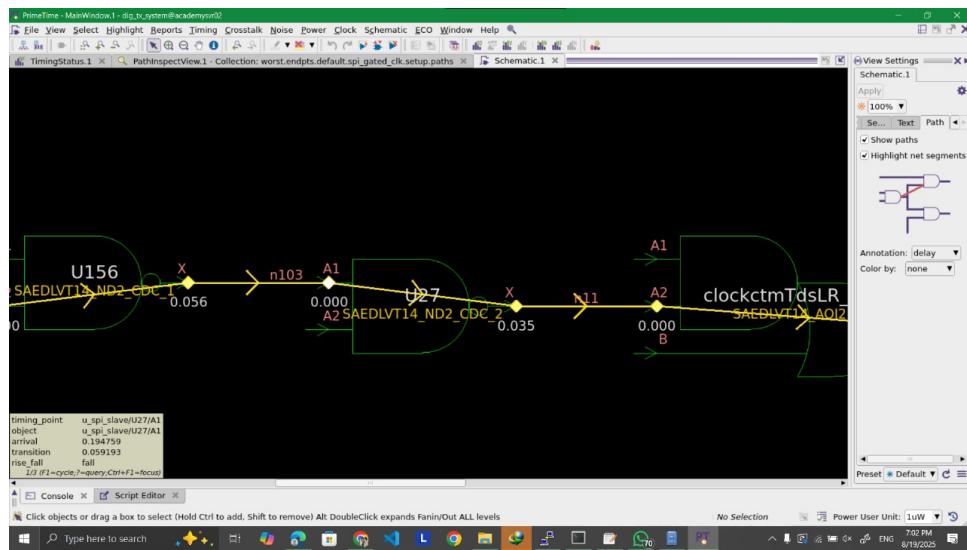


Figure 2.27: Cell schematic.

```

pt_shell> report_delay_calculation -from {u_spi_slave/U27/A1} -to {u_spi_slave/U27/X}
*****
Report Delay Calculation
Design : dig_tx_system
Version: W-2024.09-SP5
Date : Tue Aug 19 19:01:42 2025
*****
From pin: u_spi_slave/U27/A1
To pin: u_spi_slave/U27/X
Main Library Units: 1ns 1pF 1kOhm
Library: 'saed14lvt_base_tt0p8v25c'
Library Units: 1ns 1pF 1kOhm
Library Cell: 'SAEDLVT14_ND2_CDC_2'
arc sense: negative_unate
arc type: cell
Units: 1ns 1pF 1kOhm

Rise Delay
cell delay = 0.0347256 (in library unit)
Table is indexed by

```

Figure 2.28: Delay calculation from point A2 to X .

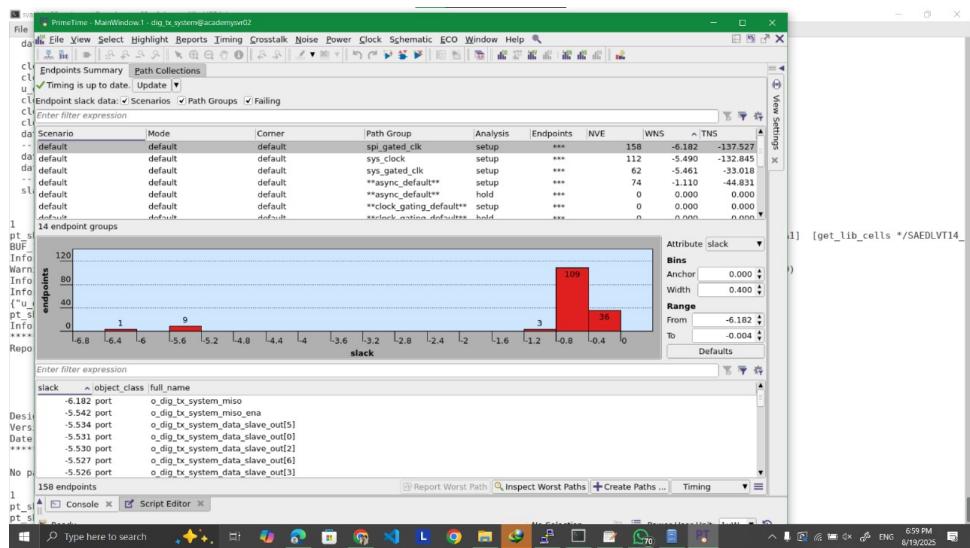


Figure 2.29: Histogram After solving prime time.

```
pt_shell> insert_buffer -new_cell_names "clk_buf_capture156" -new_net_names "cl32k_net_delayed155" [get_pins u_dig_tx_reg_file/reg_file[0][0]/Q] [get_lib_cells */SAEFLV1_WB_11]
```

Figure 2.30: Insert Buffer Command

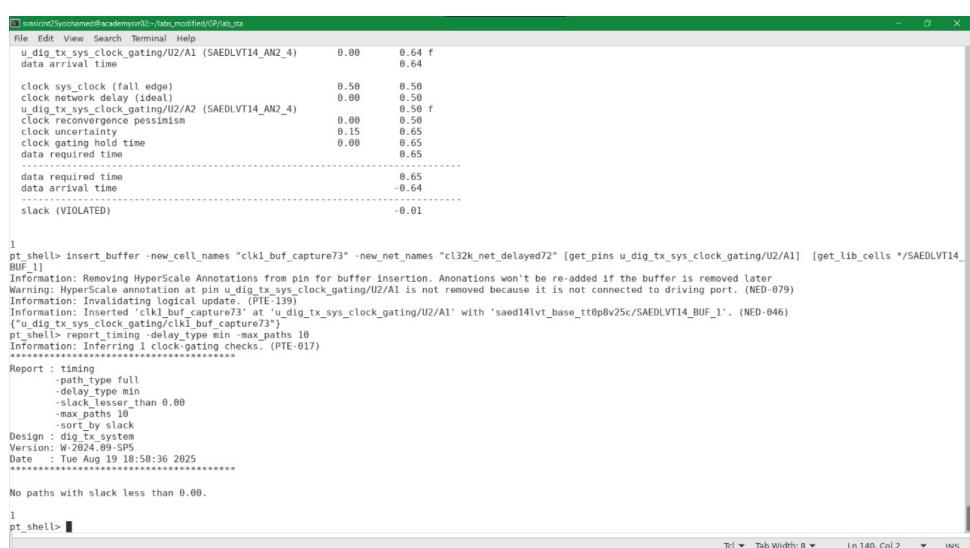


Figure 2.31: PrimeTime validation after solving timing in area compilation.

2.10 Notes2

The reports documented in the previous chapter can be found at the following destination:

/home/svasicint25yoohamed/labs_modified/GP/Work_3/reports

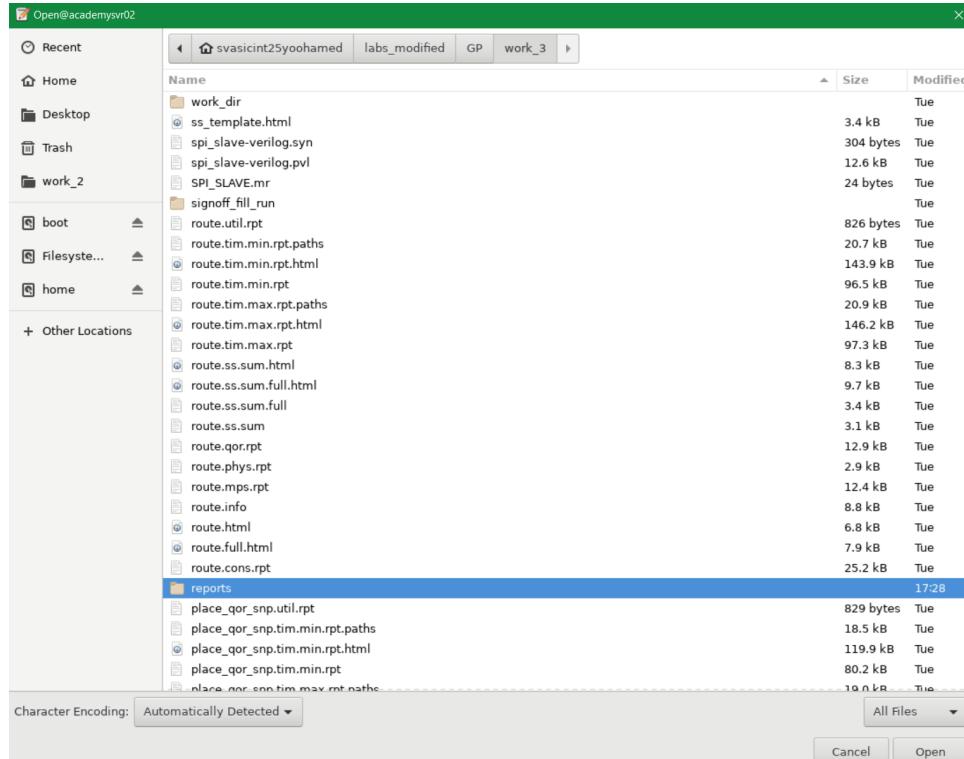


Figure 2.32: Reports Path Destination for Area

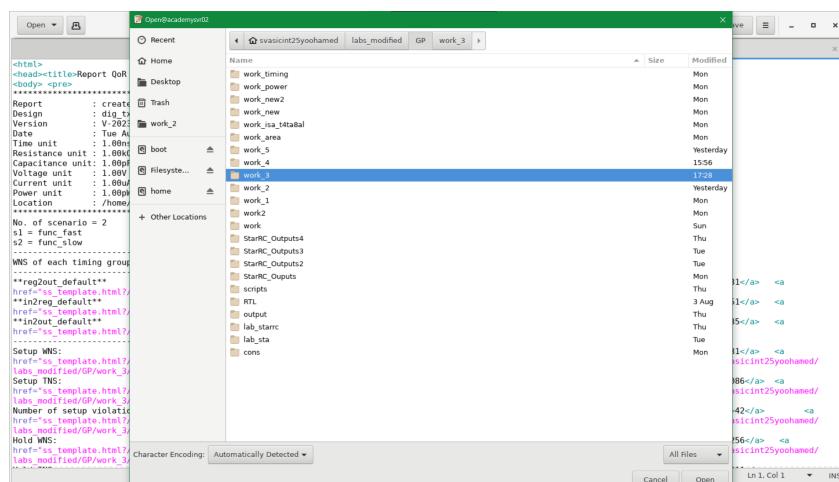


Figure 2.33: Work_3 Destination Path for Area Compilation

Chapter 3

PnR Flow Using Compile for Power

3.1 Compile for Power

The aim and objective of this experiment is to synthesize and implement a digital design that is optimized for low power consumption. The process involves carefully applying power-oriented design strategies at every stage of the flow, including synthesis, floor-planning, power planning, placement, clock tree synthesis (CTS), routing, and chip finishing. By utilizing low-power libraries, applying power-aware constraints, and integrating verification tools such as static timing analysis (STA) and StarRC extraction, the main goal is to reduce both dynamic and leakage power while still maintaining timing closure and functional correctness. This ensures that the final chip not only meets performance requirements but is also energy efficient and reliable.

```
set DESIGN_NAME      "dig_tx_system"
set Constraints_file "/home/svasicint25yoohamed/labs_modified/GP/cons/cons_v2.tcl"
set Constraints_file_sdc "/home/svasicint25yoohamed/labs_modified/GP/work_4/power_dig_tx_system.sdc"
set Core_compile     "/home/svasicint25yoohamed/labs_modified/GP/work_4/power_dig_tx_system.v"
set Warning_file    "${ROOT_DIR}/common/warnings_to_ignore.tcl"
#####
outputs
set Svf_file        "/home/svasicint25yoohamed/labs_modified/GP/output/${DESIGN_NAME}_power.svf"
set ARC_TOP          "/home/svasicint25yoohamed/labs_modified/GP/output/${DESIGN_NAME}_power.ndm"
set Top_design_pt   "/home/svasicint25yoohamed/labs_modified/GP/output/${DESIGN_NAME}_power_pt.v"
#####
#####
```

Figure 3.1: Common Modification for Power

3.2 Compilation

The compilation phase aims to generate a netlist optimized for low power. This involves using low-power standard cell libraries and constraints that prioritize reducing dynamic and leakage power. During this step, the synthesis tool balances between timing closure and power consumption by minimizing unnecessary switching activity and mapping the logic to low-power cells. Figure 3.4 shows the schematic representation of the low-power optimized compilation.

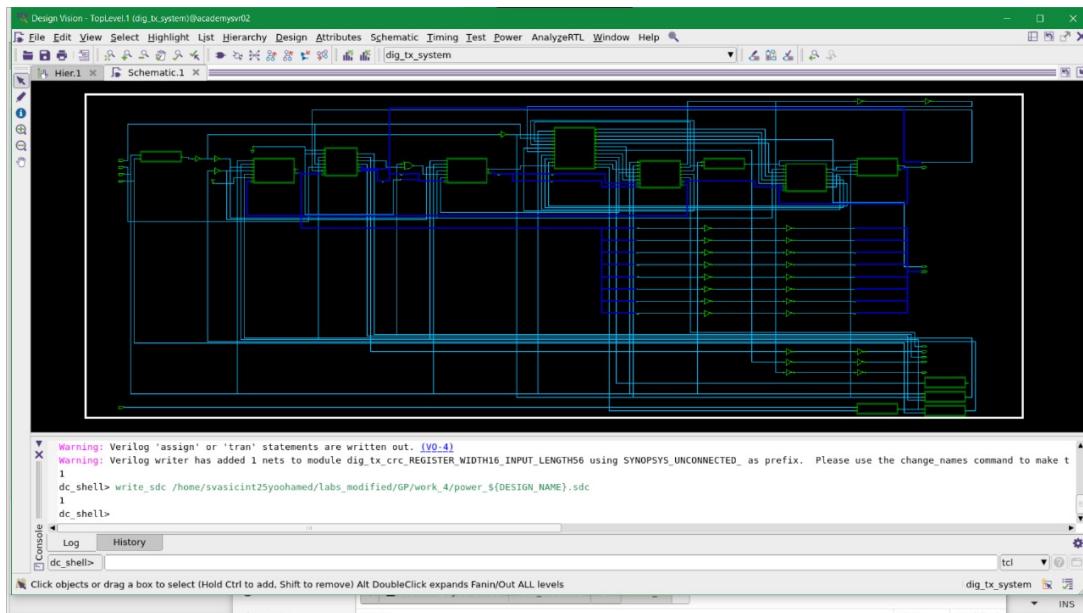


Figure 3.2: Compilation for Power Schematic

```
compile -map_effort medium -area_effort none -power_effort high
```

Figure 3.3: Compile power Script modification .png

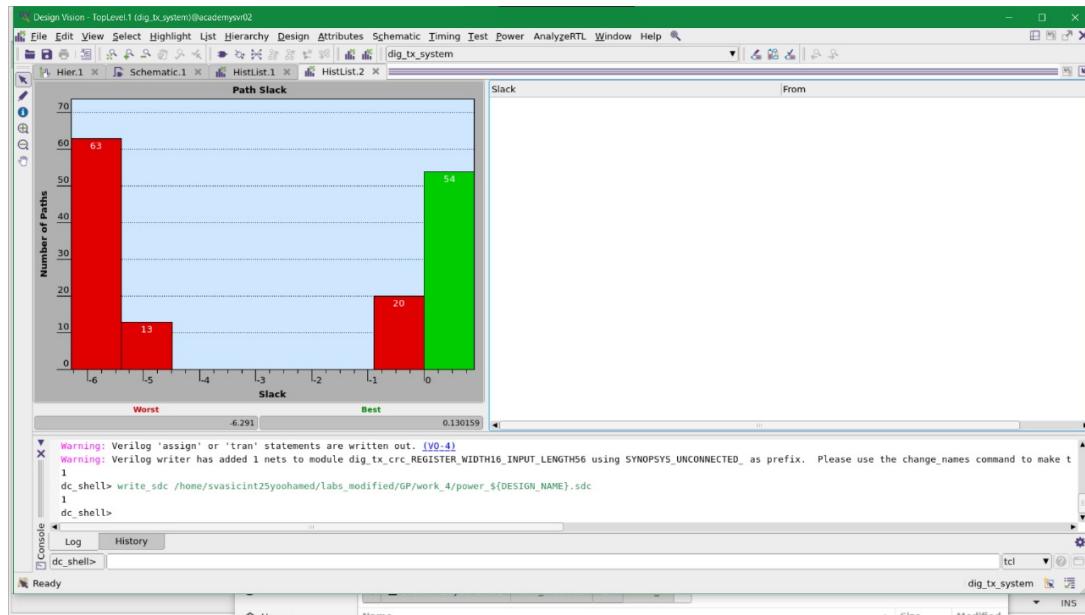


Figure 3.4: Slack histogram for Power Compilation

Combinational area:	1015.472399
Buf/Inv area:	343.078800
Noncombinational area:	393.828003
Macro/Black Box area:	0.000000
Net Interconnect area:	1049.401049
Total cell area:	1409.300402
Total area:	2458.701451

Figure 3.5: Area report

```
Hostname: academysvr02

Compile CPU Statistics
-----
Resource Sharing:          0.91
Logic Optimization:        7.70
Mapping Optimization:      6.67
-----
Overall Compile Time:      34.14
Overall Compile Wall Clock Time: 35.08
-----
Design  WNS: 6.29  TNS: 86.33  Number of Violating Paths: 44

Design (Hold)  WNS: 0.13  TNS: 28.80  Number of Violating Paths: 352
```

Figure 3.6: QoR report

3.3 Data Setup

The data setup phase prepares the design environment by specifying low-power libraries, constraints, and input data. This includes defining operating conditions, loading power-aware timing libraries, and setting up switching activity files (SAIF/VCD) to guide power optimization. Correct preparation at this stage is essential to accurately model and minimize power during later steps.

Figure 3.7 illustrates the setup process.

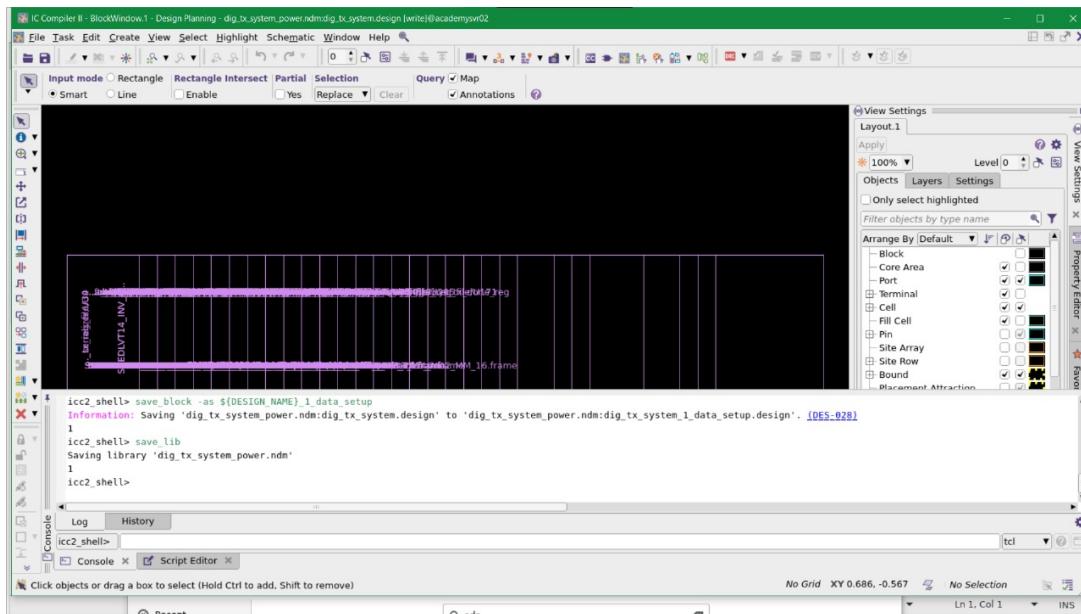


Figure 3.7: Data Setup for Low Power

3.4 Floorplan

The floorplan is designed with power optimization in mind by considering efficient partitioning and macro placement to reduce interconnect lengths, which directly lowers dynamic power. In addition, power domains may be separated to allow voltage scaling or shutoff of unused regions. Figure 3.8 shows the floorplan layout for the power-optimized design.

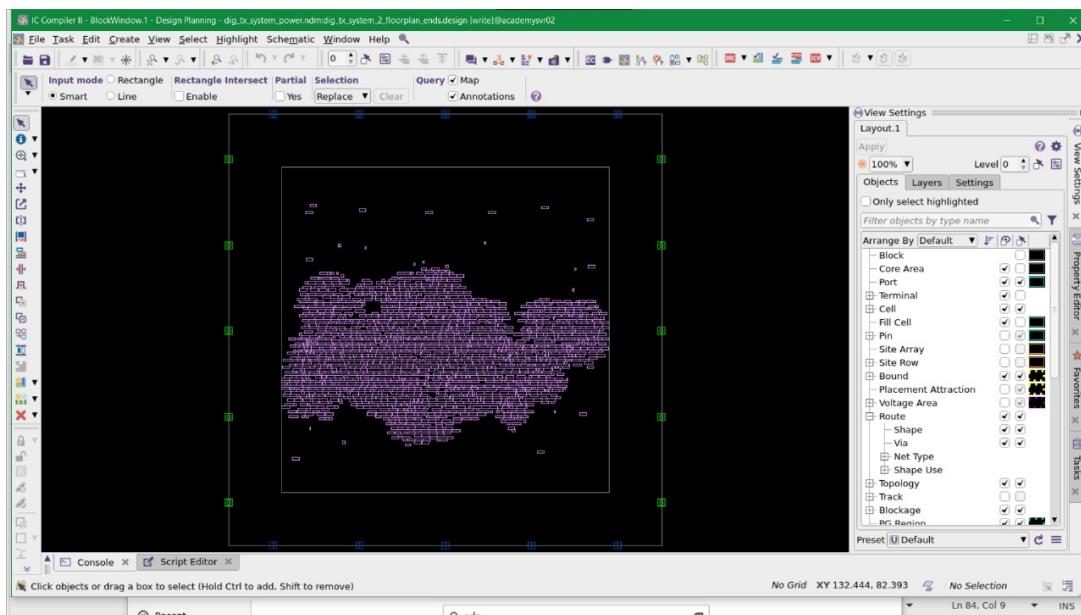


Figure 3.8: Power-Aware Floorplan

3.5 Power Plan

The power plan phase focuses on constructing a robust yet efficient power delivery network. Techniques such as power gating and voltage islands are introduced to minimize both leakage and dynamic consumption. Ensuring even power distribution without excessive IR drop is critical, while maintaining energy efficiency. Figure 3.9 highlights the implemented power grid.

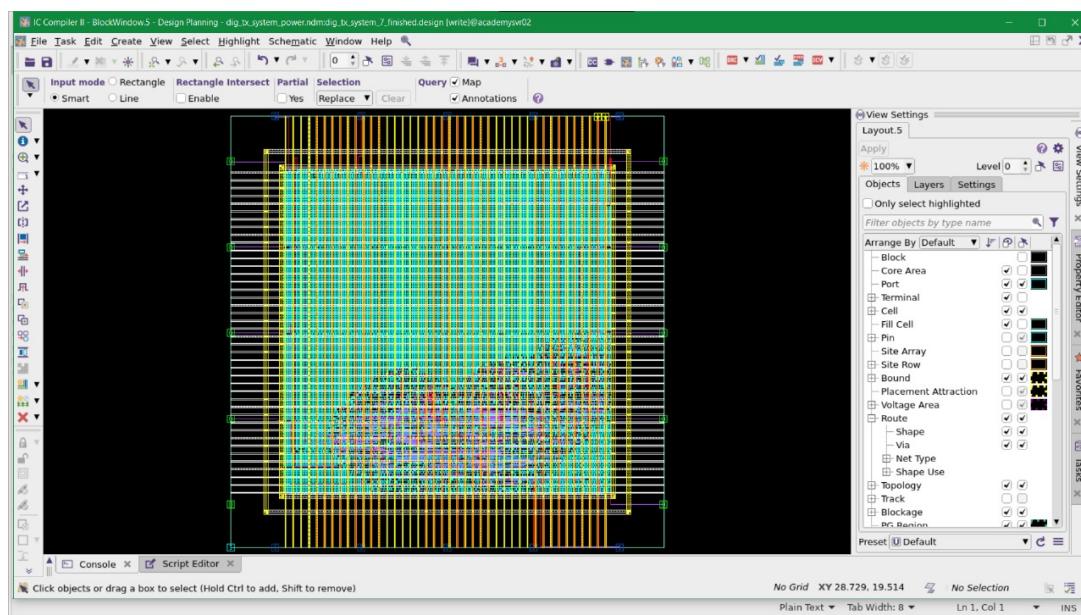


Figure 3.9: Power Plan Grid Implementation

3.6 Placement

Placement arranges the standard cells in a manner that reduces power leakage and avoids excessive switching activity. Power-aware placement techniques consider both congestion and toggle activity, distributing cells efficiently across the floorplan to balance timing and energy efficiency. Figure 3.20 illustrates the placement results.

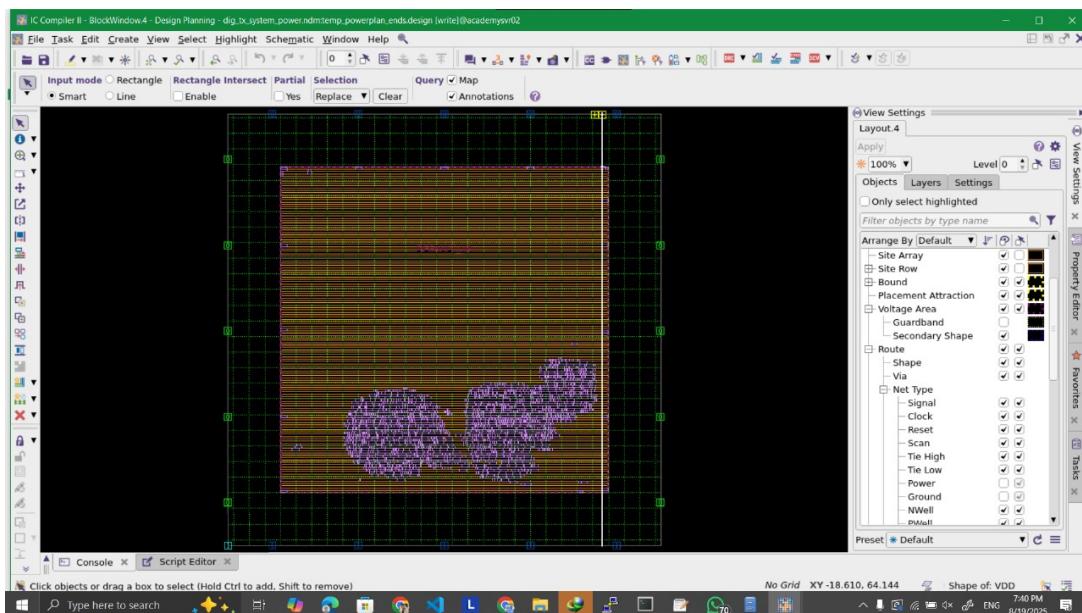


Figure 3.10: Low-Power Cell Placement

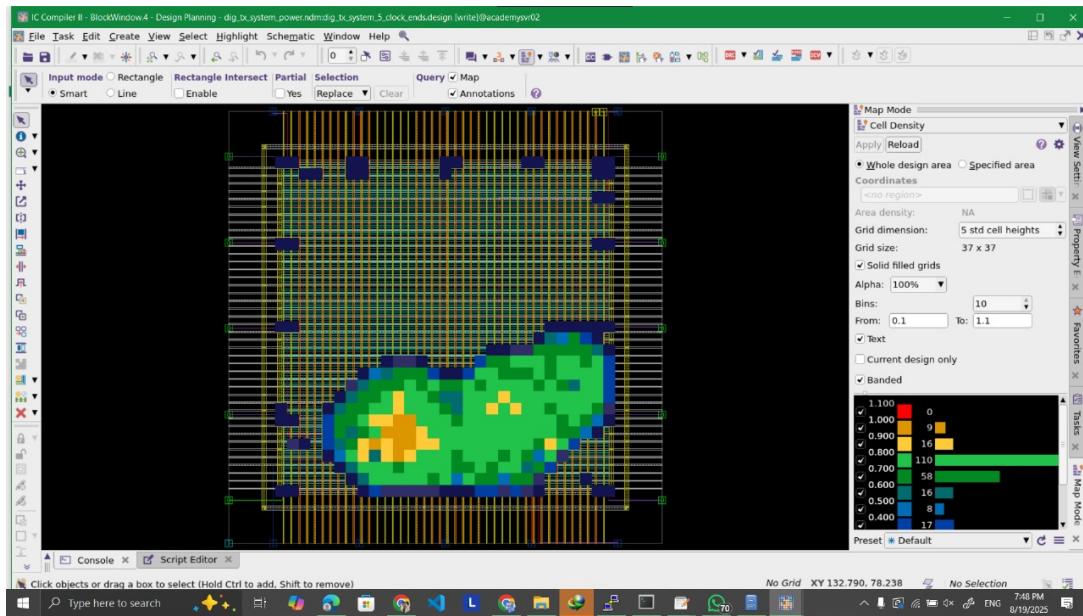


Figure 3.11: Cell density

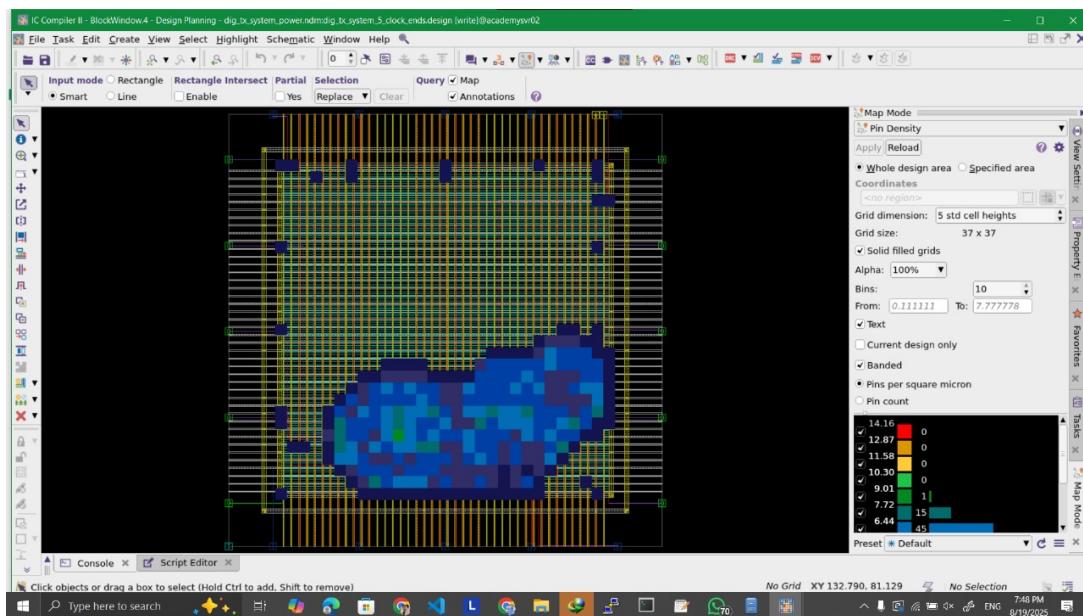


Figure 3.12: Pin density

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-6.874	0.000	-0.056	-6.874	-6.124
TNS	-92.782	0.000	-0.892	-85.767	-6.124
NUM	42	0	27	14	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.199	-0.199	0.000	0.000	0.000
TNS	-39.231	-39.231	0.000	0.000	0.000
NUM	376	376	0	0	0

Figure 3.13: Placement global timing report

3.7 CTS

Clock Tree Synthesis (CTS) is one of the most critical contributors to dynamic power. The objective here is to design the clock tree with minimal buffer insertion, shorter routing, and balanced clock paths to reduce power usage while maintaining low skew. Power-efficient CTS techniques significantly impact overall energy consumption. Figure 3.14 shows the synthesized clock tree.

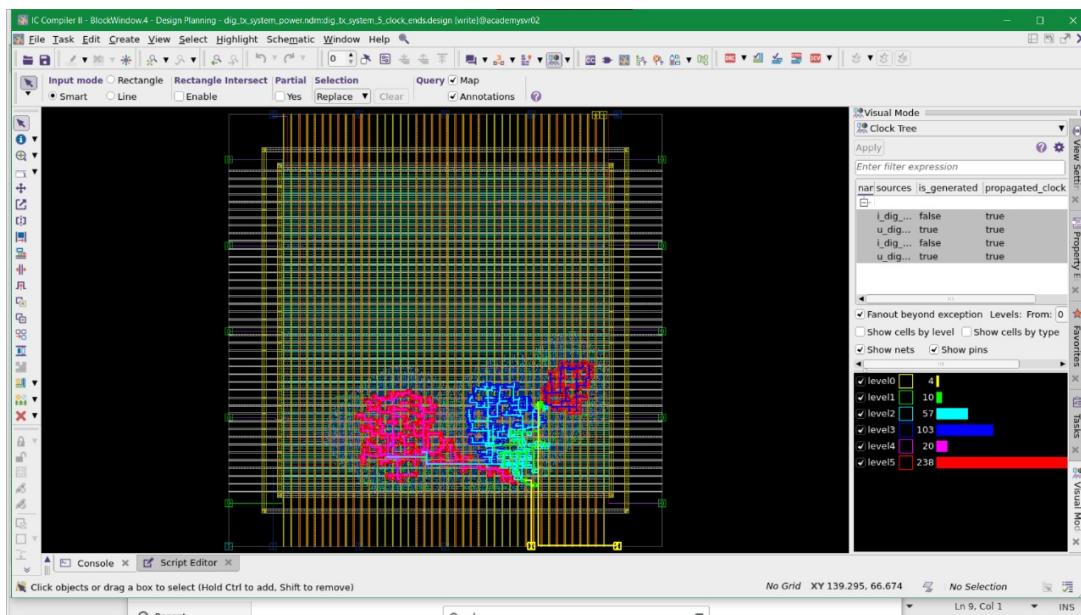


Figure 3.14: Clock Tree Synthesis for Low Power

Setup violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-7.36	-0.00	-0.21	-7.36	-6.28
TNS	-96.38	-0.00	-5.54	-84.56	-6.28
NUM	43	1	27	14	1

Hold violations					
	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.13	-0.13	0.00	0.00	0.00
TNS	-0.38	-0.38	0.00	0.00	0.00
NUM	7	7	0	0	0

Figure 3.15: CTS global timing

3.8 Routing

In the routing stage, the wires are connected in a way that minimizes capacitance and crosstalk, both of which contribute to dynamic power. Power-aware routing ensures optimal path lengths, avoids unnecessary coupling, and balances timing with reduced energy overhead. Figure 3.16 shows the routing results of the low-power design.

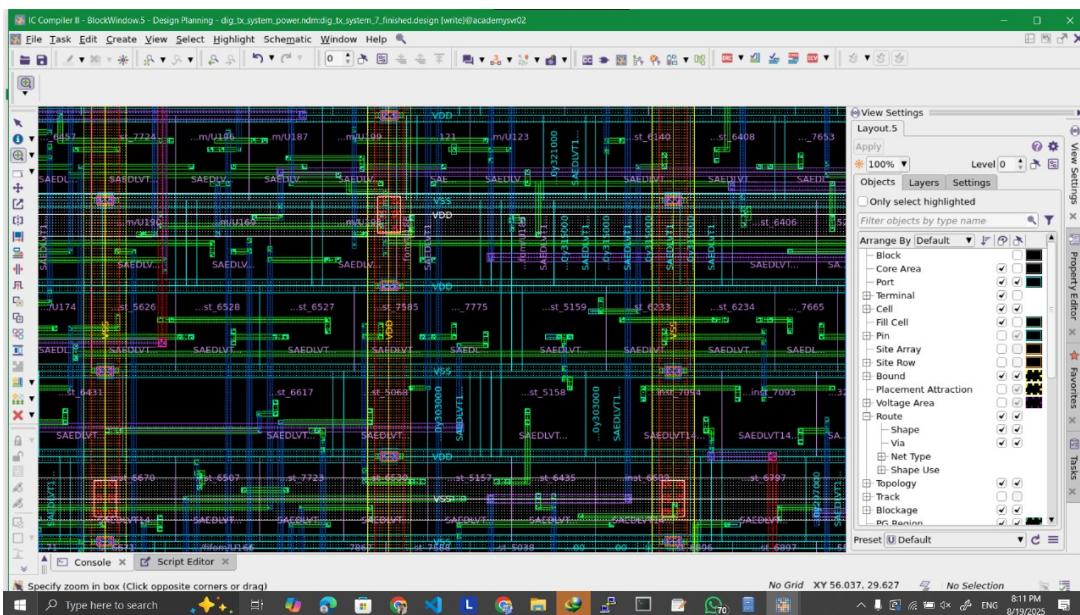


Figure 3.16: Power-Aware Routing

Setup violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-7.422	-0.001	-0.205	-7.422	-6.343
TNS	-97.160	-0.001	-5.543	-85.273	-6.343
NUM	43	1	27	14	1

Hold violations

	Total	reg->reg	in->reg	reg->out	in->out
WNS	-0.126	-0.126	0.000	0.000	0.000
TNS	-0.382	-0.382	0.000	0.000	0.000
NUM	17	17	0	0	0

Figure 3.17: Routing Global timing report

3.9 Chip Finishing

The chip finishing stage includes filler insertion, metal fill, and final verification steps. In a low-power flow, fillers and metal fills are carefully optimized to maintain power integrity without unnecessary overhead. Figure 3.18 shows the chip finishing process. DRCs faced in this station unfortunately could not be solved as its along the design.

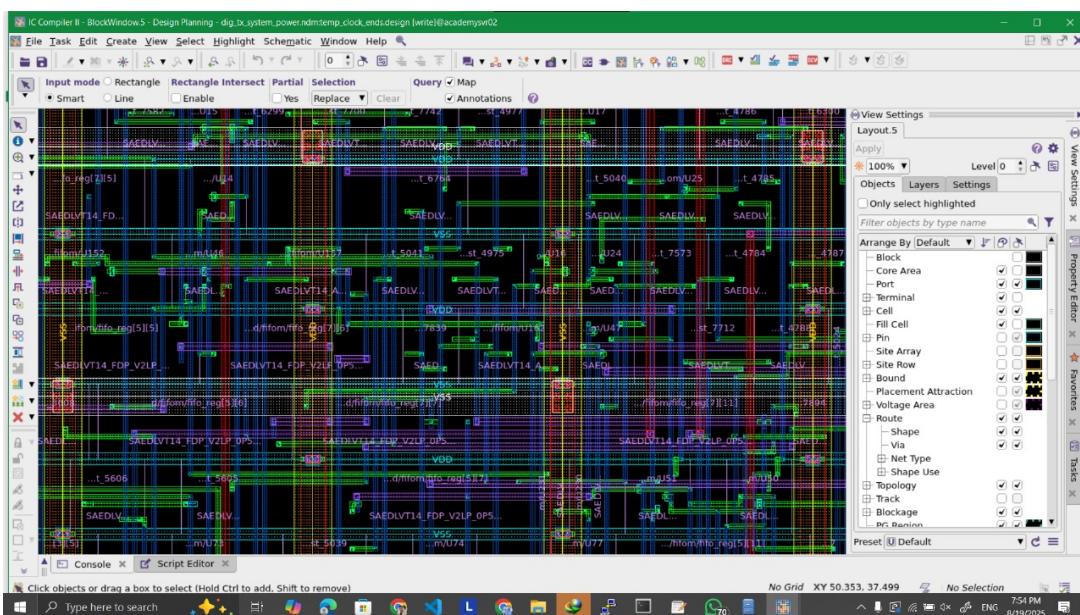


Figure 3.18: Chip Finishing with Power Optimization

```

dig_tx_system.lvs.rpt
~/lvs_moduledir/work_4/reports

[Check Short] Stage 1-2 Elapsed = 0:00:00, CPU = 0:00:00
[Check Short] Stage 2 Elapsed = 0:00:00, CPU = 0:00:00
[Check Short] Stage 2-2 Elapsed = 0:00:01, CPU = 0:00:01
[Check Short] Stage 3 Elapsed = 0:00:01, CPU = 0:00:01
[Check Short] End Elapsed = 0:00:01, CPU = 0:00:01
[Check Net] init Elapsed = 0:00:01, CPU = 0:00:01
[Check Net] Warning: Port VDD have no valid pin shapes. Skip this port. (RT-283)
[Check Net] Warning: Port VSS have no valid pin shapes. Skip this port. (RT-283)
[Check Net] 10% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 20% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 30% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 40% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 50% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 60% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 70% Elapsed = 0:00:02, CPU = 0:00:02
[Check Net] 80% Elapsed = 0:00:03, CPU = 0:00:03
[Check Net] 90% Elapsed = 0:00:03, CPU = 0:00:03
[Check Net] 100% Elapsed = 0:00:03, CPU = 0:00:03
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[0][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[1][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[2][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[3][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[4][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[5][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
Warning: Net u_dig_tx_asyn_fifo_read/fifom/fifo[6][11] has less than 2 valid port. Skip open checking for this net. (RT-204)
[Check Net] All nets are submitted.
[Check Net] 100% Elapsed = 0:00:03, CPU = 0:00:03
Information: Detected open violation for Net VDD. BBox: (0.0000 0.0000)(110.9160 110.4000). (RT-585)

=====
Maximum number of violations is set to 20
Abort checking when more than 20 violations are found
All violations might not be found.
=====
Total number of input nets is 3838.
Total number of short violations is 0.
Total number of open nets is 1.
Open nets are VDD.
Total number of floating route violations is 0.

Elapsed = 0:00:03, CPU = 0:00:03
1

```

Figure 3.19: LVS report

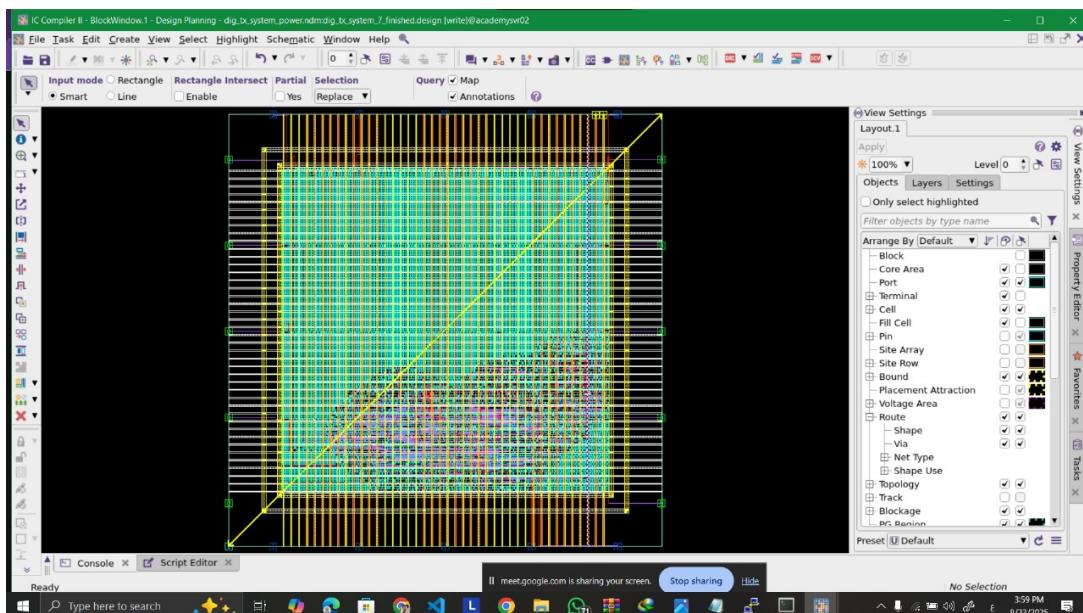


Figure 3.20: open DRC

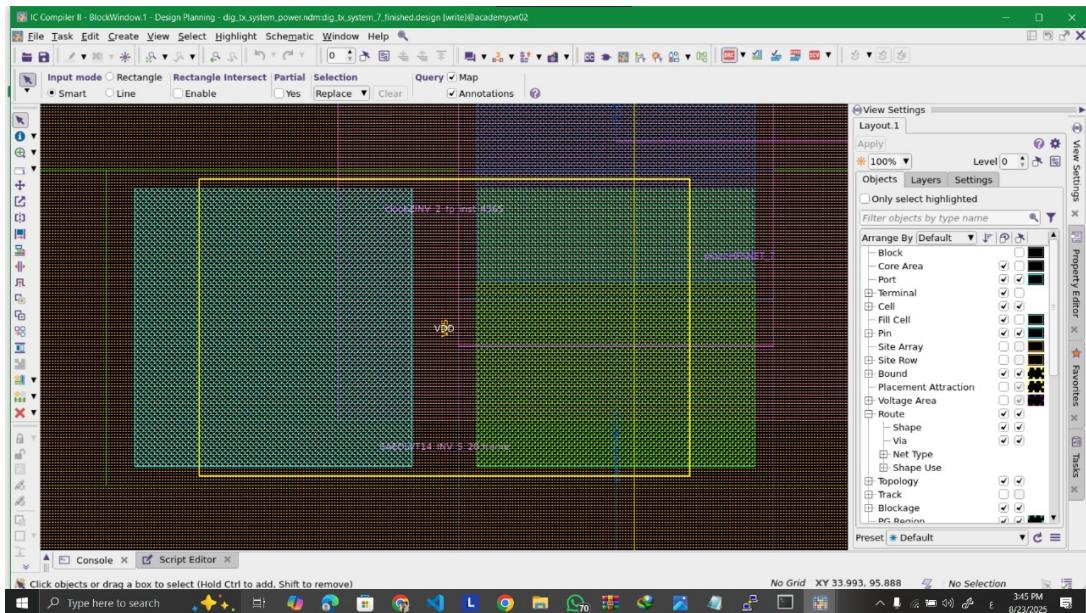


Figure 3.21: Zoomed open DRC

3.10 StarRC and STA

Finally, parasitic extraction using StarRC and verification through Static Timing Analysis (STA) are performed. The objective is to ensure that the design meets both timing closure and power requirements. Reports such as delay calculation, power estimation, and histogram analysis (Figures 3.26, 3.27, and ??) confirm whether the optimizations have successfully reduced power while preserving functional correctness.

```

svacim25yoahamed@academyv02:~/labs_modified/0/lab_sta
File Edit View Search Terminal Help
u_dig_tx_spi_clock_gating/U2/A1 (SAEDLVT14_AN2_MM_6)
  data arrival time          0.00      0.64 f
  data required time         0.64
  clock spi_clock (fall edge) 0.50      0.50
  clock network delay (ideal) 0.00      0.50
  u_dig_tx_spi_clock_gating/U2/A2 (SAEDLVT14_AN2_MM_6)
  clock reconvergence pessimism 0.00      0.50
  clock uncertainty           0.15      0.65
  clock gating hold time     0.00      0.65
  data required time          0.65
  data arrival time           0.64
  slack (VIOLATED)           -0.01

1
pt_shell> insert_buffer -new_cell_names "clk1_buf_capture194" -new_net_names "cl32k_net_delayed193" [get_pins u_dig_tx_spi_clock_gating/enable_latch_reg/0] [get_lib_cells *SAEDLVT14_BUF_1]
Information: Removing HyperScale Annotations from pin for buffer insertion. Annotations won't be re-added if the buffer is removed later
Information: Invalidating logical update. (PTE-139)
Information: Inserted 'clk1_buf_capture194' at 'u_dig_tx_spi_clock_gating/enable_latch_reg/0' with 'saedl4lvt_base_tt0p8v25c/SAEDLVT14_BUF_1'. (NED-046)
("u_dig_tx_spi_clock_gating/clk1_buf_capture194")
pt_shell> report_timing -delay_type min -max_paths 10
Information: Inferring 1 clock-gating checks. (PTE-017)
*****
Report : timing
  -path_type full
  -delay_type min
  -slack_lesser_than 0.00
  -max_paths 10
  -sort_by slack
Design : dig_tx system
Version: W-2024.09-SP5
Date  : Tue Aug 19 20:36:38 2025
*****
No paths with slack less than 0.00.

1
pt_shell>

```

Figure 3.22: Prime Time after solving

SYNTAX

```
integer remove_cells
  [-design design]
  [-force]
  [cells]
  [-all]
```

Data Types

<i>design</i>	<i>collection</i>
<i>cells</i>	<i>collection</i>

Figure 3.23: Slack Solved Using remove cell

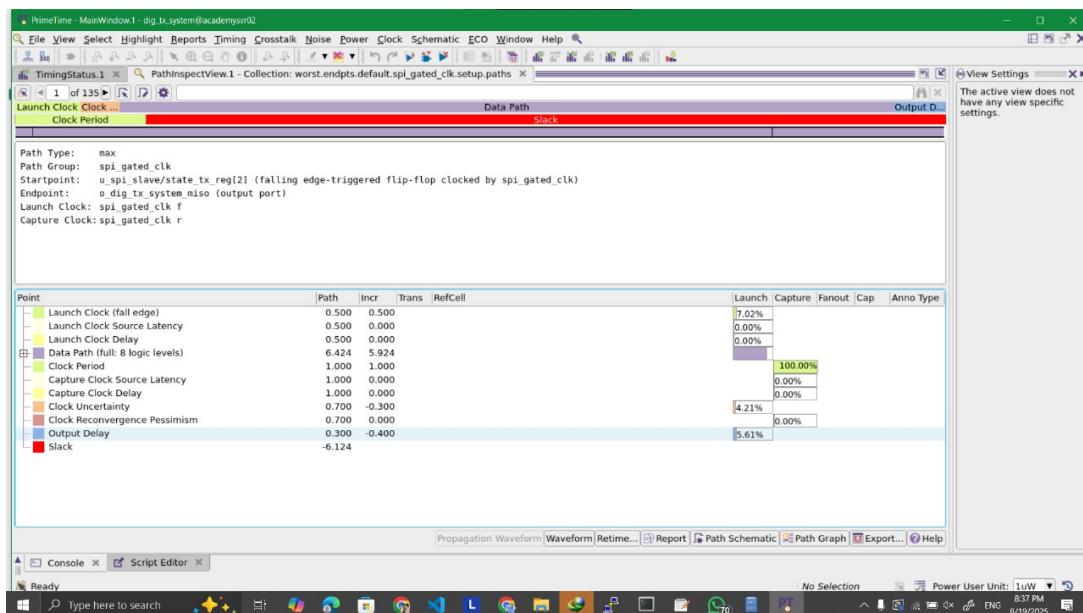


Figure 3.24: path inspection

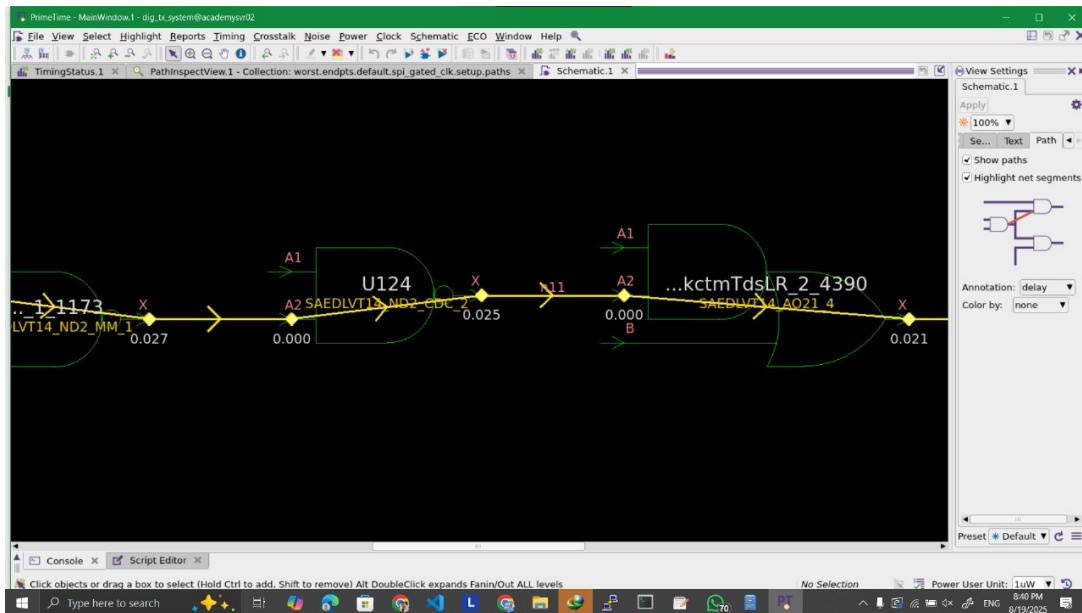


Figure 3.25: Cell schematic

```

pt_shell> report.delay_calculation -from {u_spi_slave/U124/A2} -to {u_spi_slave/U124/X}
*****
Report : delay_calculation
Design : dig_tx_system
Version: W-2024.09-SP5
Date   : Tue Aug 19 20:39:42 2025
*****
From pin: u_spi_slave/U124/A2
To pin:  u_spi_slave/U124/X
Main Library Units: Ins 1pF 1kOhm
Library: 'saed14lvt_base_tt0pV25c'
Library Units: Ins 1pF 1kOhm
Library Cell: 'SAEDLVT14_ND2_CDC_2'
arc sense:          negative_unate
arc type:           cell
Units:  Ins 1pF 1kOhm

Rise Delay
cell delay = 0.0249415 (in library unit)
Table is indexed by

```

Figure 3.26: Delay Calculation Reports

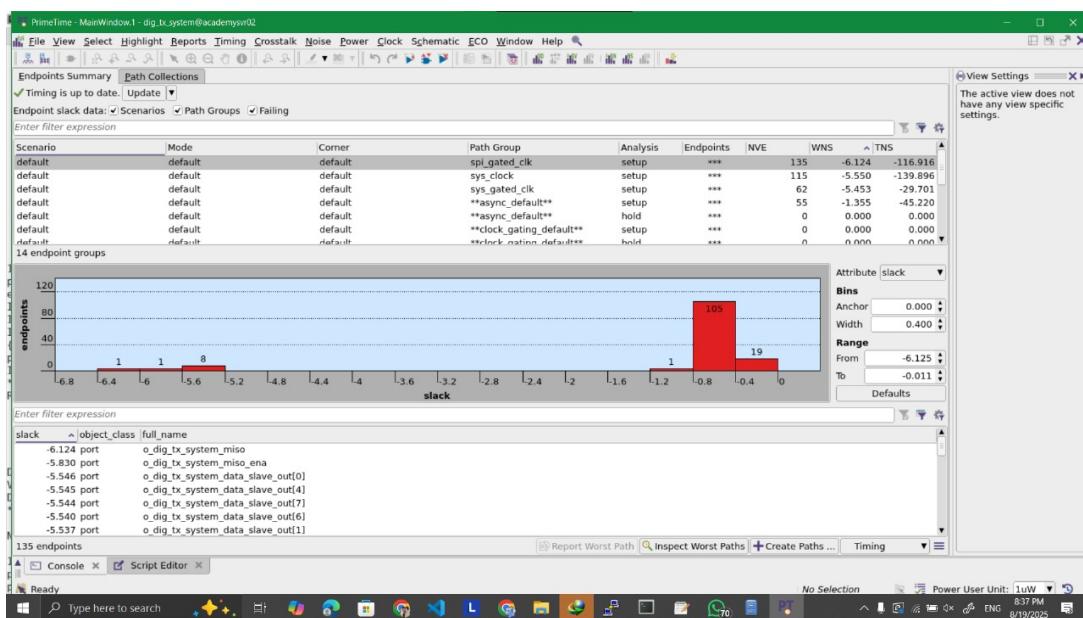


Figure 3.27: Histogram After PrimeTime

3.11 Notes3

The reports documented in the previous chapter can be found at the following destination:

/home/svasicint25yoohamed/labs_modified/GP/Work_4/reports

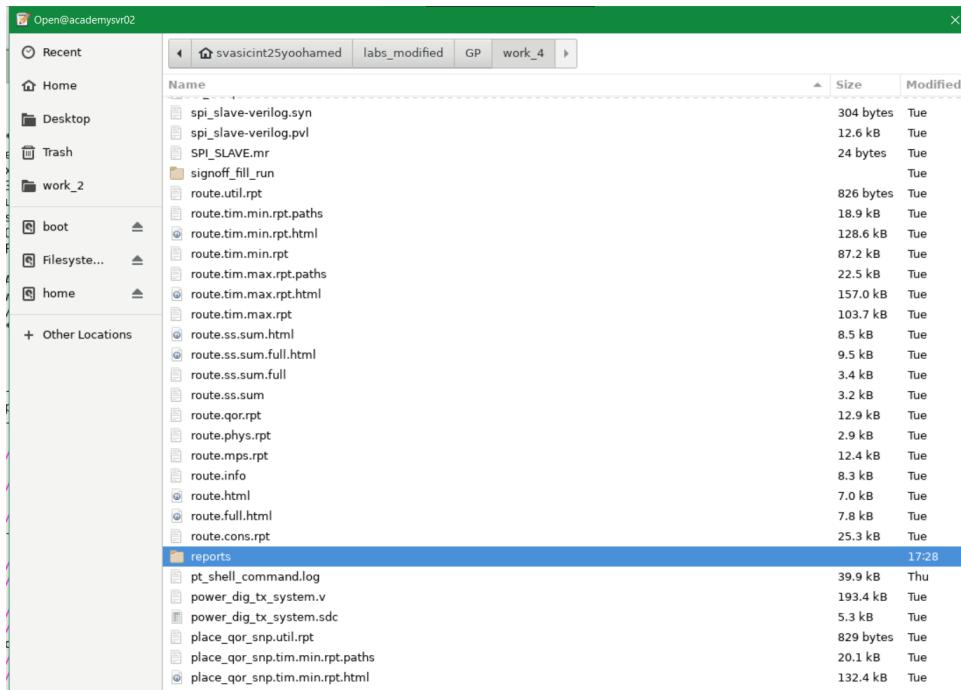


Figure 3.28: Reports Path Destination for Power

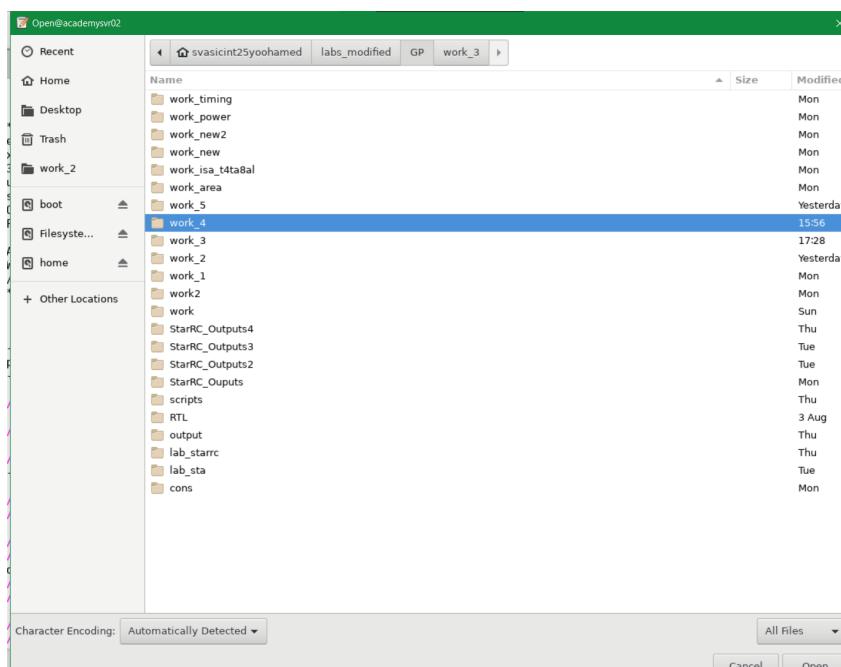


Figure 3.29: Work_4 Destination Path for Power Compilation