Instructions to be implemented in the project:

- DADDI
- DSUBI
- ADD.D
- ADD.S
- SUB.D
- SUB.S
- MUL.D
- MUL.S
- DIV.D
- DIV.S
- LW
- LD
- L.S
- L.D
- SW
- SD
- S.S
- S.D
- BNE
- BEQ

Cache Simulation:

The only required miss is the compulsory miss (the first one when cache is empty), every other cache access should be a hit afterwards.

The first miss should lead to bringing the block from the memory to the cache in X cycles while Tumasulo is executing other instructions, the block should include all the elements needed for the program.