CENTER OF NANOELECTRONICS & DEVICES

DESIGN AND COMPLETE LAYOUT OF SAR-LOGIC CHIPLET

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Submitted by: Section 10 - CND211_Group 5

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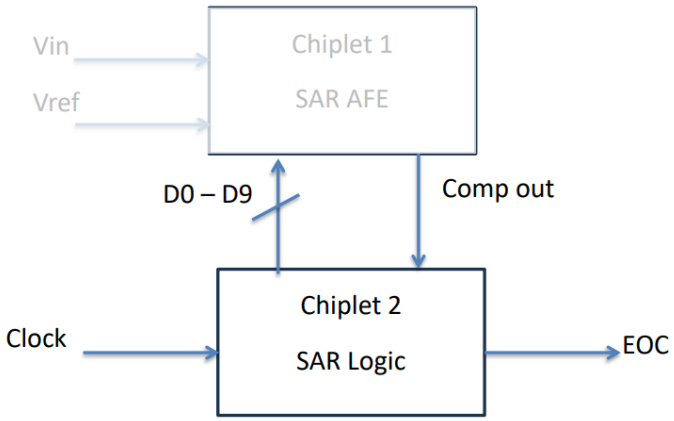
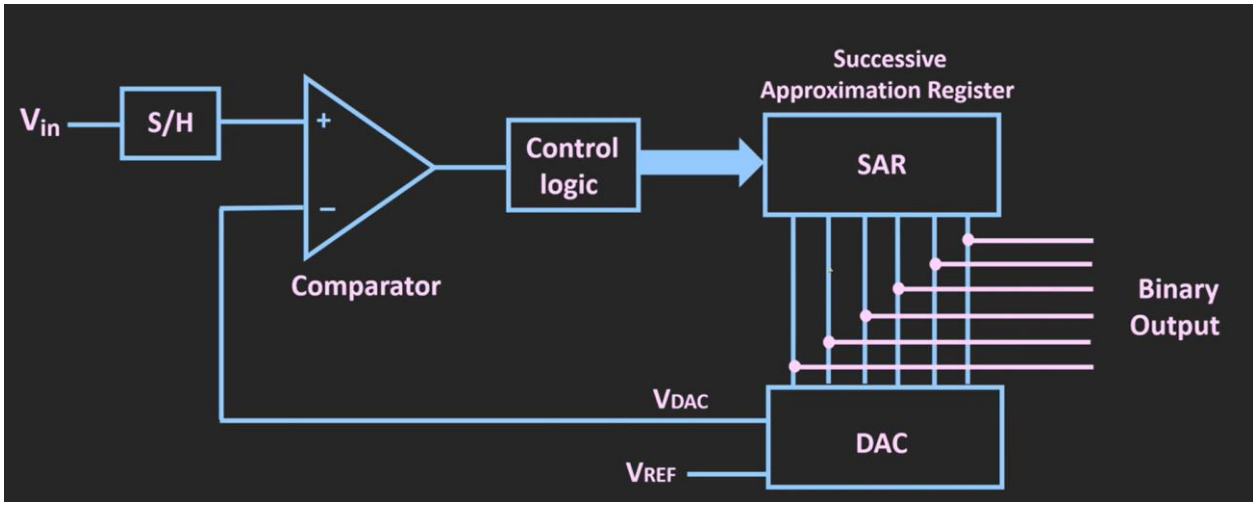
Introduction

- ***Project Overview:*** The project aims to develop a 10-bit Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) with a 100 MS/s sampling rate. This device is intended for high-speed signal processing applications, requiring meticulous design optimization to meet timing, power, and area specifications.
- ***Tools Used:*** The scripts indicate the use of Synopsys tools and the SAED90nm technology library for design and analysis.





SAR ADC Logic RTL design and Testbench

Figure 1

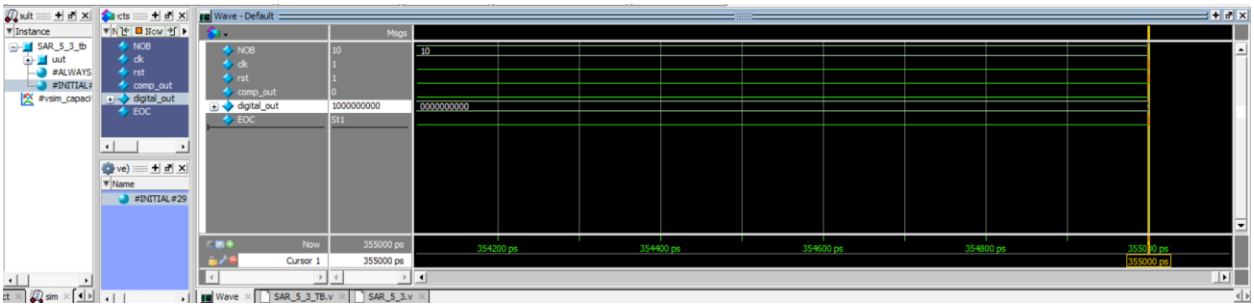


Figure 2

```
# Time:                   50, State:  0, sar_reg: 0000000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                  150, State:  0, sar_reg: 0000000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                  250, State:  1, sar_reg: 0000000000, comp_out: 1, digital_out:    0, EOC: 0
# Time:                  350, State:  2, sar_reg: 1000000000, comp_out: 1, digital_out:    0, EOC: 0
# Time:                  450, State:  3, sar_reg: 1000000000, comp_out: 1, digital_out:    0, EOC: 0
# Time:                  550, State:  1, sar_reg: 1000000000, comp_out: 1, digital_out:    0, EOC: 0
# Time:                  650, State:  2, sar_reg: 1100000000, comp_out: 1, digital_out:    0, EOC: 0
# Time:                  750, State:  3, sar_reg: 1100000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                  850, State:  1, sar_reg: 1000000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                  950, State:  2, sar_reg: 1010000000, comp_out: 1, digital_out:    0, EOC: 0
# Time:                 1050, State:  3, sar_reg: 1010000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 1150, State:  1, sar_reg: 1000000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 1250, State:  2, sar_reg: 1001000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 1350, State:  3, sar_reg: 1001000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 1450, State:  1, sar_reg: 1000000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 1550, State:  2, sar_reg: 1000100000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 1650, State:  3, sar_reg: 1000100000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 1750, State:  1, sar_reg: 1000000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 1850, State:  2, sar_reg: 1000010000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 1950, State:  3, sar_reg: 1000010000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 2050, State:  1, sar_reg: 1000000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 2150, State:  2, sar_reg: 1000001000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 2250, State:  3, sar_reg: 1000001000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 2350, State:  1, sar_reg: 1000000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 2450, State:  2, sar_reg: 1000000100, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 2550, State:  3, sar_reg: 1000000100, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 2650, State:  1, sar_reg: 1000000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 2750, State:  2, sar_reg: 1000000010, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 2850, State:  3, sar_reg: 1000000010, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 2950, State:  1, sar_reg: 1000000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 3050, State:  2, sar_reg: 1000000001, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 3150, State:  3, sar_reg: 1000000001, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 3250, State:  1, sar_reg: 1000000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 3350, State:  2, sar_reg: 1000000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 3450, State:  3, sar_reg: 1000000000, comp_out: 0, digital_out:    0, EOC: 0
# Time:                 3550, State:  4, sar_reg: 1000000000, comp_out: 0, digital_out:    0, EOC: 0
# Test SUCCESS: Output =  512 and EOC = 1
# ** Note: $finish    : E:/AUC_Advanced/Advanced Digital Design/pojects/final/rtl/SAR_5_3_TB.v(56)
#    Time: 355 ns  Iteration: 2  Instance: /SAR_5_3_tb
```

RTL DESIGN

```
module SAR_ADC_5_3 (
  input wire clk,         // Clock input
  input wire rst,         // Reset input
 // input wire start,       // Start conversion
  input wire comp_out,     // Comparator output
  output reg [9:0] digital_out, // 10-bit Digital output of ADC
  output reg EOC          // End of conversion signal
);
reg [9:0] sar_reg;          // SAR register
reg [3:0] state;            // State control
integer i;
// State definitions
localparam IDLE = 0,
       INIT = 1,
       COMPARE = 2,
       UPDATE = 3,
       FINISH = 4;
always @(posedge clk or posedge rst) begin
  if (rst) begin
    sar_reg <= 10'b0;
    digital_out <= 10'b0;
    state <= IDLE;
    EOC <= 0;
    i <= 9;  // Start with MSB
  end else begin
```

```
case (state)
    IDLE: begin
      //if (start) begin
         sar_reg <= 10'b0;
         state <= INIT;
         i <= 9;  // Start with MSB
      // end
    end
    INIT: begin
      sar_reg[i] <= 1;  // Set the current bit to 1
      state <= COMPARE;
    end
    COMPARE: begin
      state <= UPDATE;
    end
    UPDATE: begin
      if (comp_out == 0)
         sar_reg[i] <= 0;  // Set current bit to 0 if comparator is low
      i <= i - 1;              end
    COMPARE: begin
      state <= UPDATE;
    end
```

```
        UPDATE: begin
            if (comp_out == 0)
                sar_reg[i] <= 0;  // Set current bit to 0 if comparator is low
            i <= i - 1;        // Move to next bit
            if (i < 0)
                state <= FINISH;
            else
                state <= INIT;
        end
        FINISH: begin
            digital_out <= sar_reg;  // Output the final value
            EOC <= 1;
            state <= IDLE;
        end
    endcase
  end
  // Debugging output
  $display("Time: %t, State: %d, sar_reg: %b, comp_out: %b, digital_out: %d, EOC: %b", $time, state, sar_reg,
comp_out, digital_out, EOC);
end


endmodule
```

TEST BENCH

```
`timescale 1ns / 100ps

module SAR_5_3_tb;

parameter NOB = 10;  // Number of bits (10-bit)

// Inputs

reg clk;

reg rst;

//reg start;

reg comp_out;

// Outputs

wire [NOB-1:0] digital_out;

wire EOC;  // End of Conversion signal

// Instantiate the Unit Under Test (UUT)

SAR_ADC_5_3 uut (

   .clk(clk),

   .rst(rst),

   .comp_out(comp_out),

   .digital_out(digital_out),

   .EOC(EOC)

);

// Clock generation

always #5 clk = ~clk;  // Clock period of 10ns
```

```
initial begin
  // Initialize Inputs
  clk = 0;
  rst = 1; // Assert reset initially
  //start = 1;
  comp_out = 0;

  // Reset deassertion and start signal management
  #10 rst = 0;  // Deassert reset
  //#5 start = 1; #5; // Pulse start signal
  //start = 0;
  // Simulate ADC behavior
  repeat (10) begin  // Simulate for 10 cycles as example
    @(posedge clk);
    comp_out = (uut.sar_reg > 512) ? 0 : 1;  // Change comparator output based on sar_reg
  end

  // Check results after conversion
  @(posedge uut.EOC );
  if (uut.EOC && digital_out == 512) begin
    $display("Test SUCCESS: Output = %d and EOC = %b", digital_out,EOC);
  end else begin
    $display("Test FAILURE: Output = %d, Expected = 512", digital_out);
  end
            rst = 1;
  $finish; // End of testing
end
endmodule
```

Constraint Setup and Synthesis

- ## Constraint Setup:
  - **Clock Setup**: A 1 ns clock period was specified, suggesting an operating frequency of 1 GHz. This is a critical parameter as it determines the timing constraints for the entire design.
  - **Input and Output Delays**: Delays of 0.3 ns are set for both inputs and outputs relative to the clock, which is crucial for ensuring data integrity and timing reliability.
  - **Clock Uncertainty**: Set at 50 ps to account for variations due to jitter and other factors, which is important for safe timing margins.
  - **Clock Latency**: A latency of 0.12 ns is specified, which covers the combined delays through the clock generation and distribution networks.

CONSTRAINS SCRIPT

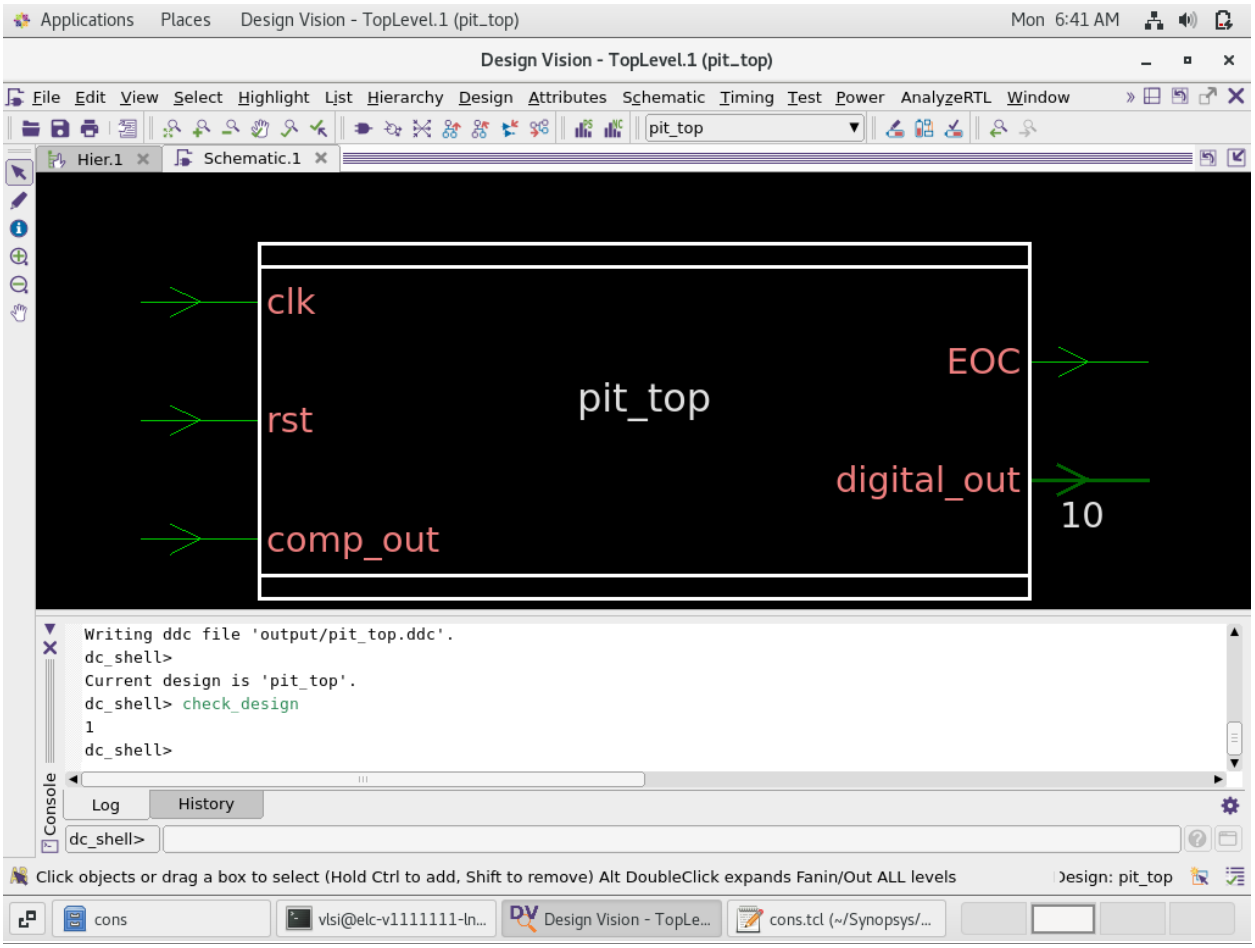
```
reset_design

create_clock -name clk -period 1 [get_ports clk]

set_input_delay -max 0.3 -clock [get_clocks clk] [remove_from_collection [all_inputs] [get_ports clk]]

set_output_delay -max 0.3 -clock [get_clocks clk] [all_outputs]

set_clock_uncertainty 0.05 [get_clocks]

#set_clock_latency -source 0.02  [get_clocks clk]

set_clock_latency  0.12 [get_clocks clk]

set_false_path -hold -from [remove_from_collection [all_inputs] [get_ports clk]]

set_false_path -hold -to [all_outputs]

set_min_library  saed90nm_max_lth.db -min_version saed90nm_min_nt.db

set_wire_load_model -name "8000" -library saed90nm_max_lth

set_wire_load_mode enclosed

set_load -max [expr {2 * [load_of saed90nm_max_lth/NBUFFX8/INP]}] [all_outputs]

set_driving_cell -no_design_rule -max -lib_cell TNBUFFX1 [remove_from_collection [all_inputs] [get_ports clk]]

group_path -name INPUTS -from [remove_from_collection [all_inputs] [get_ports clk]]

group_path -name OUTPUTS -to [all_outputs]

group_path -name COMB -from [all_inputs] -to [all_outputs]
```

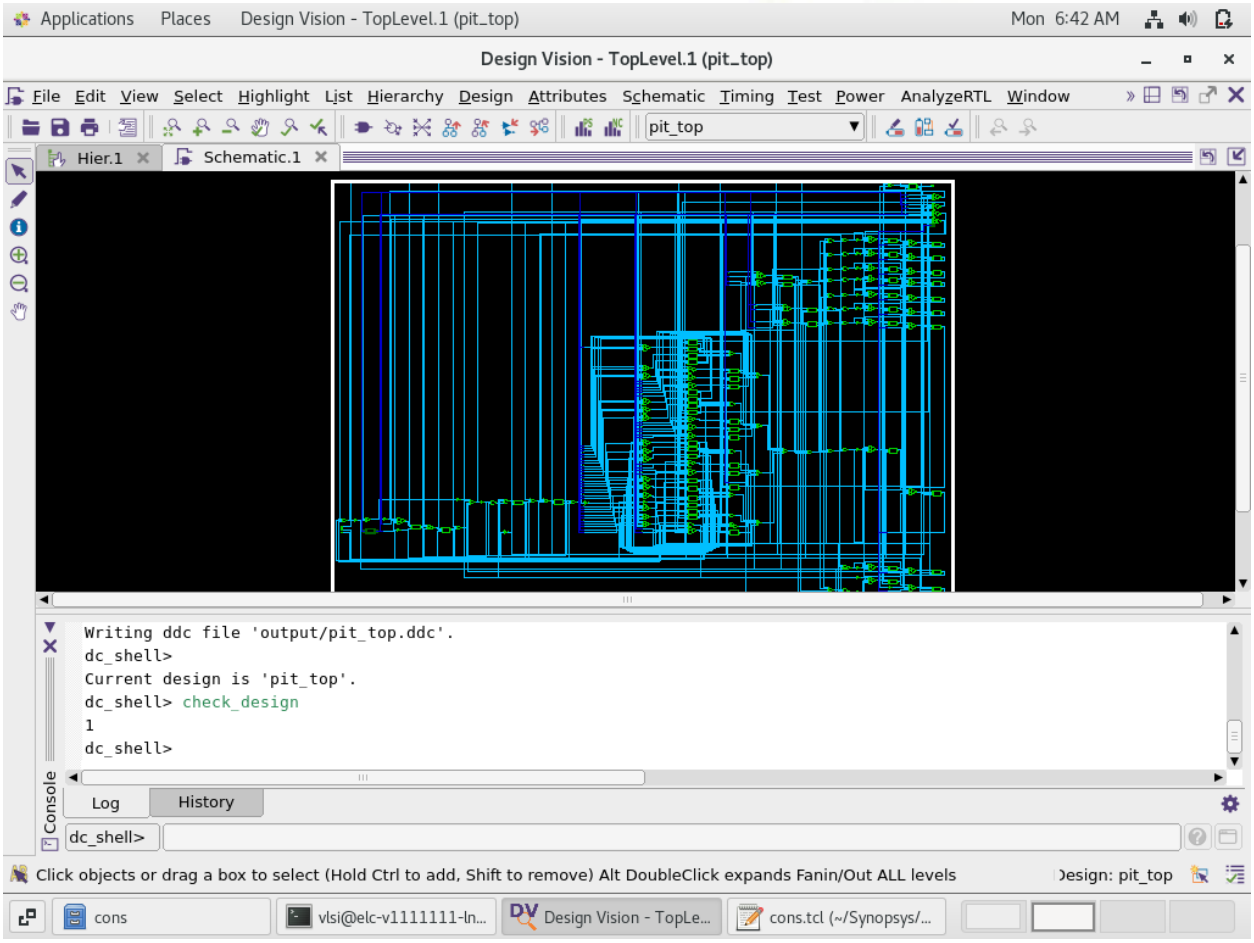
SYNTHESIS SCRIPT

```
set design pit_top

#set_app_var search_path /home/vlsi/Desktop/Syn_tools/SAED90nm_EDK_10072017/SAED90_EDK/SAED_EDK90nm/Digital_Standard_cell_Library/synopsys/models

set_app_var search_path /eda/synopsys/SAED90nm_EDK_10072017/SAED90_EDK/SAED_EDK90nm/Digital_Standard_cell_Library/synopsys/models

#set_app_var target_library "NangateOpenCellLibrary_ss0p95vn40c.db NangateOpenCellLibrary_ff1p25v0c.db NangateOpenCellLibrary_ss0p95v125c.db NangateOpenCellLibrary_tt1p1v25c.db"

set_app_var target_library "saed90nm_max_lth.db"

set_app_var link_library "* $target_library"

sh rm -rf work

sh mkdir -p work

define_design_lib work -path ./work

analyze -library work -format verilog ../rtl/${design}.v

elaborate $design -lib work

current_design

# the rest of the flow will be next lab isa

check_design -summary

source  -echo -verbose ./cons/cons.tcl

link

set_fix_multiple_port_nets -all

compile -map_effort medium

report_area > ./report/synth_area.rpt

report_cell > ./report/synth_cells.rpt

report_qor  > ./report/synth_qor.rpt

report_resources > ./report/synth_resources.rpt
```

```
report_timing -max_paths 10 > ./report/synth_timing.rpt


write_sdc  output/${design}.sdc


define_name_rules  no_case -case_insensitive

change_names -rule no_case -hierarchy

change_names -rule verilog -hierarchy

set verilogout_no_tri              true

set verilogout_equation  false


write -hierarchy -format verilog -output output/${design}.v

write -f ddc -hierarchy -output output/${design}.ddc


#exit

#start_gui
```

SYNTHESIS OUTPUT




Applications
Places
Design Vision - TopLevel.1 (pit_top)
Mon 6:42 AM
Design Vision - TopLevel.1 (pit_top)
File Edit View Select Highlight List Hierarchy Design Attributes Schematic Timing Test Power AnalyzeRTL Window
pit_top
Hier.1
Schematic.1
Writing ddc file 'output/pit_top.ddc'.
dc_shell>
Current design is 'pit_top'.
dc_shell> check_design
1
dc_shell>
Console
Log
History
dc_shell>
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove) Alt DoubleClick expands Fanin/Out ALL levels
Design: pit_top
cons
vlsi@elc-v1111111-ln...
Design Vision - TopLe...
cons.tcl (~/Synopsys/...

SYNTHESIS QUALITY OF RESOURCES

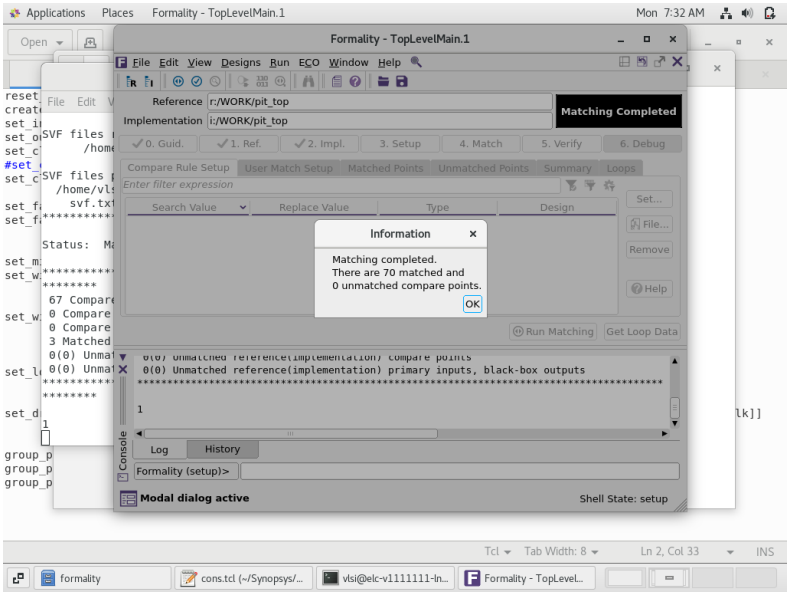
```
****************************************
Report : qor
Design : pit_top
Version: V-2023.12
Date   : Mon May  6 07:08:53 2024
****************************************


  Timing Path Group 'INPUTS'
  -----------------------------------
  Levels of Logic:                7.00
  Critical Path Length:           0.38
  Critical Path Slack:            0.21
  Critical Path Clk Period:       1.00
  Total Negative Slack:           0.00
  No. of Violating Paths:         0.00
  Worst Hold Violation:           0.00
  Total Hold Violation:           0.00
  No. of Hold Violations:         0.00
  -----------------------------------

  Timing Path Group 'OUTPUTS'
  -----------------------------------
  Levels of Logic:                0.00
  Critical Path Length:           0.16
  Critical Path Slack:            0.49
  Critical Path Clk Period:       1.00
  Total Negative Slack:           0.00
  No. of Violating Paths:         0.00
  Worst Hold Violation:           0.00
  Total Hold Violation:           0.00
  No. of Hold Violations:         0.00
  -----------------------------------
```

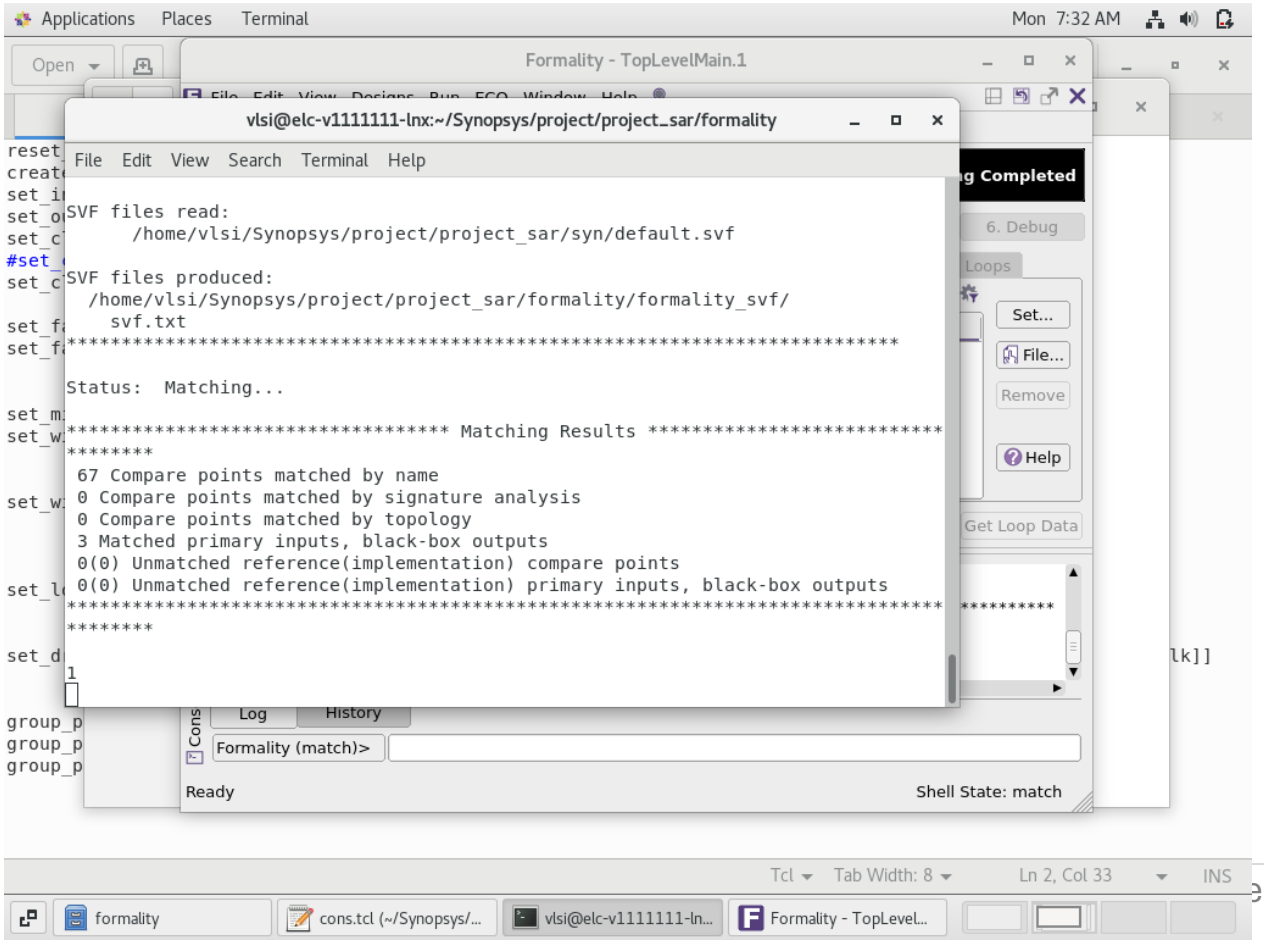
```
  Timing Path Group 'clk'
  -----------------------------------
  Levels of Logic:               16.00
  Critical Path Length:           0.82
  Critical Path Slack:            0.06
  Critical Path Clk Period:       1.00
  Total Negative Slack:           0.00
  No. of Violating Paths:         0.00
  Worst Hold Violation:           0.00
  Total Hold Violation:           0.00
  No. of Hold Violations:         0.00
  -----------------------------------


  Cell Count
  -----------------------------------
  Hierarchical Cell Count:           1
  Hierarchical Port Count:          64
  Leaf Cell Count:                 302
  Buf/Inv Cell Count:               44
  Buf Cell Count:                    0
  Inv Cell Count:                   44
  CT Buf/Inv Cell Count:             0
  Combinational Cell Count:        246
  Sequential Cell Count:            56
  Macro Count:                       0
  -----------------------------------


  Area
  -----------------------------------
  Combinational Area:      1865.318403
  Noncombinational Area:   1804.492828
  Buf/Inv Area:             243.302406
  Total Buffer Area:              0.00
  Total Inverter Area:          243.30
  Macro/Black Box Area:       0.000000
  Net Area:                 190.227459
  -----------------------------------
  Cell Area:               3669.811232
  Design Area:             3860.038691
```

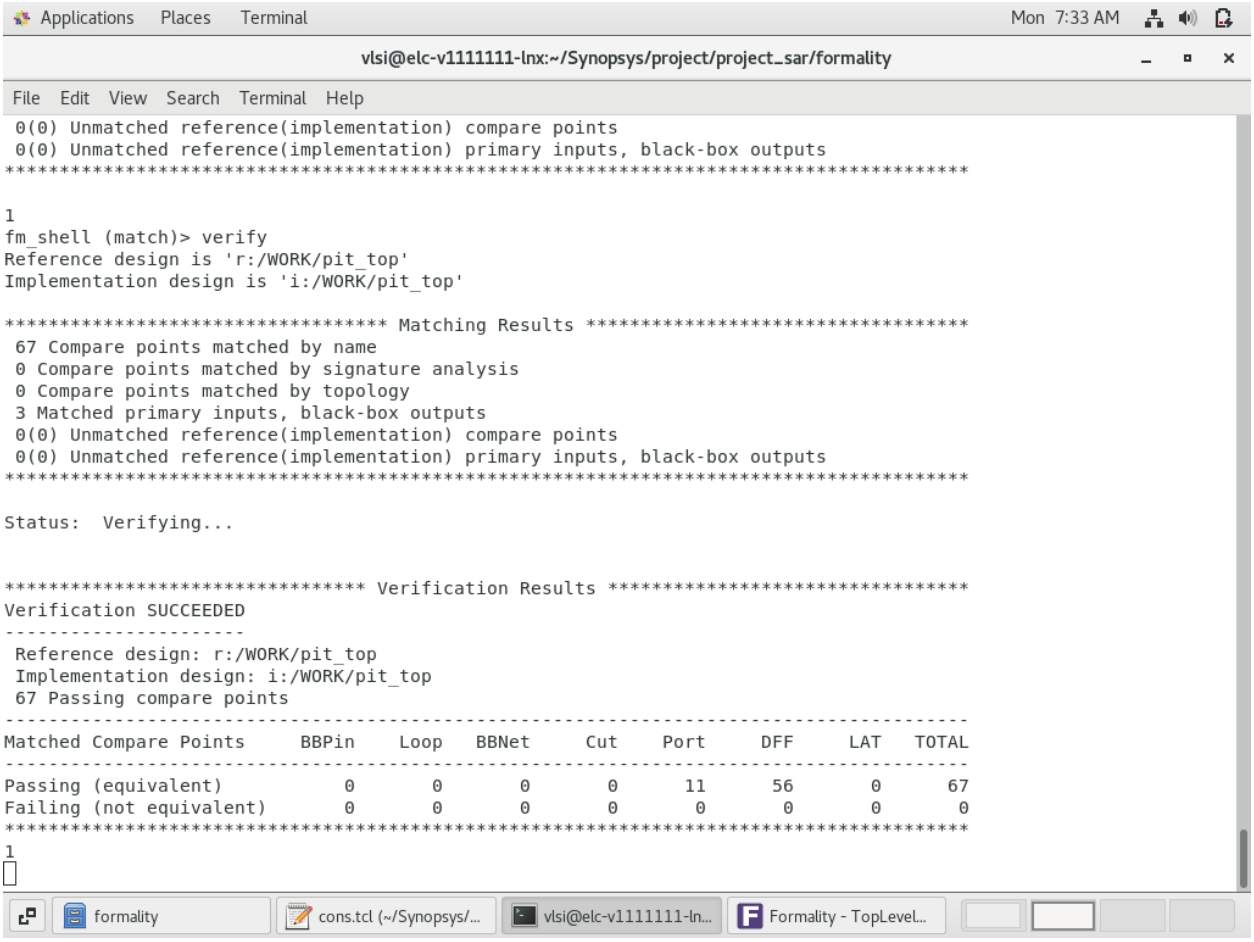
```
  Design Rules
  ----------------------------------
  Total Number of Nets:           336
  Nets With Violations:             0
  Max Trans Violations:             0
  Max Cap Violations:               0
  ----------------------------------


  Hostname: elc-v1111111-lnx

  Compile CPU Statistics
  ----------------------------------------
  Resource Sharing:                  4.98
  Logic Optimization:               10.01
  Mapping Optimization:              6.01
  ----------------------------------------
  Overall Compile Time:             31.62
  Overall Compile Wall Clock Time:  53.33

  --------------------------------------------------------------------

  Design  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0


  Design (Hold)  WNS: 0.00  TNS: 0.00  Number of Violating Paths: 0

  --------------------------------------------------------------------


1
```

Name	Date modified	Type	Size
synth_area	5/6/2024 4:08 AM	RPT File	2 KB
synth_cells	5/6/2024 4:08 AM	RPT File	23 KB
synth_qor	5/6/2024 4:08 AM	RPT File	4 KB
synth_qor_1ns	5/6/2024 3:54 AM	RPT File	4 KB
synth_resources	5/6/2024 4:08 AM	RPT File	2 KB
synth_timing	5/6/2024 4:08 AM	RPT File	59 KB

FORMAL VERIFICATION

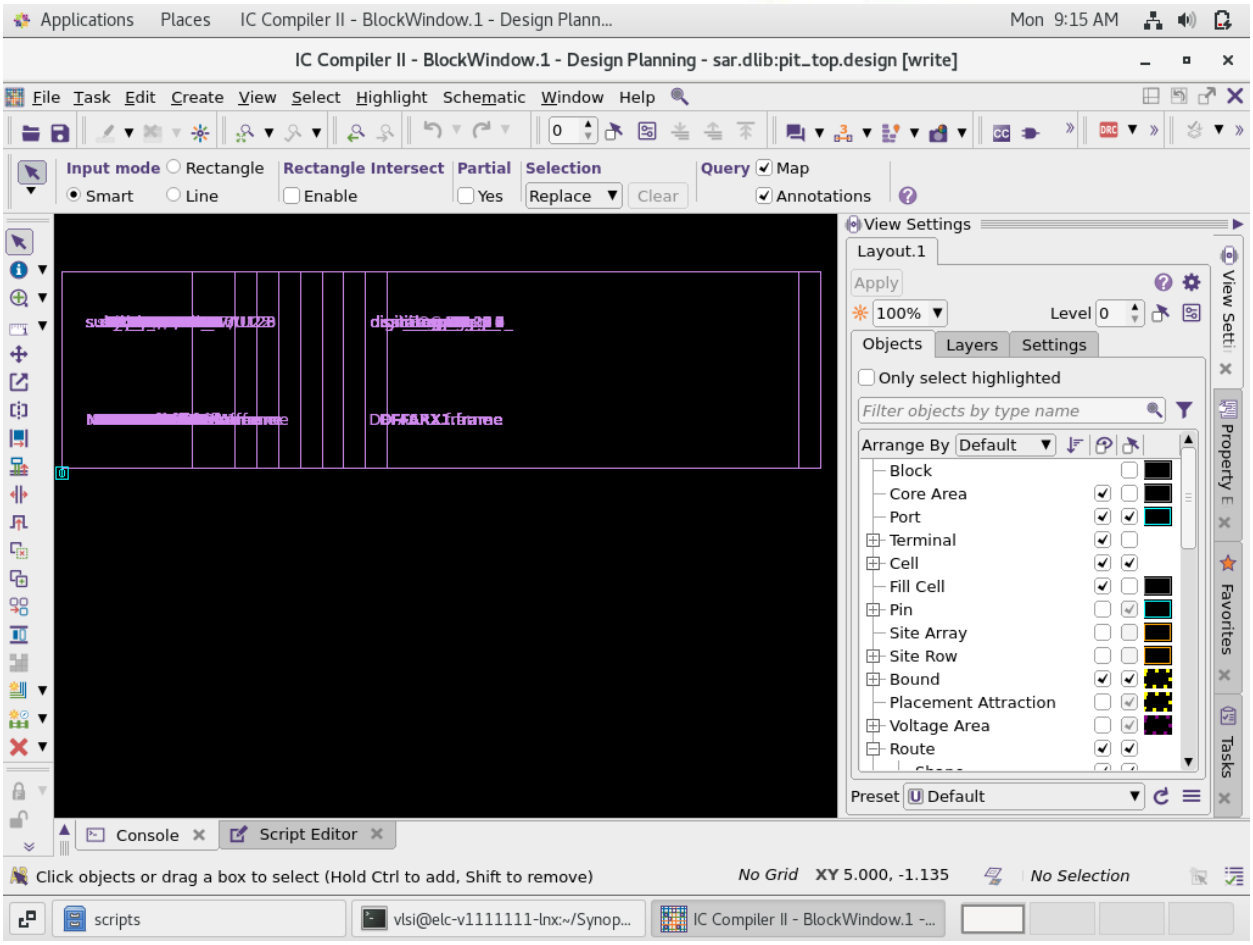





Applications Places Terminal
Mon 7:33 AM
vlsi@elc-v1111111-lnx:~/Synopsys/project/project_sar/formality
File Edit View Search Terminal Help
0(0) Unmatched reference(implementation) compare points
0(0) Unmatched reference(implementation) primary inputs, black-box outputs
1
fm_shell (match)> verify
Reference design is 'r:/WORK/pit_top'
Implementation design is 'i:/WORK/pit_top'
Matching Results
67 Compare points matched by name
0 Compare points matched by signature analysis
0 Compare points matched by topology
3 Matched primary inputs, black-box outputs
0(0) Unmatched reference(implementation) compare points
0(0) Unmatched reference(implementation) primary inputs, black-box outputs
Status: Verifying...
Verification Results
Verification SUCCEEDED
Reference design: r:/WORK/pit_top
Implementation design: i:/WORK/pit_top
67 Passing compare points
Matched Compare Points BBPin Loop BBNet Cut Port DFF LAT TOTAL
Passing (equivalent) 0 0 0 0 11 56 0 67
Failing (not equivalent) 0 0 0 0 0 0 0 0
1
formality
cons.tcl (~/Synopsys/...
vlsi@elc-v1111111-ln...
Formality - TopLevel...

Data Setup

```
# put the search path directory of the technology

#set_app_var search_path
/eda/synopsys/SAED90nm_EDK_10072017/SAED90_EDK/SAED_EDK90nm/Digital_Standard_cell_Library/process/astro/tech

set_app_var search_path /eda/synopsys/SAED90nm_EDK_10072017/SAED90_EDK/SAED_EDK90nm

set TECH_FILE $search_path/Digital_Standard_cell_Library/process/astro/tech/astroTechFile.tf

# put the directory of your ndm created from the library manager

set reference_library /home/vlsi/Synopsys/project/project_sar/ndm/saed90nm_max_lth.ndm

#create design library from technology file & ndm

create_lib -technology $TECH_FILE -ref_libs $reference_library sar.dlib

#read gate level netlist output from synthesis

read_verilog -top pit_top /home/vlsi/Synopsys/project/project_sar/syn/output/pit_top.v

link_block

set Tech $search_path/Technology_Kit/starrcxt

read_parasitic_tech -layermap $Tech/tech2itf.map -tlup $Tech/tluplus/saed90nm_1p9m_1t_Cmax.tluplus  -name maxTLU

read_parasitic_tech -layermap $Tech/tech2itf.map -tlup $Tech/tluplus/saed90nm_1p9m_1t_Cmin.tluplus  -name minTLU

#put the sdc file output from synthesis

read_sdc /home/vlsi/Synopsys/project/project_sar/syn/output/pit_top.sdc

get_site_defs

set_attribute [get_site_defs unit] symmetry y

set_attribute [get_layers {M1 M3 M5 M7 M9} ] routing_direction horizontal

set_attribute [get_layers {M2 M4 M6 M8 } ] routing_direction vertical

get_attribute [get_layers M7] routing_direction

report_ignored_layers

set_ignored_layers -max_routing_layer M8

report_ignored_layers

save_block
```


Applications
Places
IC Compiler II - BlockWindow.1 - Design Plann...
Mon 9:15 AM
IC Compiler II - BlockWindow.1 - Design Planning - sar.dlib:pit_top.design [write]
File Task Edit Create View Select Highlight Schematic Window Help
Input mode
Smart
Rectangle
Line
Rectangle Intersect
Enable
Partial
Yes
Selection
Replace
Clear
Query
Map
Annotations
View Settings
Layout.1
Apply
100%
Level
Objects
Layers
Settings
Only select highlighted
Filter objects by type name
Arrange By
Default
Block
Core Area
Port
Terminal
Cell
Fill Cell
Pin
Site Array
Site Row
Bound
Placement Attraction
Voltage Area
Route
Preset
Default
View Setti
Property E
Favorites
Tasks
Console
Script Editor
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
No Grid
XY 5.000, -1.135
No Selection
scripts
vlsi@elc-v1111111-lnx:~/Synop...
IC Compiler II - BlockWindow.1 -...

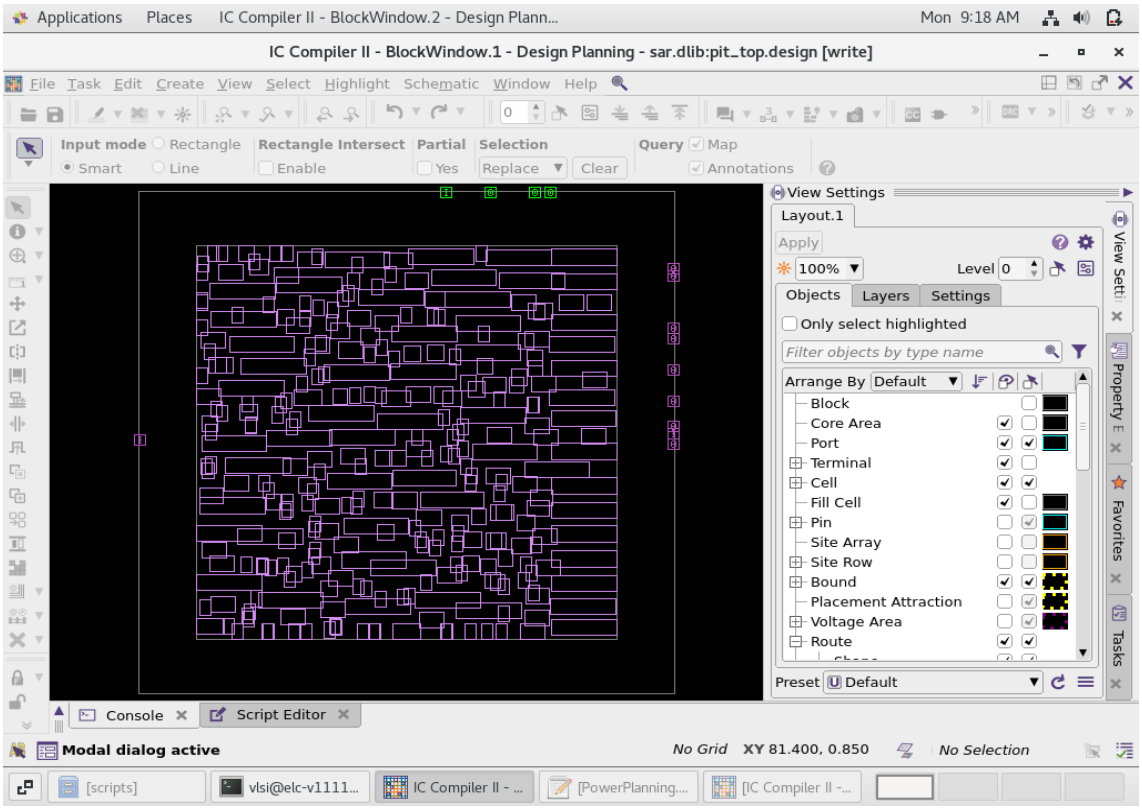
FLOOR AND POWER PLANNING

SCRIPT

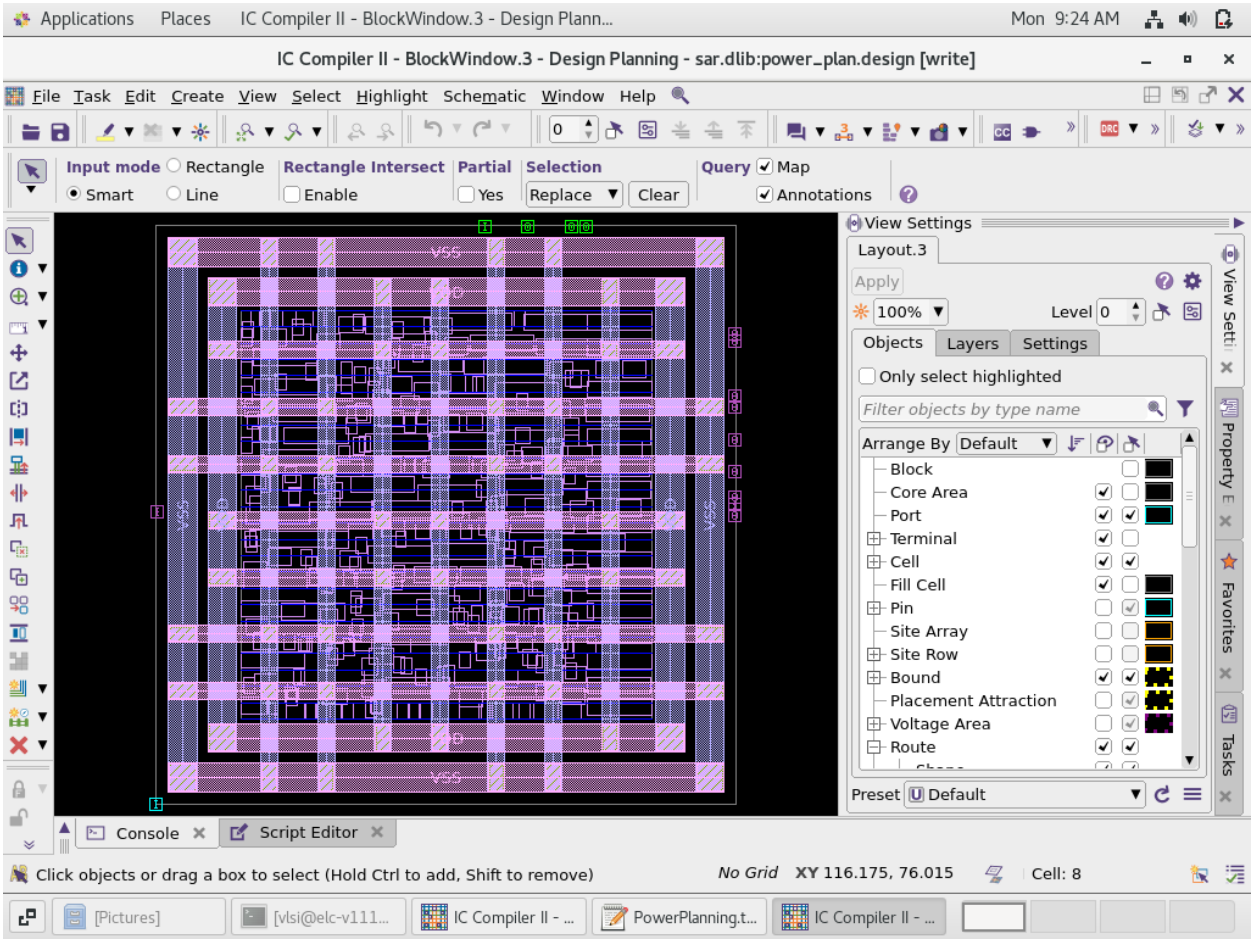
```
initialize_floorplan -side_ratio {1 1} -core_offset {15}

create_placement -floorplan

set_block_pin_constraint -self -allowed_layers {M3 M4 M5 M6}

place_pins -self

copy_block -from_block sar.dlib:pit_top.design -to_block power_plan

current_block power_plan.design

report_ignored_layers

remove_ignored_layers -all -max_routing_layer -min_routing_layer

report_ignored_layers

set_app_option -name plan.pgroute.auto_connect_pg_net -value true

create_net -power VDD

create_net -ground VSS

#PG RING CREATION

create_pg_ring_pattern ring_pattern -horizontal_layer M9    -horizontal_width {5} -horizontal_spacing {2}    -vertical_layer M8 -
vertical_width {5}    -vertical_spacing {2}

set_pg_strategy core_ring -core -pattern \

  {{pattern: ring_pattern}{nets: {VDD VSS}}{offset: {0.8 0.8}}} \

  -extension {{stop: innermost_ring}}

compile_pg -strategies core_ring connect_pg_net -net VDD [get_pins -hierarchical "*/VDD"]

connect_pg_net -net VSS [get_pins -hierarchical "*/VSS"]
```

```
# PG MESH CREATION

create_pg_mesh_pattern pg_mesh1    -parameters {w1 p1 w2 p2 f t}    -layers {{{vertical_layer: M8} {width: @w1} {spacing:
interleaving}       {pitch: @p1} {offset: @f} {trim: @t}}          {{horizontal_layer: M9 } {width: @w2} {spacing: interleaving}       {pitch:
@p2} {offset: @f} {trim: @t}}}

set_pg_strategy s_mesh1 \

  -pattern {{pattern: pg_mesh1} {nets: {VDD VSS VSS VDD}} \

{offset_start: 5 5} {parameters: 3 40 3 40 5 false}} \

  -core -extension {{stop: outermost_ring}}

compile_pg -strategies s_mesh1

#STANDARD CELL RAIL INSERTION

create_pg_std_cell_conn_pattern     std_cell_rail     -layers {M1}     -rail_width 0.06

set_pg_strategy rail_strat -core \

   -pattern {{name: std_cell_rail} {nets: VDD VSS} }

compile_pg -strategies rail_strat

save_block
```

LAYOUT VIEW OF FLOOR PLANNING



LAYOUT VIEW OF POWER PLANNING

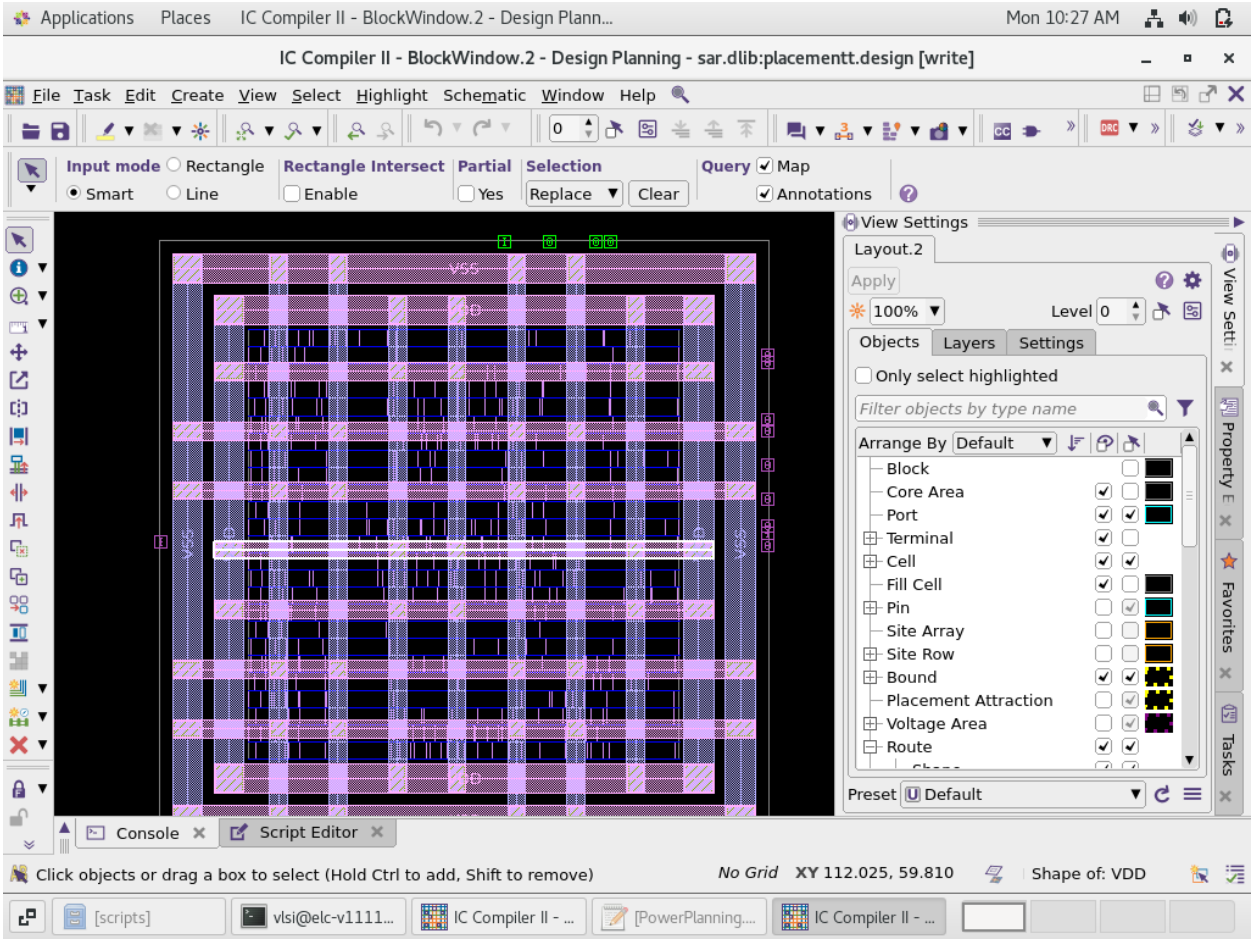


Placement

PLACEMENT SCRIPT

```
copy_block -from_block sar.dlib:power_plan.design -to_block placementt

current_block placementt.design

report_qor -summary

report_design -summary

report_utilization

check_design -checks pre_placement_stage

report_lib saed90nm_max_lth

set_voltage 1.08

set_parasitic_parameters -early_spec maxTLU -late_spec minTLU

# Run 5 stages of placement : .coarse placement  .initial_drc-HFS .running initial optimization .final_place

#  . final_optomization

place_opt

#View congestion map

#report_congestion -rerun_global_router

# check legalizaation of all cells [no overlapping cells ....]

check_legality -verbose

report_utilization

report_qor

save_block
```

LAYOUT VIEW OF PLACEMENT



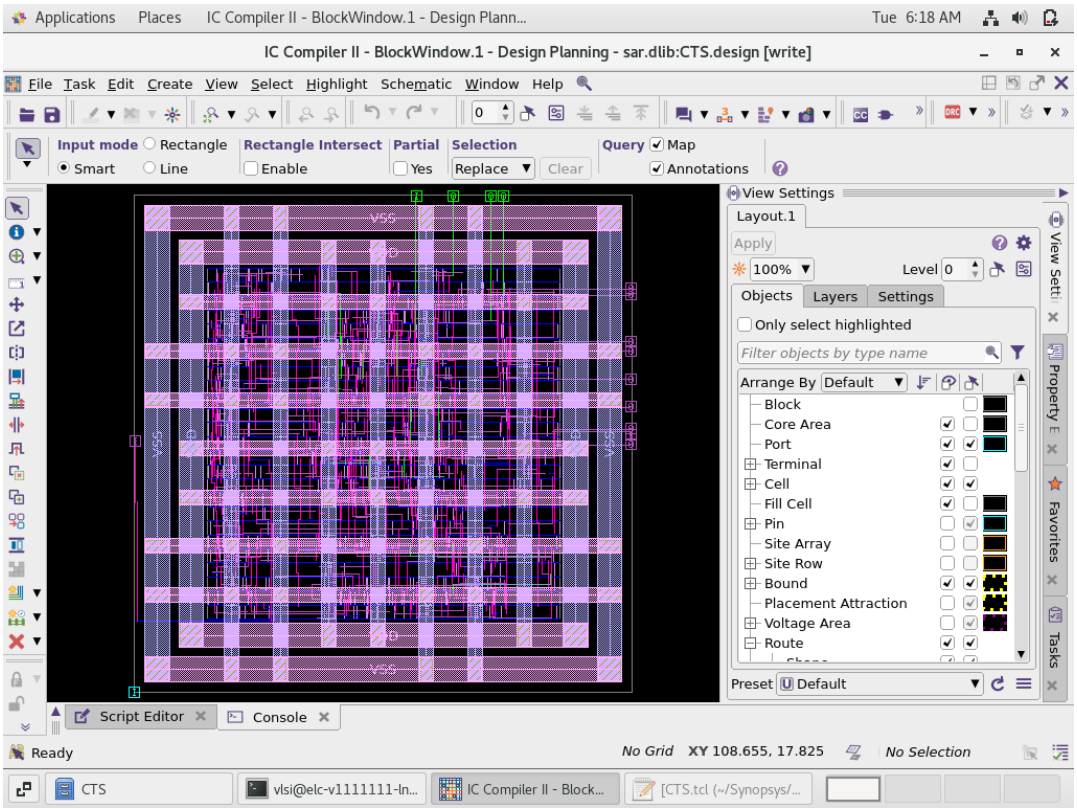
Clock tree synthesis (CTS)

CTS SCRIPT

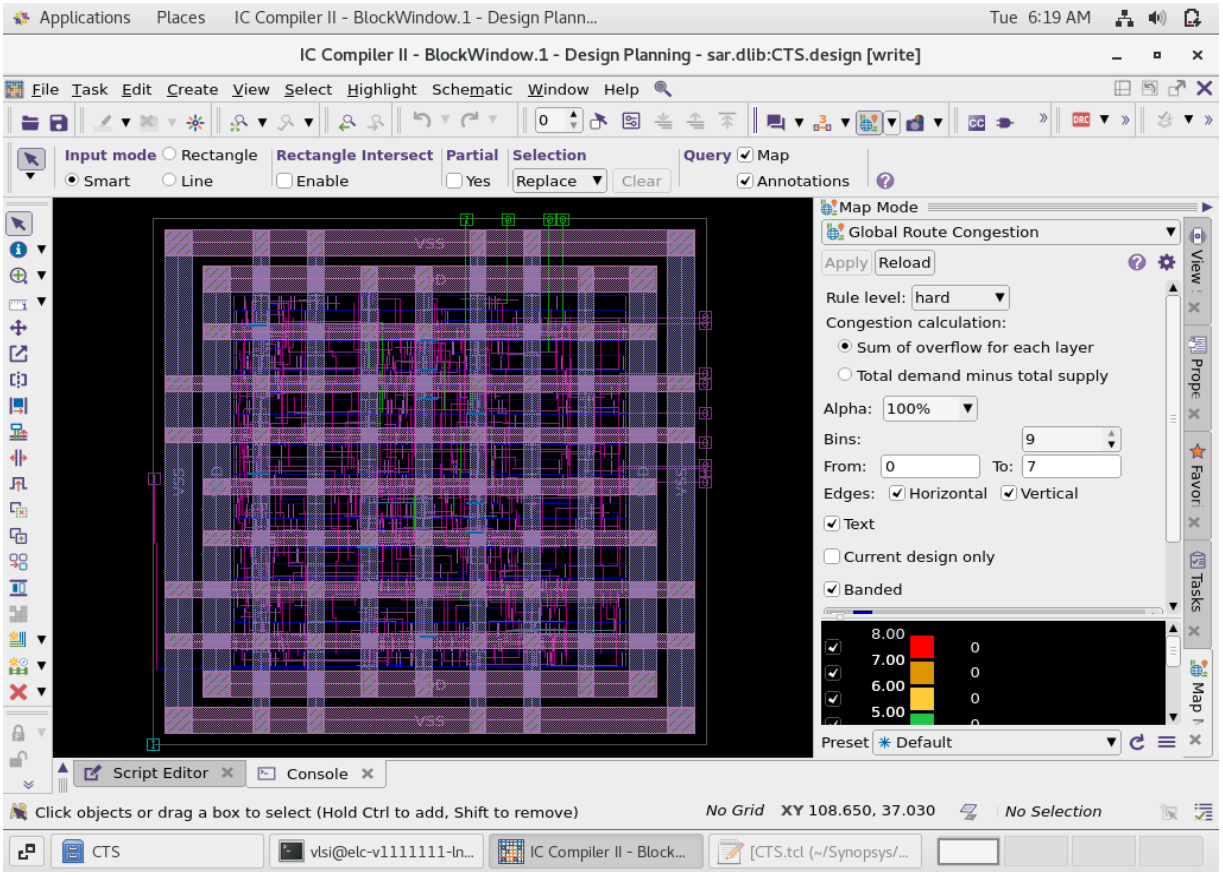
```
report_clock_qor -type structure

derive_clock_cell_references -output cts_leg_set.tcl > /dev/null

set CTS_CELLS [get_lib_cells "*/NBUFFX2 */NBUFFX4 */NBUFFX8 "]

set CTS_NDR_MIN_ROUTING_LAYER "M4"

set CTS_NDR_MAX_ROUTING_LAYER "M5"

set CTS_LEAF_NDR_MIN_ROUTING_LAYER "M1"

set CTS_LEAF_NDR_MAX_ROUTING_LAYER "M5"

set CTS_NDR_RULE_NAME "cts_w2_s2_vlg"

#set CTS_LEAF_NDR_RULE_NAME            "cts_w1_s2"

create_routing_rule $CTS_NDR_RULE_NAME\

                        -default_reference_rule \

                        -taper_distance 0.4 \

                        -driver_taper_distance 0.4 \

                        -widths  {M3 0.16 M4 0.32 M5 0.32} \

                        -spacings {M3 0.16 M4 0.32 M5 0.32}

set_clock_routing_rules -rules $CTS_NDR_RULE_NAME \

-min_routing_layer $CTS_NDR_MIN_ROUTING_LAYER \

-max_routing_layer $CTS_NDR_MAX_ROUTING_LAYER

report_routing_rules -verbose

report_clock_routing_rules

#Sink pins will not follows NDRs

set_clock_routing_rules -net_type sink -default_rule -min_routing_layer M1 -max_routing_layer M2
```

```
#DRC

report_ports -verbose [get_ports *clk*]

set_driving_cell -scenarios [all_scenarios] -lib_cell NBUFFX4 [get_ports *clk*]

set_app_options -name time.remove_clock_reconvergence_pessimism -value true

report_clock_settings

set_clock_tree_options -target_skew 0.5 -clock [get_clocks *]

set_clock_tree_options -target_latency 0.1  -clock [get_clocks *]

clock_opt

save_block
```

CTS LAYOUT VIEW



GLOBAL ROUTE CONGESTION MAP



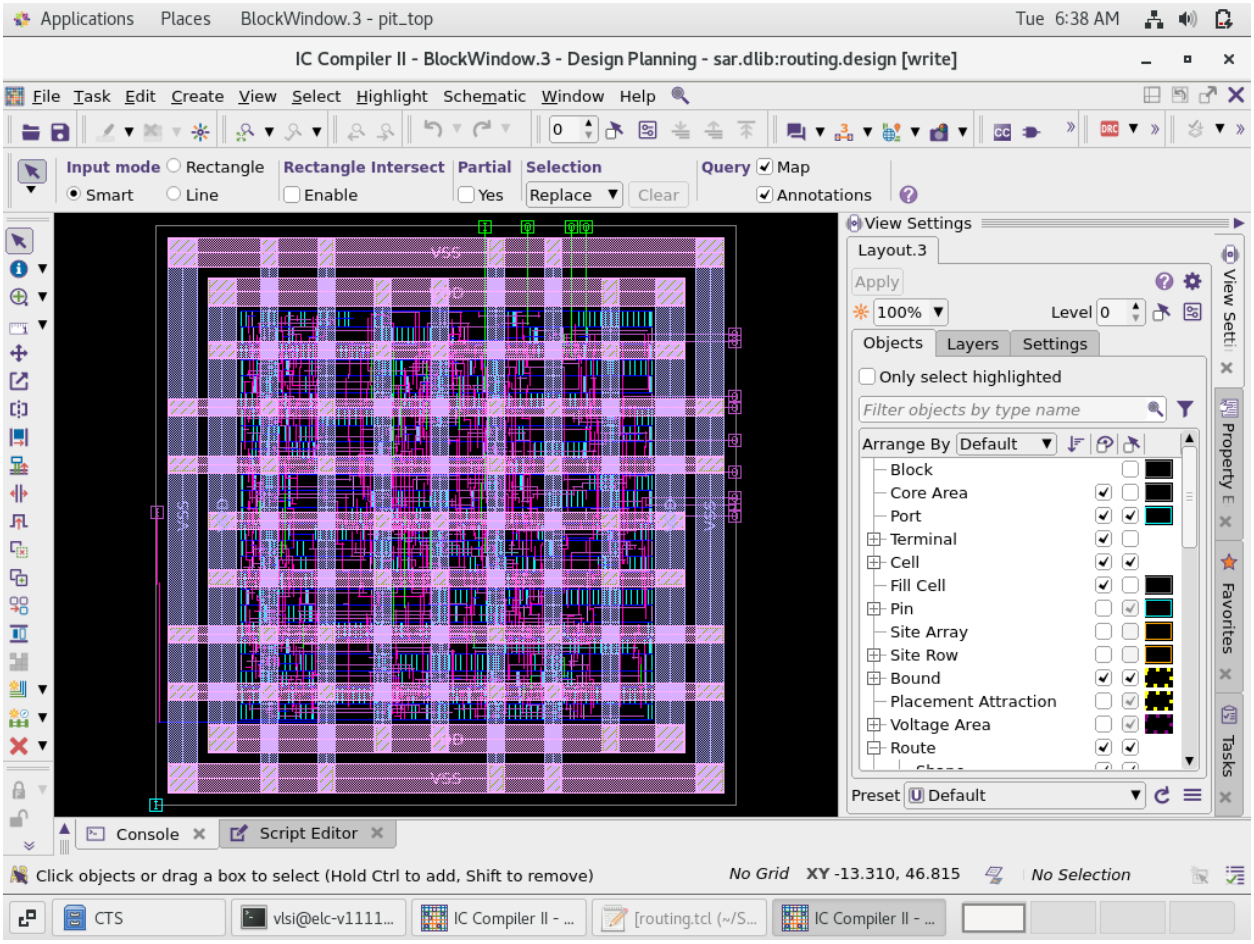
ROUTING

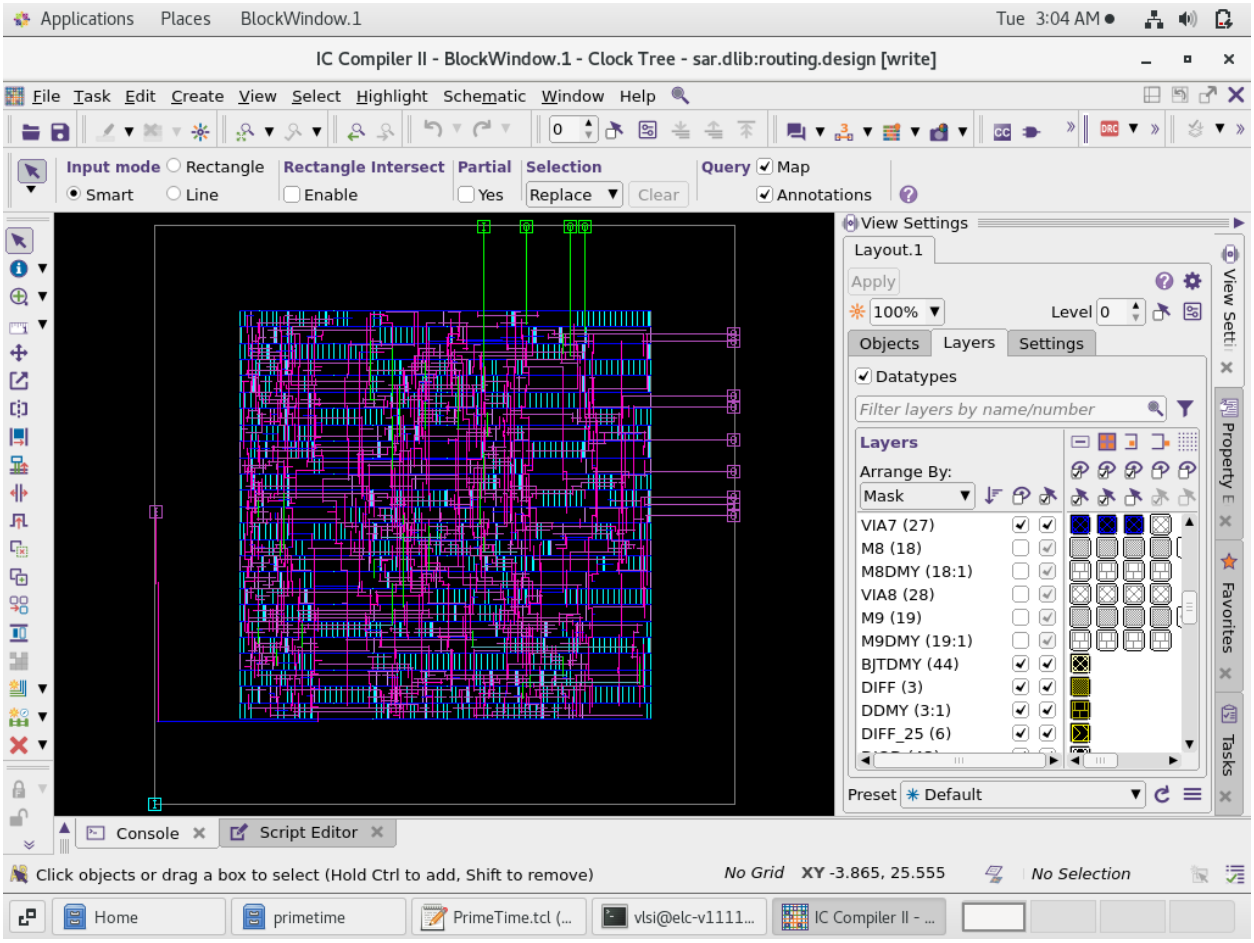
ROUTING SCRIPT

```
copy_block -from_block sar.dlib:CTS.design -to_block routing

current_block routing.design

report_qor -summary

check_design -checks pre_route_stage

source
/eda/synopsys/SAED90nm_EDK_10072017/SAED90_EDK/SAED_EDK90nm/Digital_Standard_cell_Library/process/astro/tech/saed
90nm_1p9m_antenna.tcl

route_auto

# Routing Optimization

route_opt

check_routes

# 2.Filler Cells Insertion

set FillerCells " SHFILL128 SHFILL64 SHFILL3 SHFILL2 SHFILL1 "

create_stdcell_fillers -lib_cells $FillerCells

connect_pg_net -automatic

remove_stdcell_fillers_with_violation

check_legality

# 3.Checks & Output

set DESIGN_NAME pit_top

# Netlist after physical synthesis

##write_verilog  ./output/${DESIGN_NAME}.v

write_verilog  /home/vlsi/Synopsys/project/project_sar/pnr/output/${DESIGN_NAME}.v

#SDC_OUT

#write_sdc -output ./output/${DESIGN_NAME}.out.sdc

write_sdc -output /home/vlsi/Synopsys/project/project_sar/pnr/output/${DESIGN_NAME}.out.sdc
```

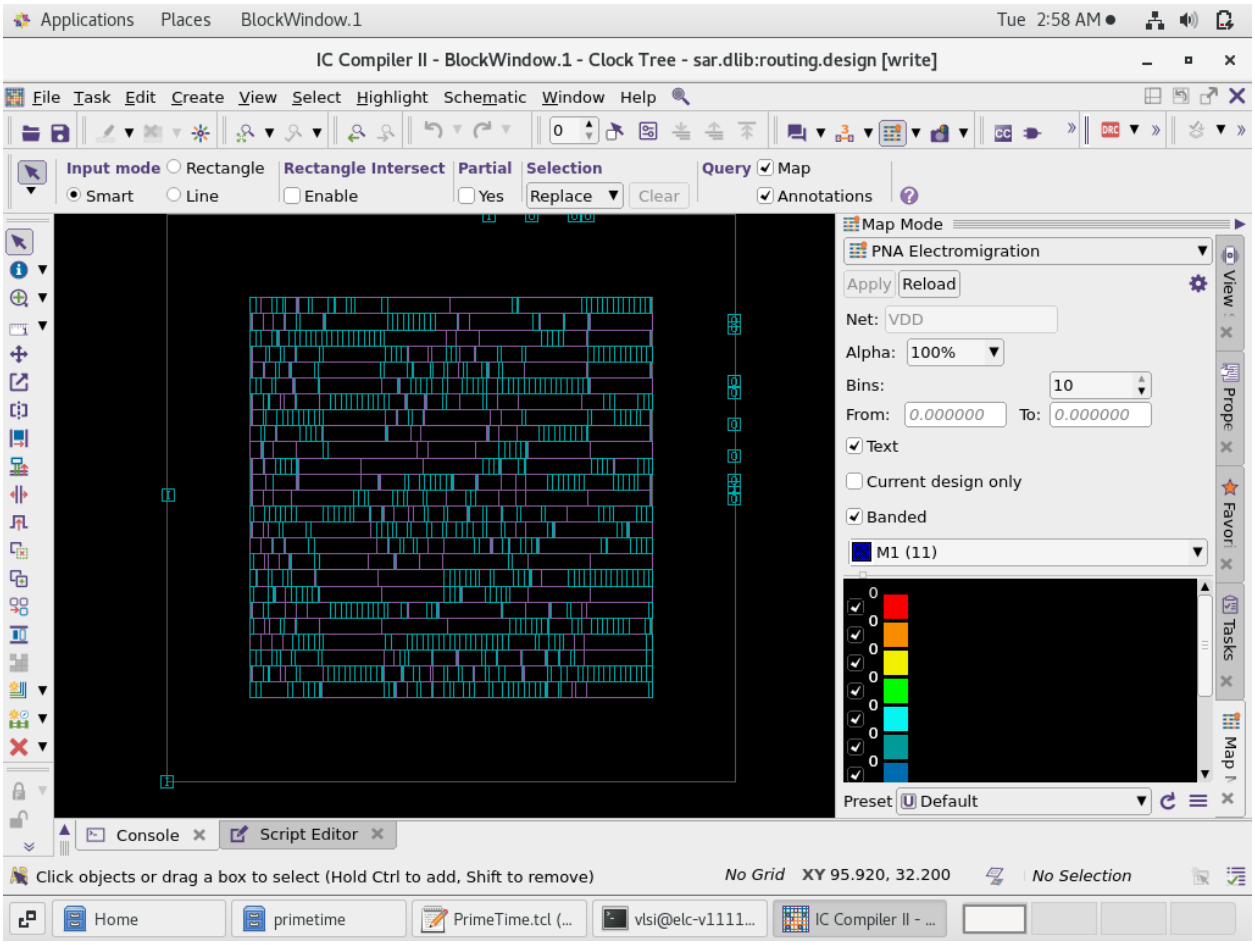
```
# SPEF_OUT

#write_parasitics -format SPEF -output ./output/${DESIGN_NAME}.out.spef

write_parasitics -format SPEF -output /home/vlsi/Synopsys/project/project_sar/pnr/output/${DESIGN_NAME}.out.spef

######DEF_OUT

#write_def ./output/${DESIGN_NAME}.out.def

write_def /home/vlsi/Synopsys/project/project_sar/pnr/output/${DESIGN_NAME}.out.def



##########GDS_OUT



set GDS_MAP_FILE
/eda/synopsys/SAED90nm_EDK_10072017/SAED90_EDK/SAED_EDK90nm/Technology_Kit/milkyway/saed90nm.gdsout.map



set STD_CELL_GDS
/eda/synopsys/SAED90nm_EDK_10072017/SAED90_EDK/SAED_EDK90nm/Digital_Standard_cell_Library/layout/gds/saed90nm.gds



write_gds \

-view design \

-lib_cell_view frame \

-output_pin all \

-fill include \

-exclude_empty_block \

-long_names \

-layer_map "$GDS_MAP_FILE" \

-keep_data_type \

-merge_files "$STD_CELL_GDS" \

/home/vlsi/Synopsys/project/project_sar/pnr/output/${DESIGN_NAME}.gds

save_block
```

ROUTING LAYOUT VIEW

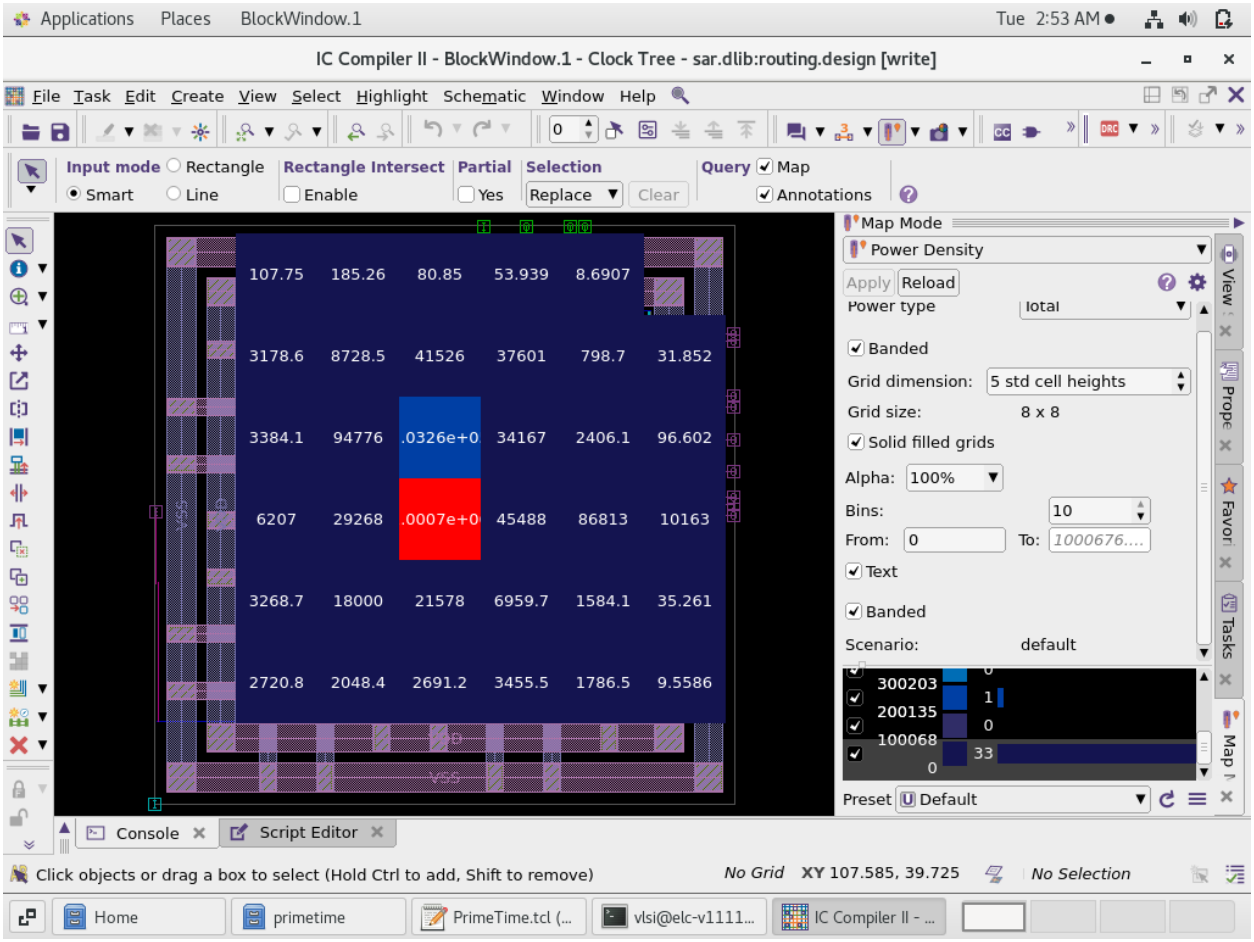



Applications
Places
BlockWindow.1
Tue 3:04 AM
IC Compiler II - BlockWindow.1 - Clock Tree - sar.dlib:routing.design [write]
File Task Edit Create View Select Highlight Schematic Window Help
Input mode
Rectangle
Smart
Line
Rectangle Intersect
Enable
Partial
Yes
Selection
Replace
Clear
Query
Map
Annotations
View Settings
Layout.1
Apply
100%
Level
Objects
Layers
Settings
Datatypes
Filter layers by name/number
Layers
Arrange By:
Mask
VIA7 (27)
M8 (18)
M8DMY (18:1)
VIA8 (28)
M9 (19)
M9DMY (19:1)
BJTDMY (44)
DIFF (3)
DDMY (3:1)
DIFF_25 (6)
Preset
Default
View Setti
Property E
Favorites
Tasks
Console
Script Editor
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
No Grid
XY -3.865, 25.555
No Selection
Home
primetime
PrimeTime.tcl (...
vlsi@elc-v1111...
IC Compiler II - ...

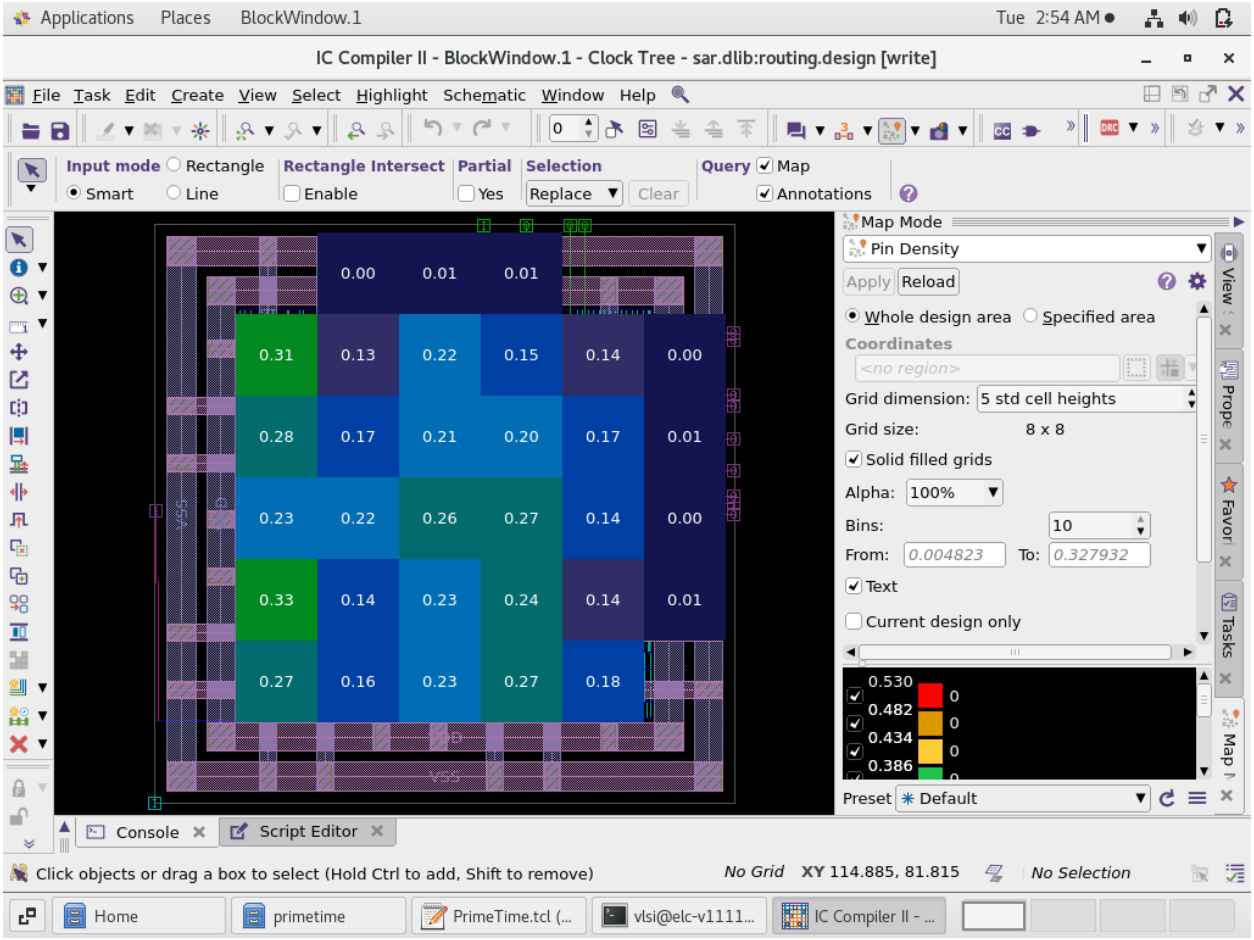
FILLER CELLS



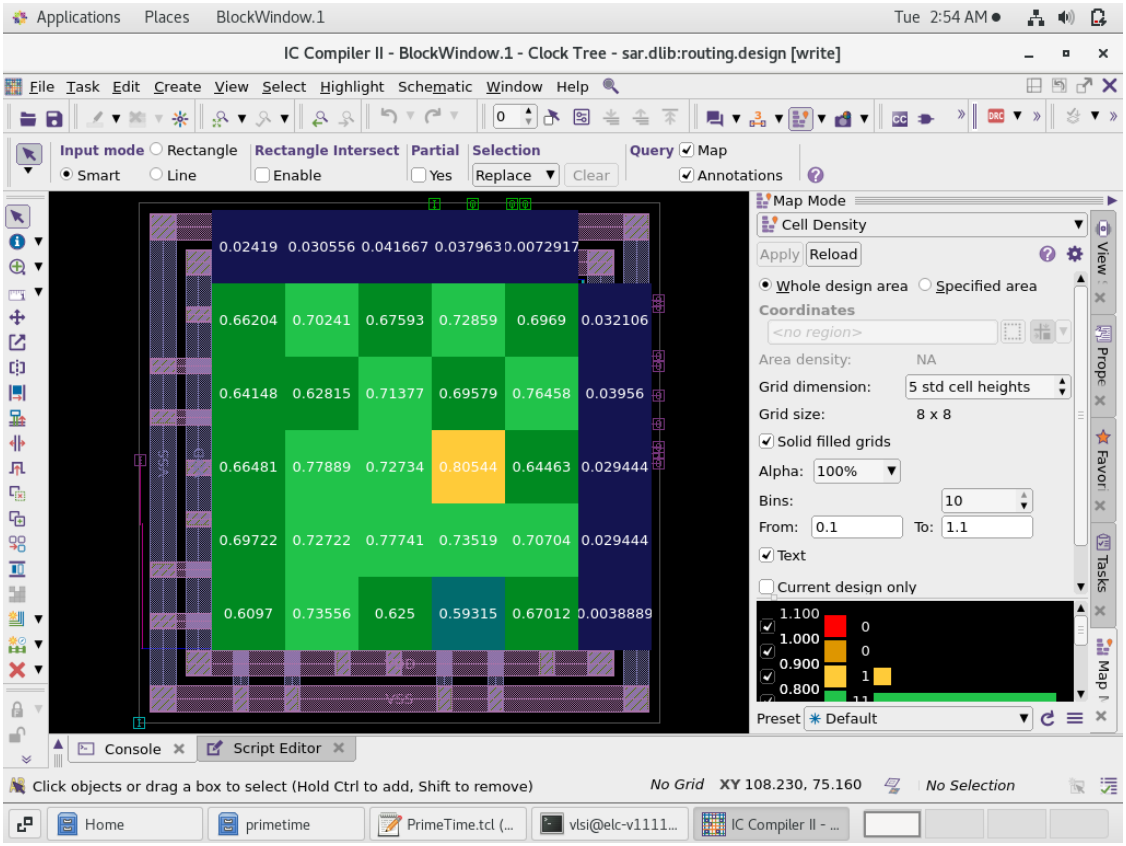
POWER DENSITY



PIN DENSITY


Applications Places BlockWindow.1 Tue 2:54 AM
IC Compiler II - BlockWindow.1 - Clock Tree - sar.dlib:routing.design [write]
File Task Edit Create View Select Highlight Schematic Window Help
Input mode Rectangle Smart Line
Rectangle Intersect Enable
Partial Yes
Selection Replace Clear
Query Map Annotations
0.00 0.01 0.01
0.31 0.13 0.22 0.15 0.14 0.00
0.28 0.17 0.21 0.20 0.17 0.01
0.23 0.22 0.26 0.27 0.14 0.00
0.33 0.14 0.23 0.24 0.14 0.01
0.27 0.16 0.23 0.27 0.18
Map Mode
Pin Density
Apply Reload
Whole design area Specified area
Coordinates
<no region>
Grid dimension: 5 std cell heights
Grid size: 8 x 8
Solid filled grids
Alpha: 100%
Bins: 10
From: 0.004823 To: 0.327932
Text
Current design only
0.530 0
0.482 0
0.434 0
0.386
Preset Default
Console Script Editor
Click objects or drag a box to select (Hold Ctrl to add, Shift to remove)
No Grid XY 114.885, 81.815 No Selection
Home primetime PrimeTime.tcl (... vlsi@elc-v1111... IC Compiler II - ...

CELL DENSITY



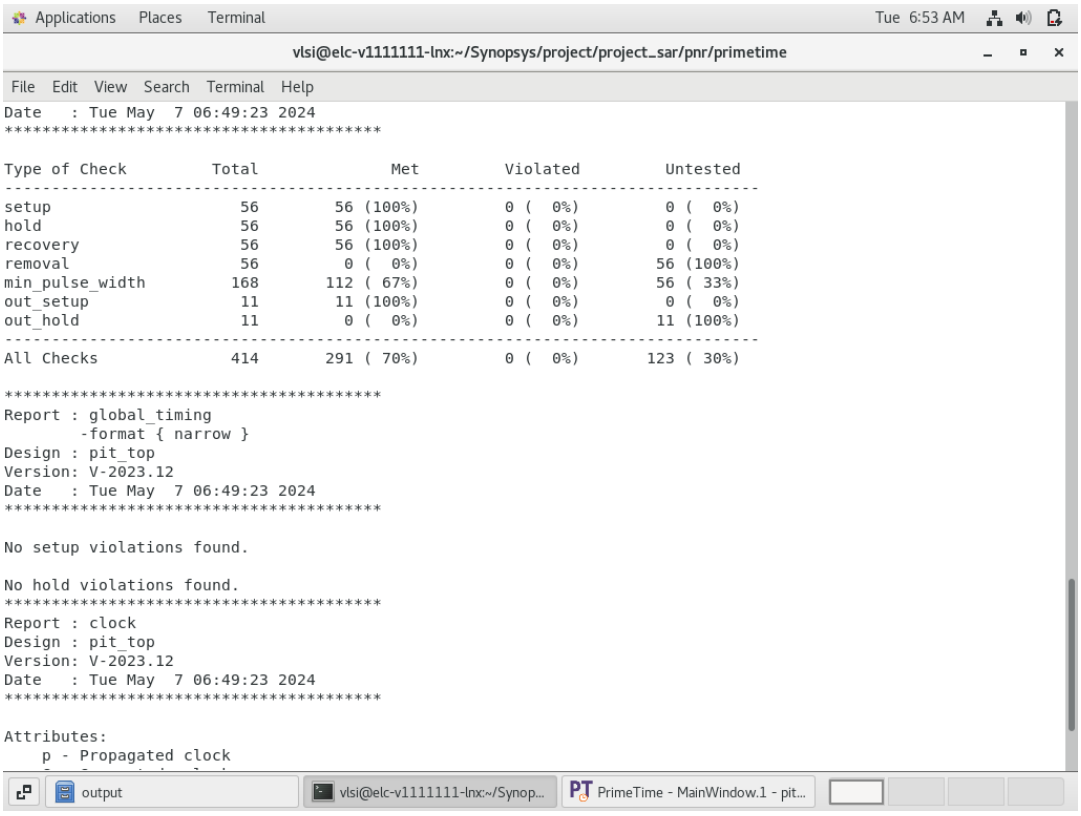
OUTPUT FILES

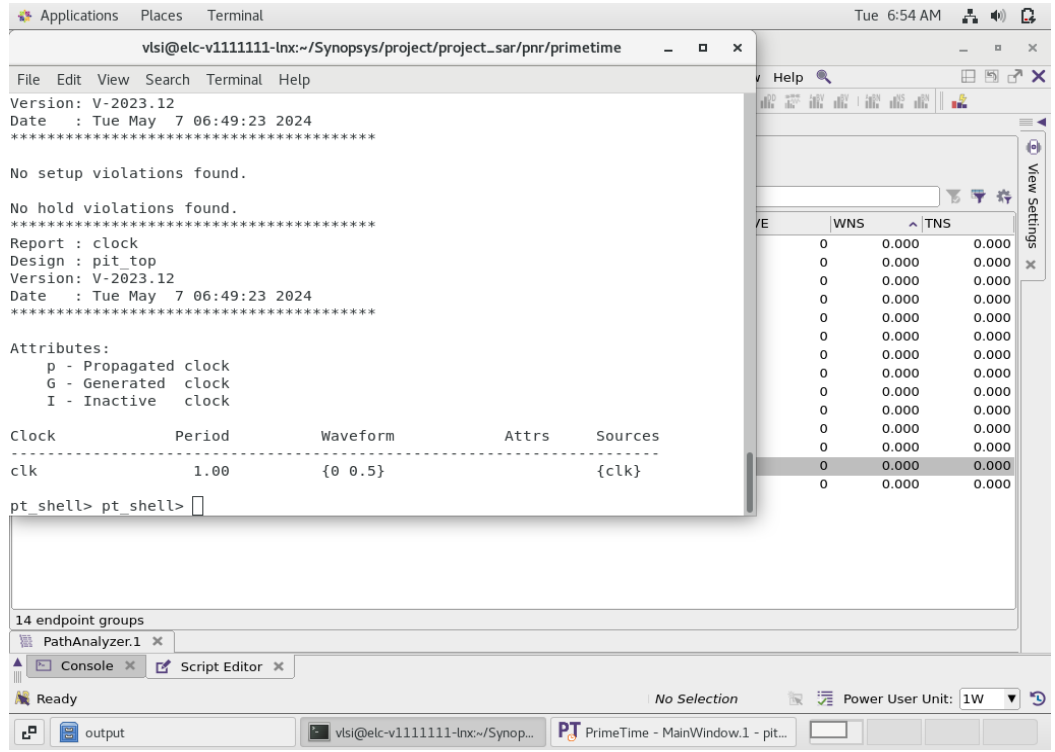
pit_top.gds	5/7/2024 3:34 AM	GDS File	4,652 KB
pit_top.out.def	5/7/2024 3:34 AM	DEF File	243 KB
pit_top.out.sdc	5/7/2024 3:34 AM	SDC File	6 KB
pit_top.out.spef.maxTLU_-40.spef	5/7/2024 3:34 AM	SPEF File	420 KB
pit_top.out.spef.minTLU_-40.spef	5/7/2024 3:34 AM	SPEF File	421 KB
pit_top.out.spef.spef_scenario	5/7/2024 3:34 AM	SPEF_SCENARIO Fi...	1 KB
pit_top.v	5/7/2024 3:34 AM	V File	50 KB

Prime Time

SCRIPT

```
# Prime Time Setup

set Design_name pit_top

set search_path /eda/synopsys/SAED90nm_EDK_10072017/SAED90_EDK/SAED_EDK90nm

set target_library $search_path/Digital_Standard_cell_Library/synopsys/models/saed90nm_max_lth.db

set link_path "* $target_library"

set Netlist_files  /home/vlsi/Synopsys/project/project_sar/pnr/output/pit_top.v

set SPEF_files    /home/vlsi/Synopsys/project/project_sar/pnr/output/pit_top.out.spef.spef_scenario

set constrains_file  /home/vlsi/Synopsys/project/project_sar/pnr/output/pit_top.out.sdc

# Netlist Reading from ICC2

read_verilog $Netlist_files

link_design pit_top

# Reading parasitics & constrains

read_parasitics  $SPEF_files

read_sdc $constrains_file

update_timing

# Checks

report_timing

report_analysis_coverage

report_global_timing

report_clocks
```


Applications Places Terminal
Tue 6:53 AM
vlsi@elc-v1111111-lnx:~/Synopsys/project/project_sar/pnr/primetime
File Edit View Search Terminal Help
Date : Tue May 7 06:49:23 2024
Type of Check Total Met Violated Untested
setup 56 56 (100%) 0 (0%) 0 (0%)
hold 56 56 (100%) 0 (0%) 0 (0%)
recovery 56 56 (100%) 0 (0%) 0 (0%)
removal 56 0 (0%) 0 (0%) 56 (100%)
min_pulse_width 168 112 (67%) 0 (0%) 56 (33%)
out_setup 11 11 (100%) 0 (0%) 0 (0%)
out_hold 11 0 (0%) 0 (0%) 11 (100%)
All Checks 414 291 (70%) 0 (0%) 123 (30%)
Report : global_timing
-format { narrow }
Design : pit_top
Version: V-2023.12
Date : Tue May 7 06:49:23 2024
No setup violations found.
No hold violations found.
Report : clock
Design : pit_top
Version: V-2023.12
Date : Tue May 7 06:49:23 2024
Attributes:
p - Propagated clock
output
vlsi@elc-v1111111-lnx:~/Synop...
PrimeTime - MainWindow.1 - pit...


Applications Places Terminal
Tue 6:54 AM
vlsi@elc-v1111111-lnx:~/Synopsys/project/project_sar/pnr/primetime
File Edit View Search Terminal Help
Version: V-2023.12
Date : Tue May 7 06:49:23 2024
No setup violations found.
No hold violations found.
Report : clock
Design : pit_top
Version: V-2023.12
Date : Tue May 7 06:49:23 2024
Attributes:
p - Propagated clock
G - Generated clock
I - Inactive clock
Clock Period Waveform Attrs Sources
clk 1.00 {0 0.5} {clk}
pt_shell> pt_shell>
WNS
TNS
View Settings
14 endpoint groups
PathAnalyzer.1
Console
Script Editor
Ready
No Selection
Power User Unit:
1W
output
vlsi@elc-v1111111-lnx:~/Synop...
PrimeTime - MainWindow.1 - pit...

REFERENCES

https://www.researchgate.net/publication/42387214_Linearity_Analysis_on_a_Series-Split_Capacitor_Array_for_High-Speed_SAR_ADCs

https://youtu.be/h0CGtr4SC9s