

ASSAIGNMENT 1

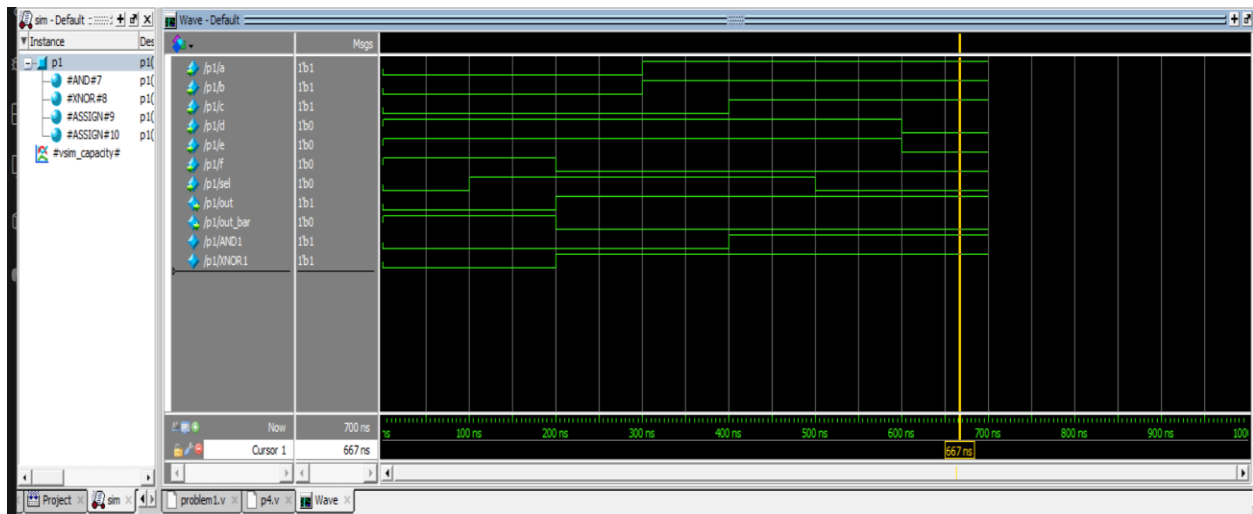
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P1)

Code :

```
E: > Digital_course > design > session1 > HA > Essential > .v files > problem1.v > ...  
1  module p1 (a,b,c,d,e,f,sel,out,out_bar) ;  
2  input a,b,c,d,e,f,sel;  
3  output out , out_bar;  
4  
5  wire AND1 , XNOR1;  
6  
7  and (AND1,a,b,c);  
8  xnor(XNOR1,d,e,f);  
9  assign out = (sel==1)?XNOR1:AND1;  
10 assign out_bar = ~out;  
11 endmodule
```

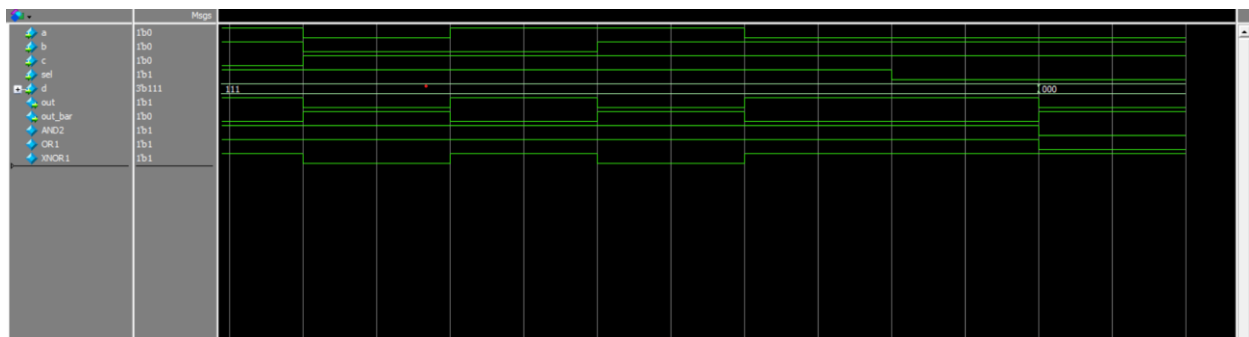
Waveform snippet:



P2) Code:

```
E: > Digital_course > design > session1 > HA > Essential > .v files > problem2.v > ...
1  module p2 (a,b,c,d,sel,out,out_bar);
2  input a,b,c,sel;
3  input [2:0]d;
4  output reg out ,out_bar;
5  reg AND2,OR1,XNOR1;
6
7  always @ (*) begin
8
9      AND2 = d[0] & d[1];
10     OR1  = d[2] | AND2;
11     XNOR1= a~^b~^c;
12     if (sel==1) begin
13         out = XNOR1;
14     end
15     else begin
16         out = OR1;
17     end
18     out_bar = ~out;
19 end
20 endmodule
```

Waveform snippet :

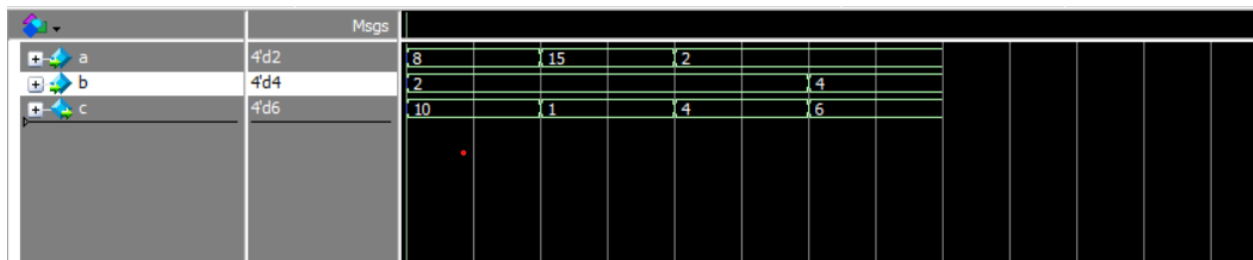


P3) code:

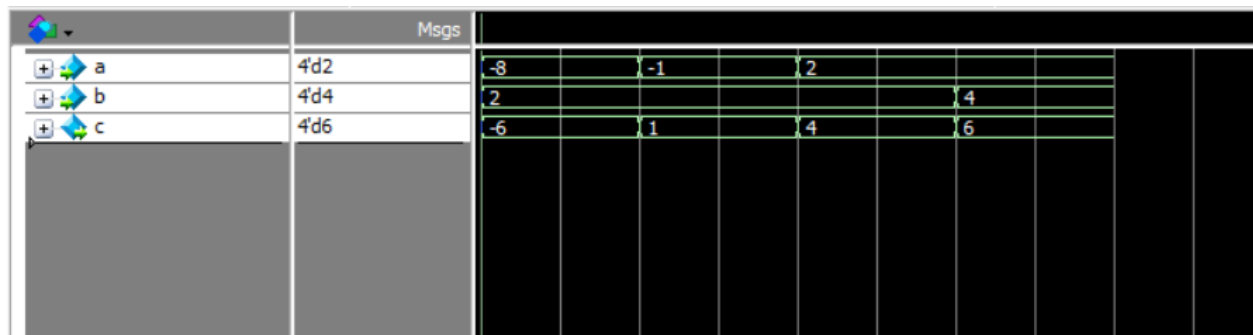
```
E: > Digital_course > design > session1 > HA > Essential > .v files > problem3.v > p3
1  module p3 (a,b,c);
2  input  [3:0] a,b ;
3  output [3:0] c ;
4
5  assign c = a + b ;
6  endmodule
```

Waveform snippet:

For unsigned adder



Signed adder:



P4) code:

```

1  module p4 (a , b );
2  parameter n = 2;
3  input [n-1:0] a;
4  output [2^n-1:0] b;
5
6  assign b = (a == 2'b00) ? 4'b0001 :
7  |          |          | (a == 2'b01) ? 4'b0010 :
8  |          |          | (a == 2'b10) ? 4'b0100 :
9  |          |          | 4'b1000 ;
10
11 endmodule
12
13

```

Waveform snippet:

[illegible]

P5) code:

```
E: > Digital_course > design > session1 > HA > Essential > .v files > problem5.v > ...
1  module p5 (a , b);
2  input [7:0] a;
3  output[8:0] b;
4  wire parity ;
5  assign parity = (a[0]^a[1]^a[2]^a[3]^a[4]^a[5]^a[6]^a[7]);
6
7  assign b = {a,parity};
8  endmodule
```

Waveform snippet:

	Msgs	
a	8b00000001	00001010 00001011 00000000 11111111 00000001
b	9b000000011	000010100 000010111 000000000 111111110 000000011
parity	1'b1	

P6) code :

```
E: > Digital_course > design > session1 > HA > Essential > .v files > problem6(2).v > nbit_alu
1  module nbit_alu (in0, in1 , opcode , out , enable , a,b,c,d,e,f,g);
2  parameter width = 4 ;
3  input [width-1:0] in0,in1 , enable;
4  input [1:0] opcode;
5  output reg [width-1:0] out;
6  output reg a,b,c,d,e,f,g
7  always @ (in0, in1 , opcode ) begin
8  case (opcode)
9  2'b00: out=in0+in1;
10 2'b01: out=in0|in1;
11 2'b10: out=in0-in1;
12 2'b11: out=in0^in1;
13 endcase
14 if (enable==1) begin
15     case (out)
16         4'h0: {a,b,c,d,e,f,g} = 7'b1111110;
17         4'h1: {a,b,c,d,e,f,g} = 7'b0110000;
18         4'h2: {a,b,c,d,e,f,g} = 7'b1101101;
19         4'h3: {a,b,c,d,e,f,g} = 7'b1111001;
20         4'h4: {a,b,c,d,e,f,g} = 7'b0110011;
21         4'h5: {a,b,c,d,e,f,g} = 7'b1011011;
22         4'h6: {a,b,c,d,e,f,g} = 7'b1011111;
23         4'h7: {a,b,c,d,e,f,g} = 7'b1110000;
24         4'h8: {a,b,c,d,e,f,g} = 7'b1111111;
25         4'h9: {a,b,c,d,e,f,g} = 7'b1111011;
26         4'hA: {a,b,c,d,e,f,g} = 7'b1110111;
27         4'hB: {a,b,c,d,e,f,g} = 7'b0011111;
28         4'hC: {a,b,c,d,e,f,g} = 7'b1001110;
29         4'hD: {a,b,c,d,e,f,g} = 7'b0111101;
30         4'hE: {a,b,c,d,e,f,g} = 7'b1001111;
31         4'hF: {a,b,c,d,e,f,g} = 7'b1001111;
32         default : {a,b,c,d,e,f,g} = 7'b0000000;
33     endcase
34 end
35 else {a,b,c,d,e,f,g} = 7'b0000000;
36 end
37 endmodule
```

Waveform snippet :

