[DOCUMENT TITLE]

Prepared by : YOUSSEF MOHAMED ABDELAAL BAYOUMI (gp2)
Yusuf Mohamed Sayed Hassan (gp1)
Omar Ayman Adel Elashkar (gp2)
Supervised by : ENG. Kareem Wassem

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1. QuestaSim Snippets

- **Check write operation**

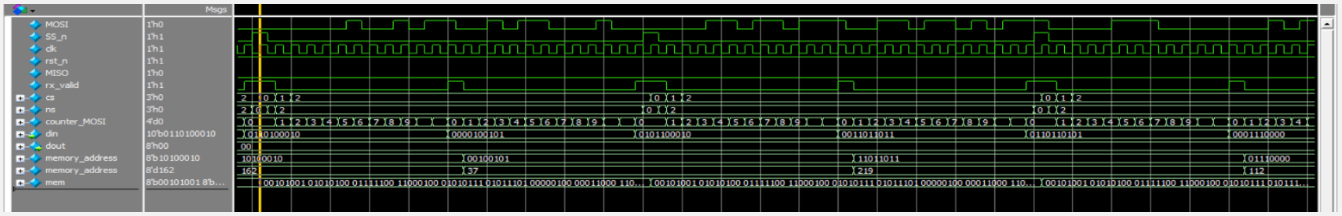

Figure 1: WRITE operation check

This snippet demonstrates the following behaviors:

- **State Transitions:**
  - 0 → IDLE state
  - 1 → CHCK_CMD (Check Command) state
  - 2 → WRITE state
- **Master Behavior (cs = 2):**
  - When **cs** is set to 2, the master receives the address after 10 clock cycles, followed by receiving the data after an additional 10 clock cycles.
- **Output Signals:**
  - **Dout** remains at 0, as no output is expected in this sequence.
  - **MISO** is held at 0 throughout.

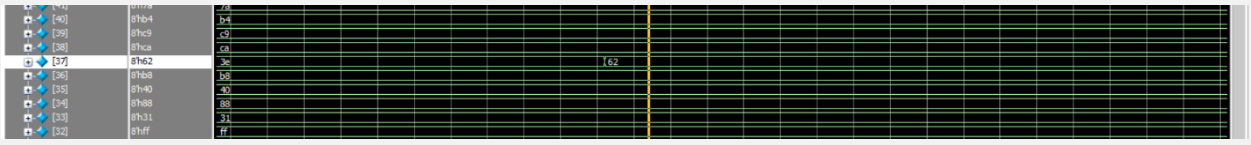

Figure 2: memory assigning check

This snippet demonstrates assigning memory address **37** with the value **0x62**, which corresponds to the binary input **0110 0010**.

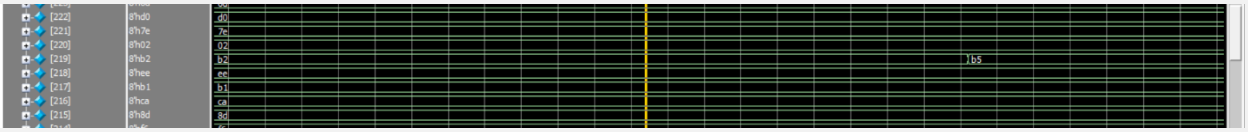

Figure 3: memory assigning check

This snippet demonstrates assigning memory address **219** with the value **0xb5**, which corresponds to the binary input **1011 0101**.

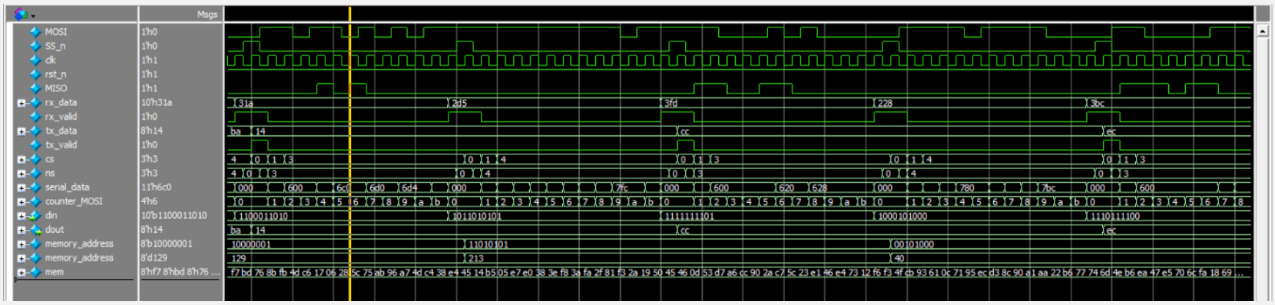

Figure 4: READ operation check

This snippet demonstrates the following behaviors:

- **State Transitions:**
    - 0 → IDLE state
    - 1 → CHCK_CMD (Check Command) state
    - 3 → READ_ADD (Read Address) state
    - 4 → READ_DATA (Read Data) state
- **Master Behavior (cs signal):**
    - When **cs** is set to 3, the master receives the address after 10 clock cycles.
    - When **cs** is set to 4, the master sends the data stored at the specified memory address to the slave device.
- **Output Signals:**
    - **Dout** is assigned the value read from the memory address.
    - **MISO** begins driving the assigned value, shifting it out serially over 8 clock cycles.

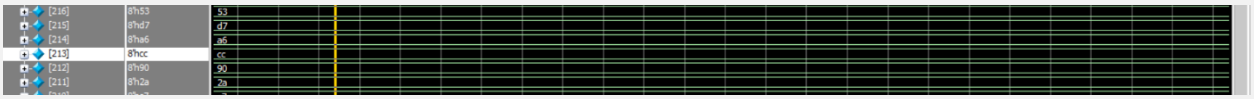

Figure 5: DOUT assigning check

This snippet demonstrates that the value stored at memory address **0x213** is correctly assigned to the **Dout** signal.

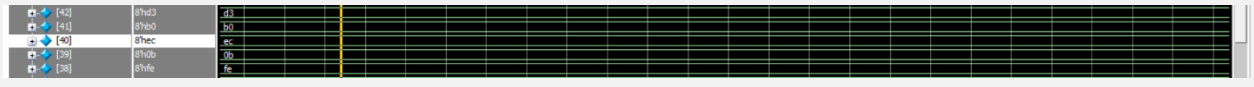

Figure 6: DOUT assigning check

This snippet demonstrates that the value stored at memory address **0x40** is correctly assigned to the **Dout** signal.

2. Linting (snippets showing no errors)

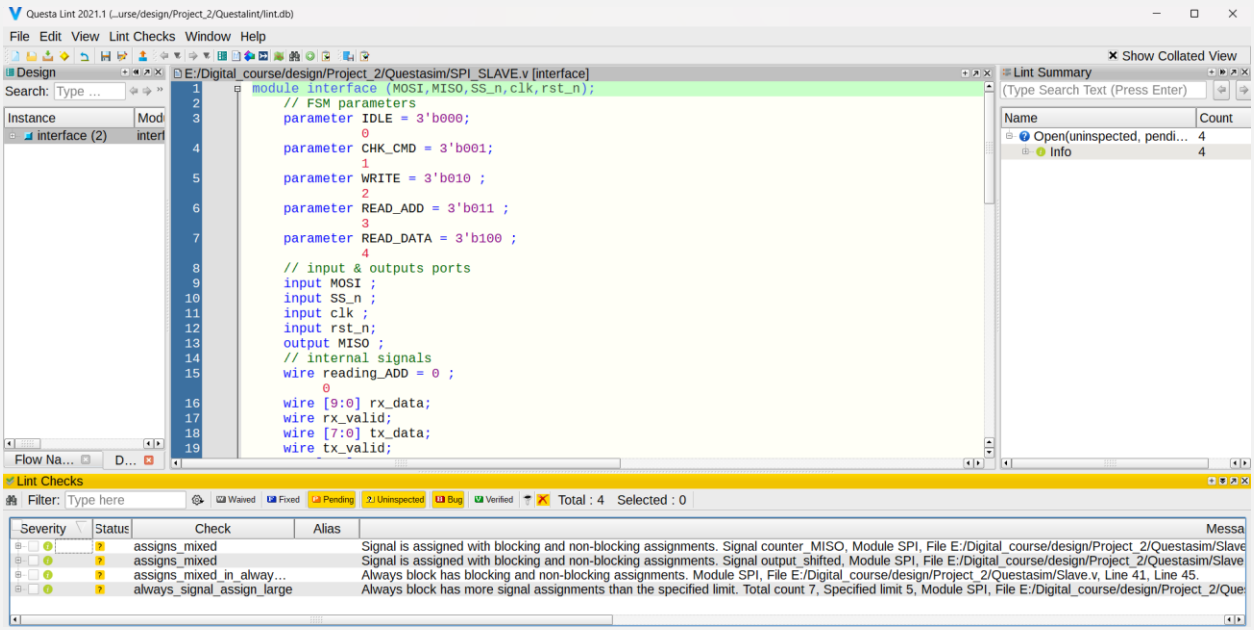

Figure7 : linting

3. Elaboration and synthetization

3.1. Elaboration schematic

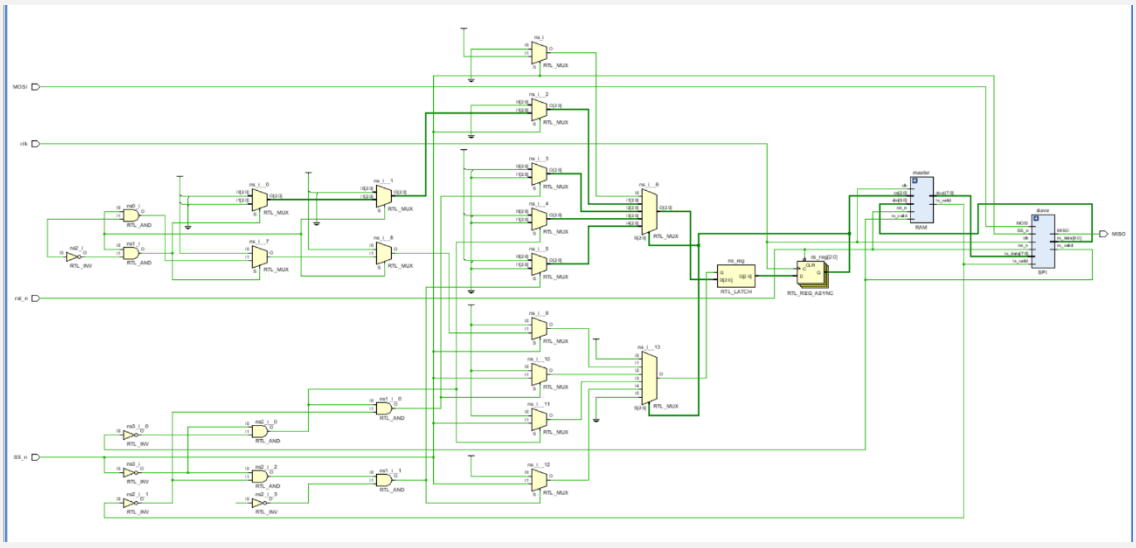

Figure8: RTL schematic

SPI slave

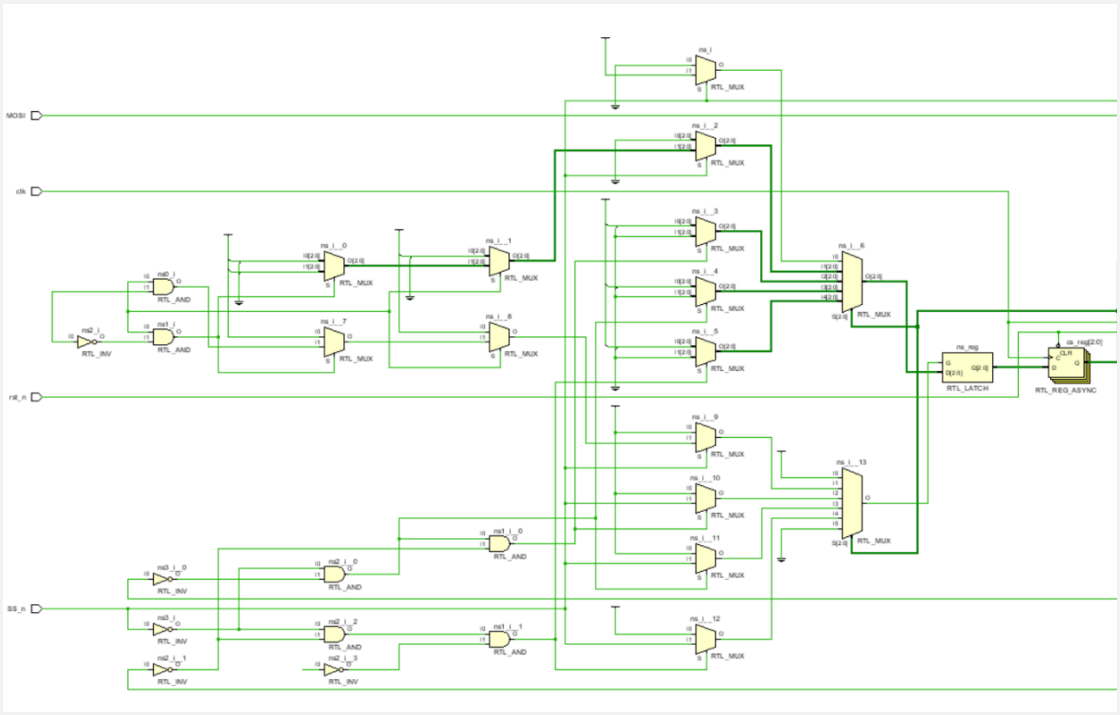

Figure9: RTL schematic

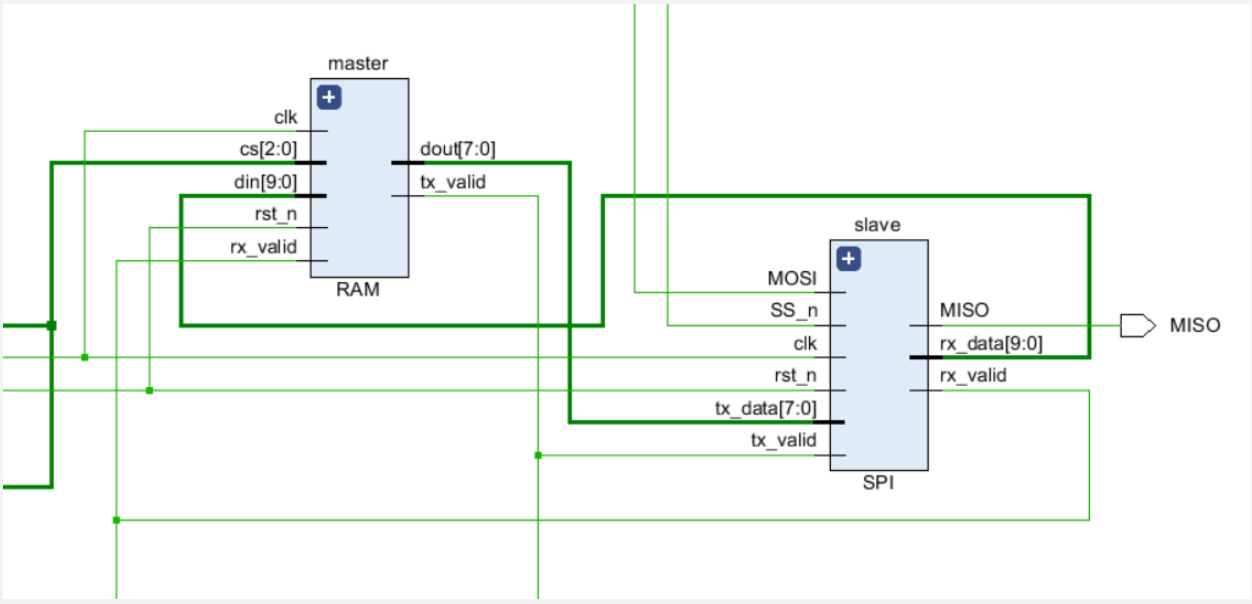

Figure10: RTL schematic

3.2. Synthesis schematic

- **Sequential encoding**
  - Synthesis schematic

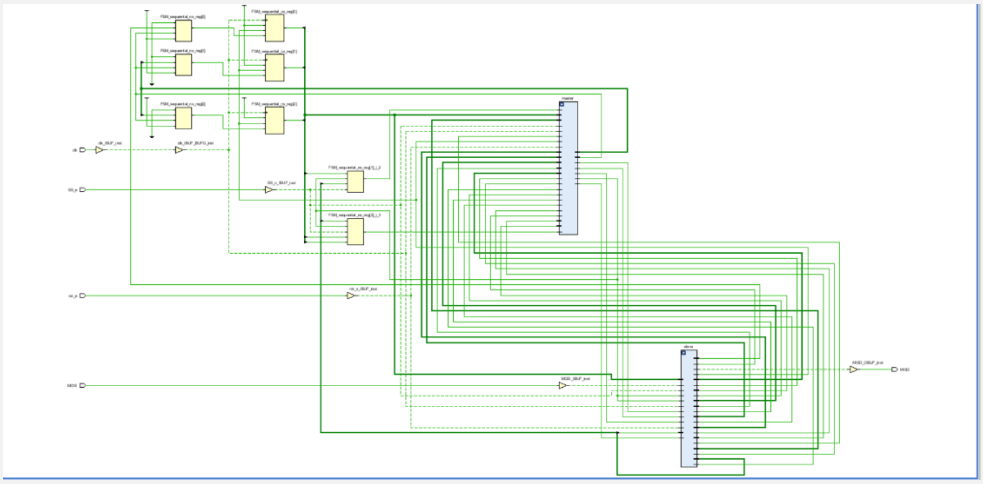

Figure11 :Synthesis schematic

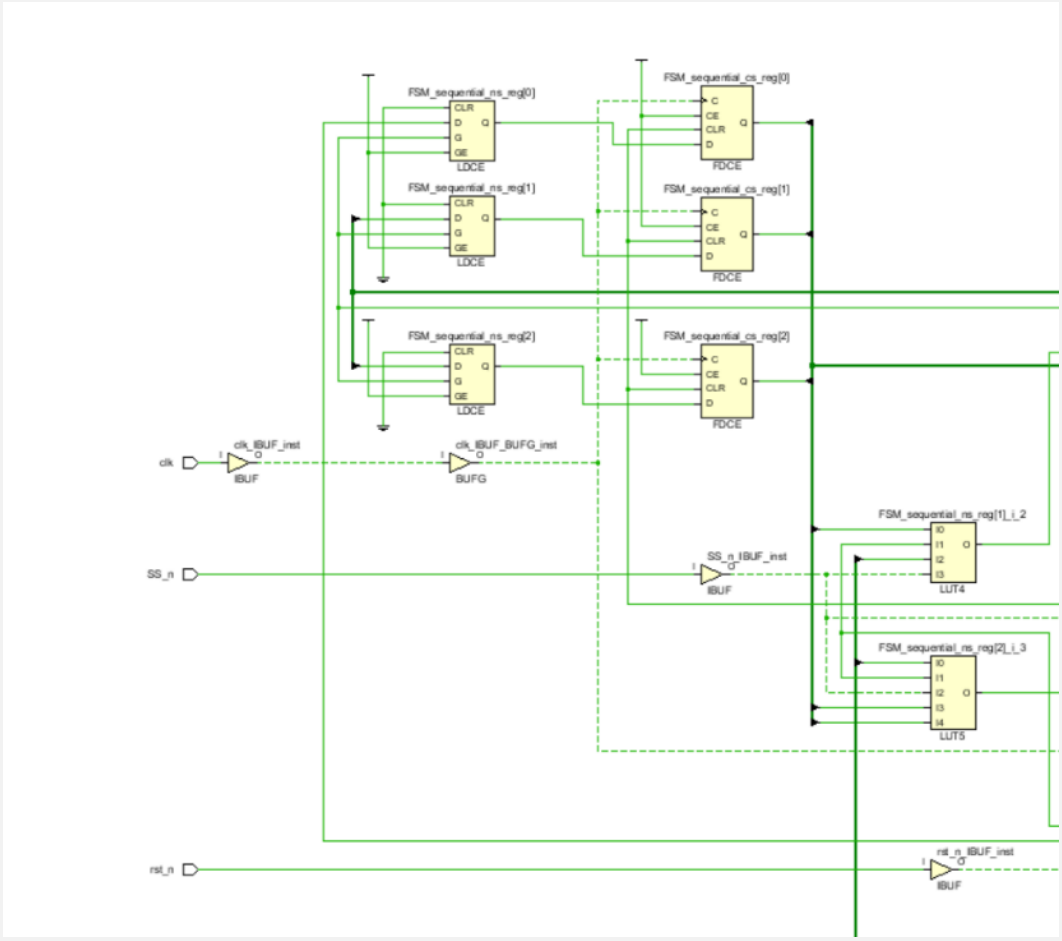

Figure12 :Synthesis schematic

SPI slave

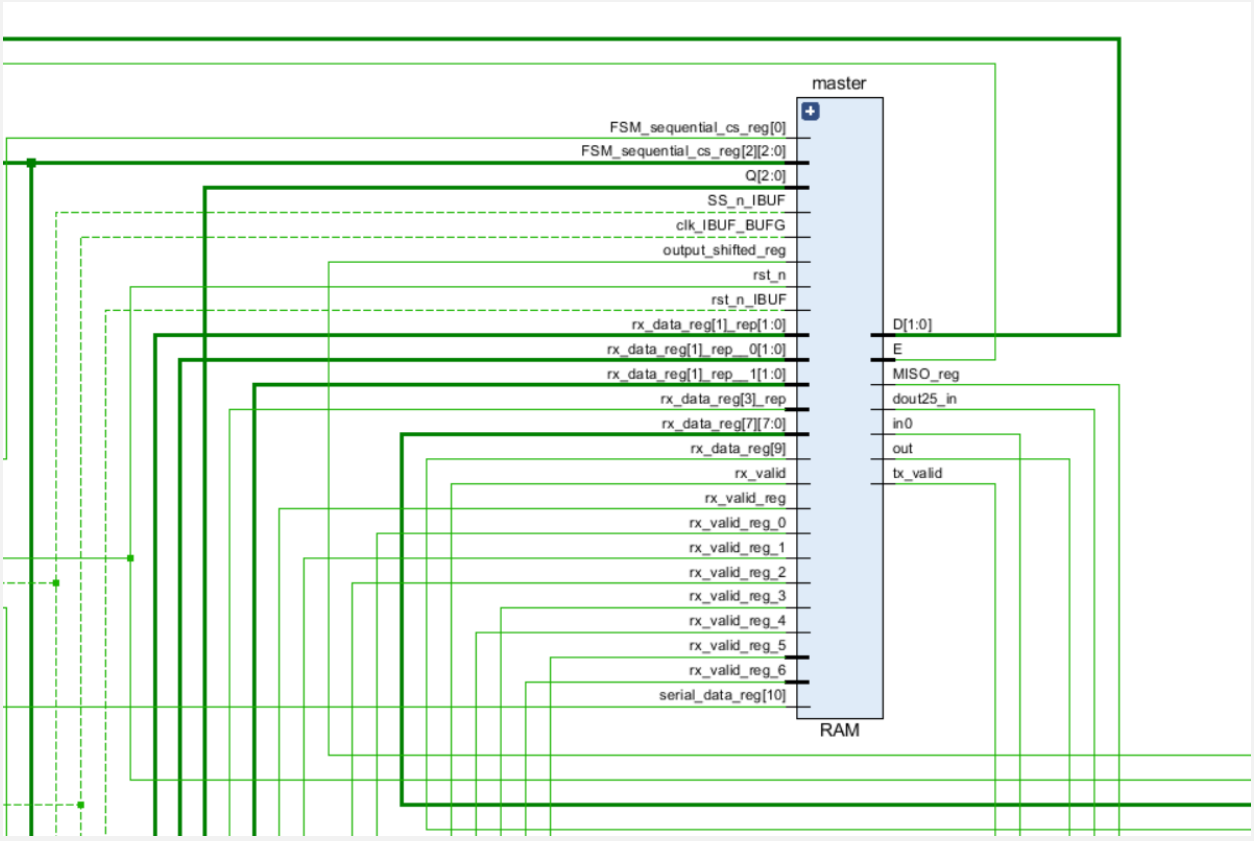

Figure13 :Synthesis schematic

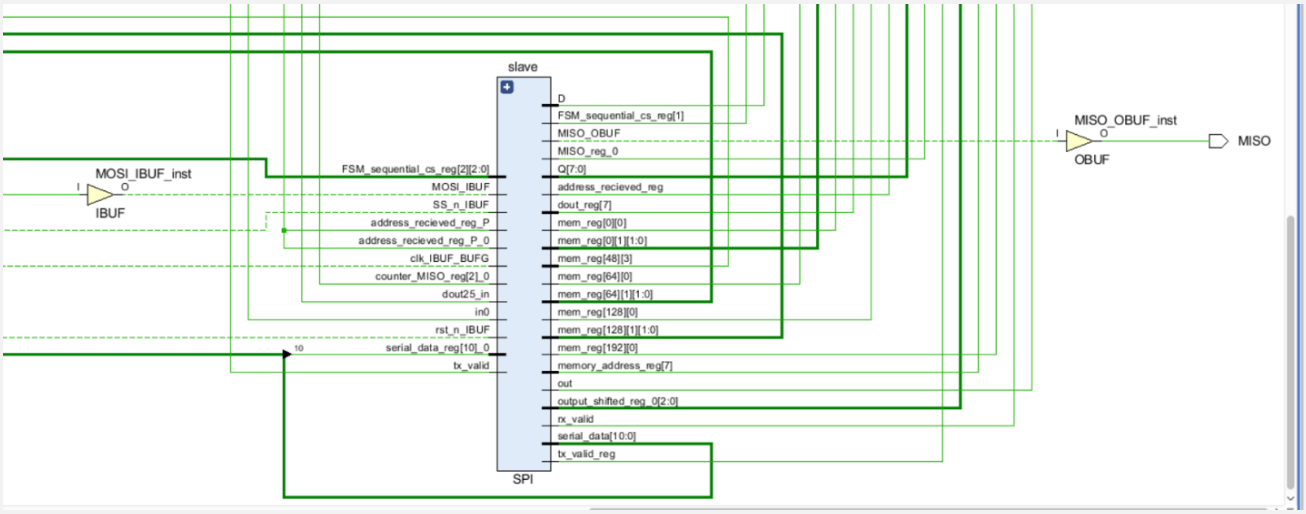

Figure14 :Synthesis schematic

- Synthesis report showing the encoding used

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	010	010
READ_ADD	011	011
READ_DATA	100	100

Figure 15: Synthesis report

- Timing report snippet

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.319 ns	Worst Hold Slack (WHS):	0.139 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4206	Total Number of Endpoints:	4206	Total Number of Endpoints:	2114

All user specified timing constraints are met.

Figure 16: Timing report

- **One_hot encoding**
  - Synthesis schematic

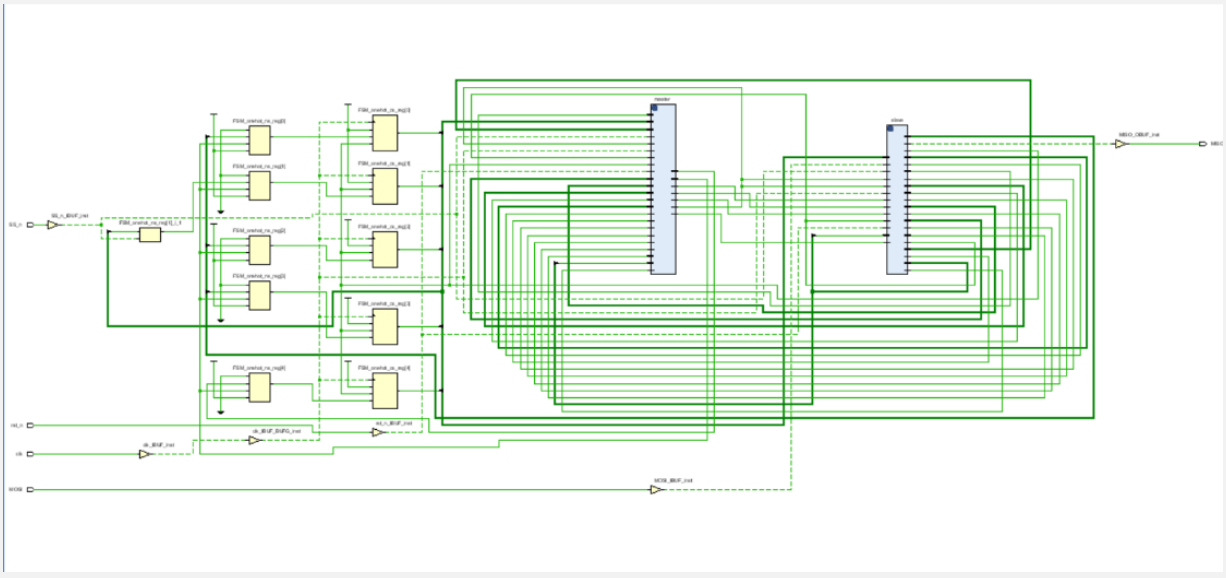

Figure17 :Synthesis schematic

SPI slave

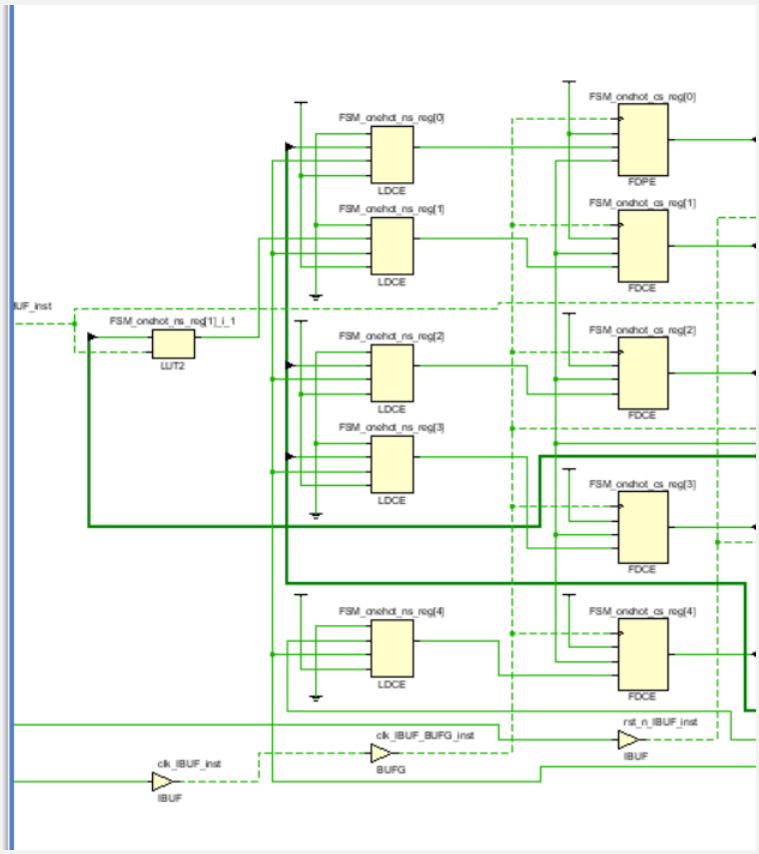

Figure18 :Synthesis schematic

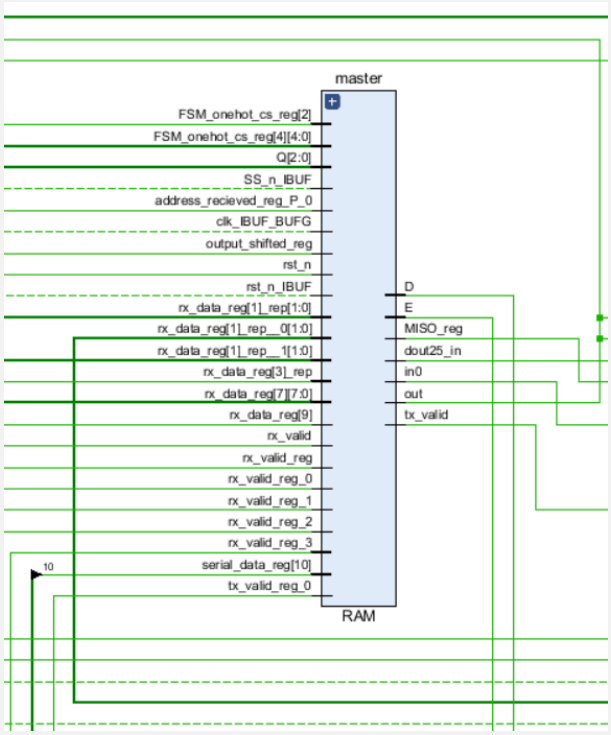

Figure19 :Synthesis schematic

SPI slave

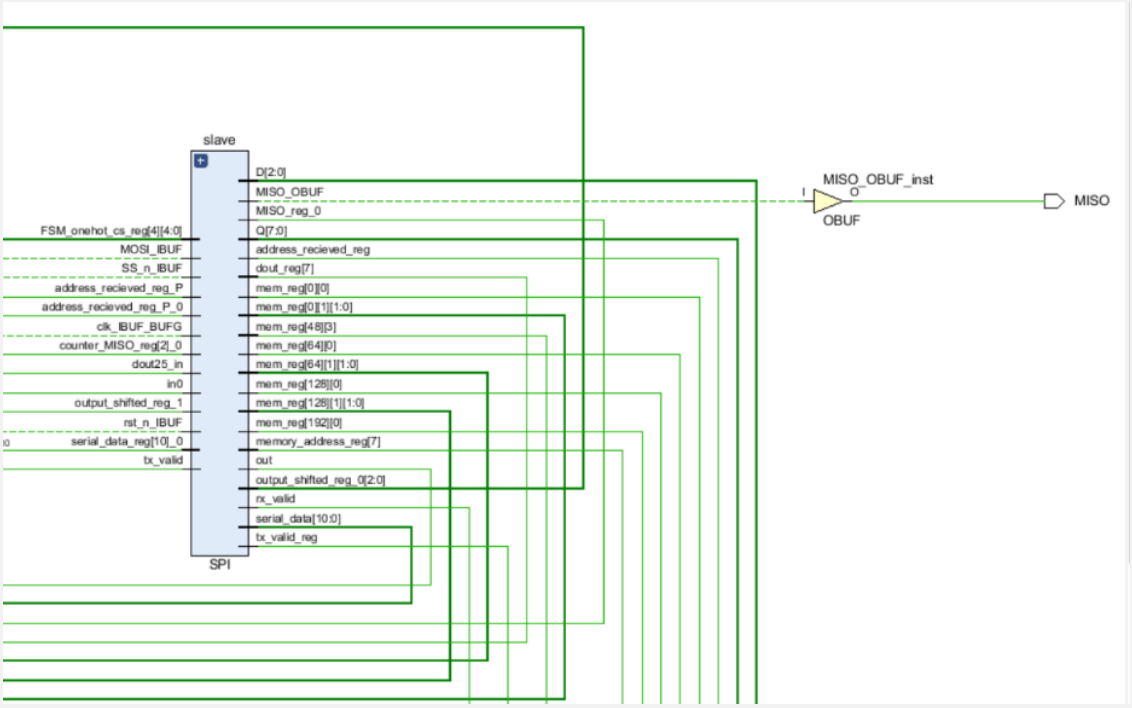

Figure20 :Synthesis schematic

- Synthesis report showing the encoding used

State	New Encoding	Previous Encoding
IDLE	00001	000
CHK_CMD	00010	001
WRITE	00100	010
READ_ADD	01000	011
READ_DATA	10000	100

Figure21: Synthesis report

- Timing report snippet

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.325 ns	Worst Hold Slack (WHS):	0.139 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4206	Total Number of Endpoints:	4206	Total Number of Endpoints:	2116

All user specified timing constraints are met.

Figure22: Timing report

- **Gray encoding**
  - Synthesis schematic

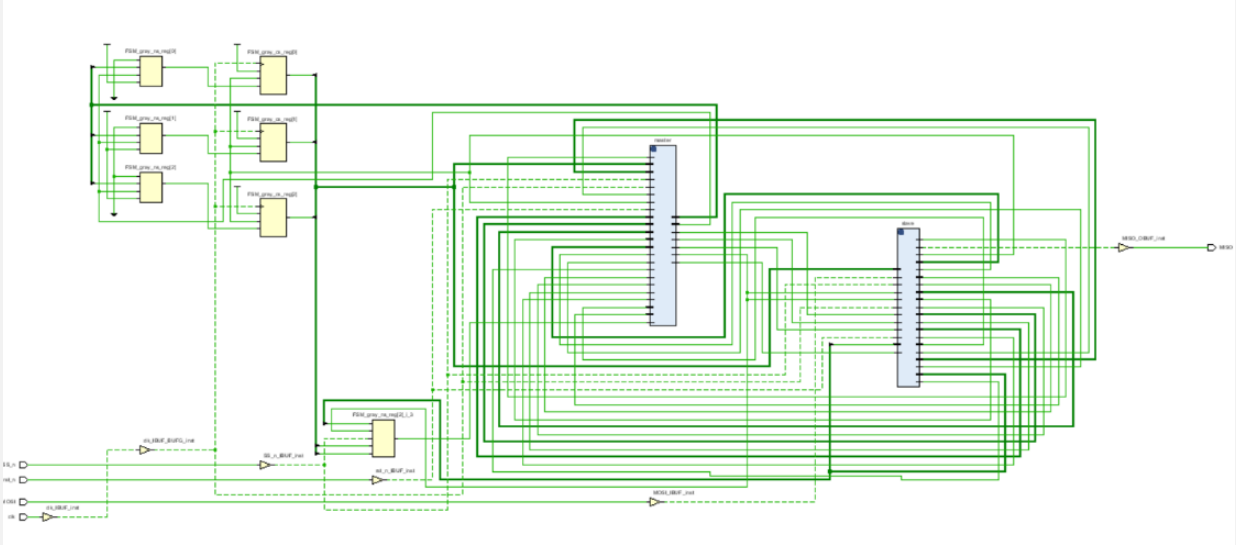

Figure23 :Synthesis schematic

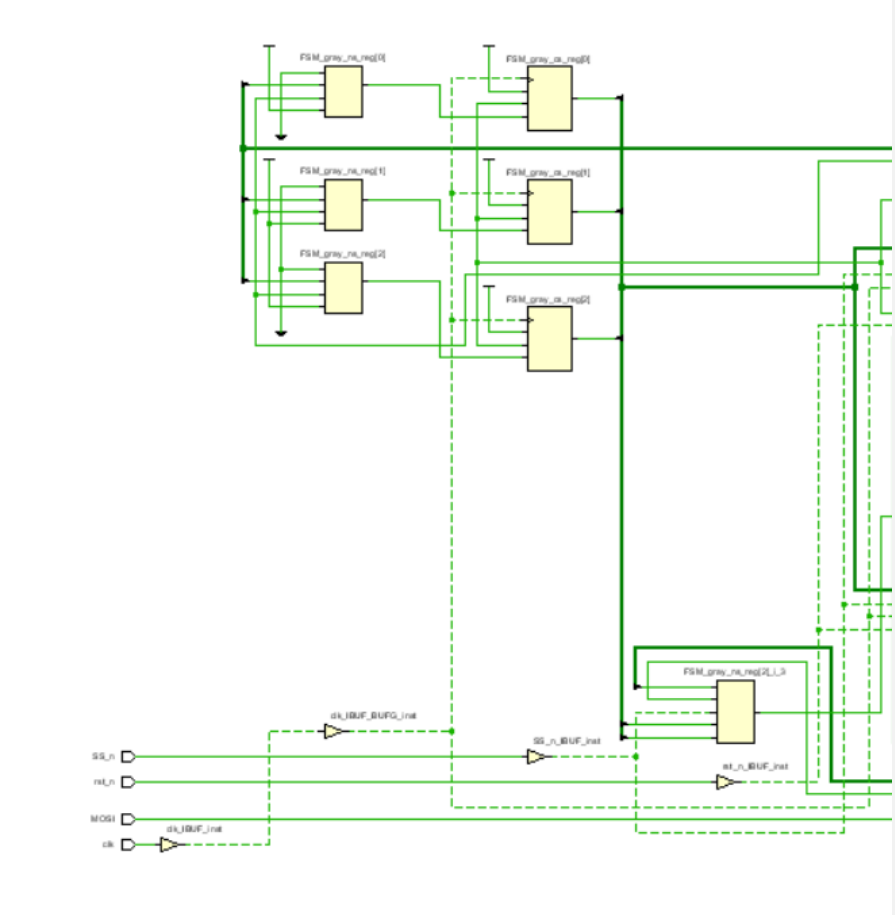

Figure24 :Synthesis schematic

SPI slave

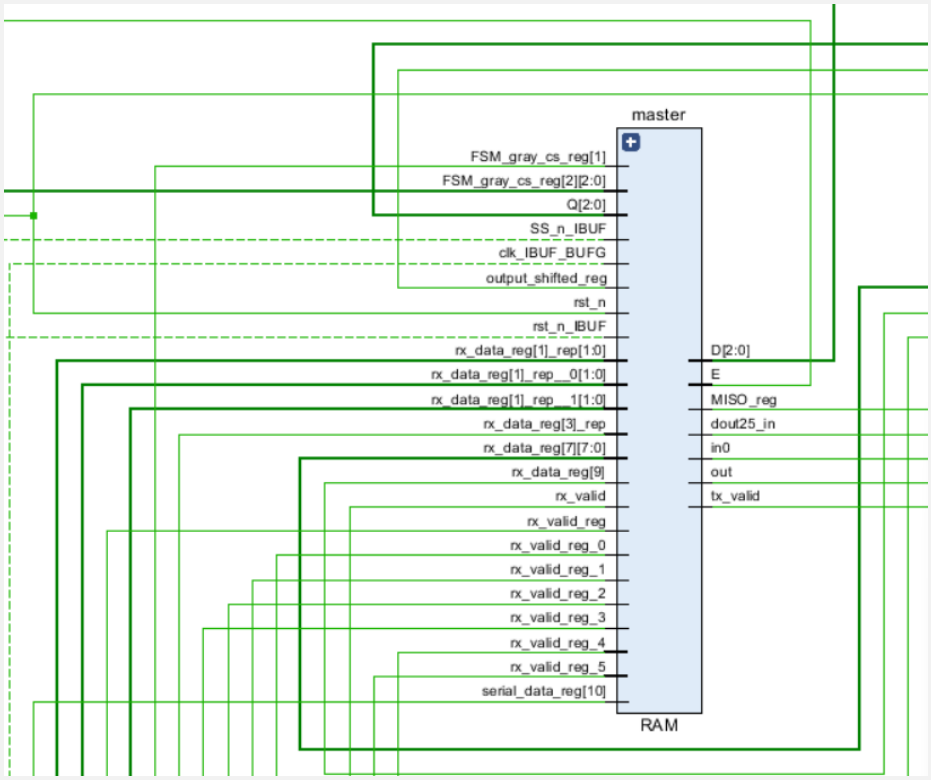

Figure25 :Synthesis schematic

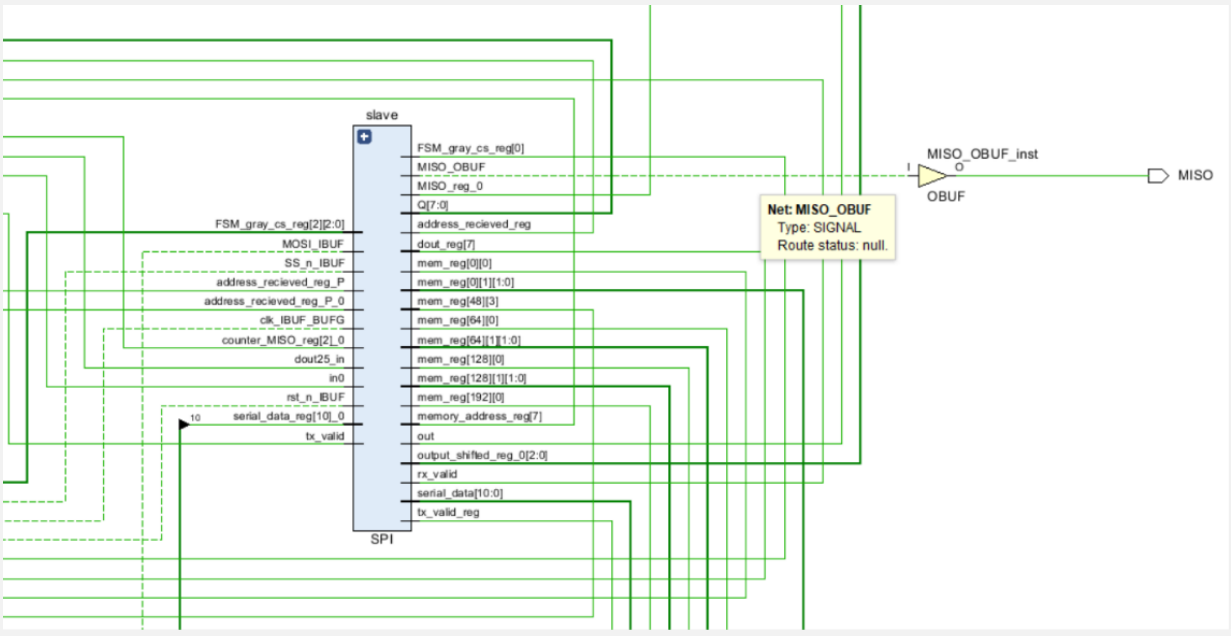

Figure26 :Synthesis schematic

- Synthesis report showing the encoding used

State	New Encoding	Previous Encoding
IDLE	000	000
CHK_CMD	001	001
WRITE	011	010
READ_ADD	010	011
READ_DATA	111	100

Figure27 : Synthesis report

- Timing report snippet

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	6.319 ns	Worst Hold Slack (WHS):	0.139 ns	Worst Pulse Width Slack (WPWS):	4.500 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	4206	Total Number of Endpoints:	4206	Total Number of Endpoints:	2114

All user specified timing constraints are met.

Figure28: Timing report

4. Implementation snippets for each encoding

- **Sequential encoding**
  - **Utilization report**

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
interface	2126	4031	283	136	1353	2018	108	763	0.5	5	2	1
dbg_hub (dbg_hub)	475	727	0	0	248	451	24	311	0	0	1	1
master (RAM)	851	2070	273	136	732	851	0	8	0	0	0	0
slave (SPI)	34	39	0	0	18	34	0	18	0	0	0	0
u_ila_0 (u_ila_0)	764	1189	10	0	363	680	84	423	0.5	0	0	0

Figure29: Utilization report

  - **Timing report**

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.098 ns	Worst Hold Slack (WHS):	0.037 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	7987	Total Number of Endpoints:	7971	Total Number of Endpoints:	4212

All user specified timing constraints are met.

Figure30: Timing report

- **FPGA device snippet**

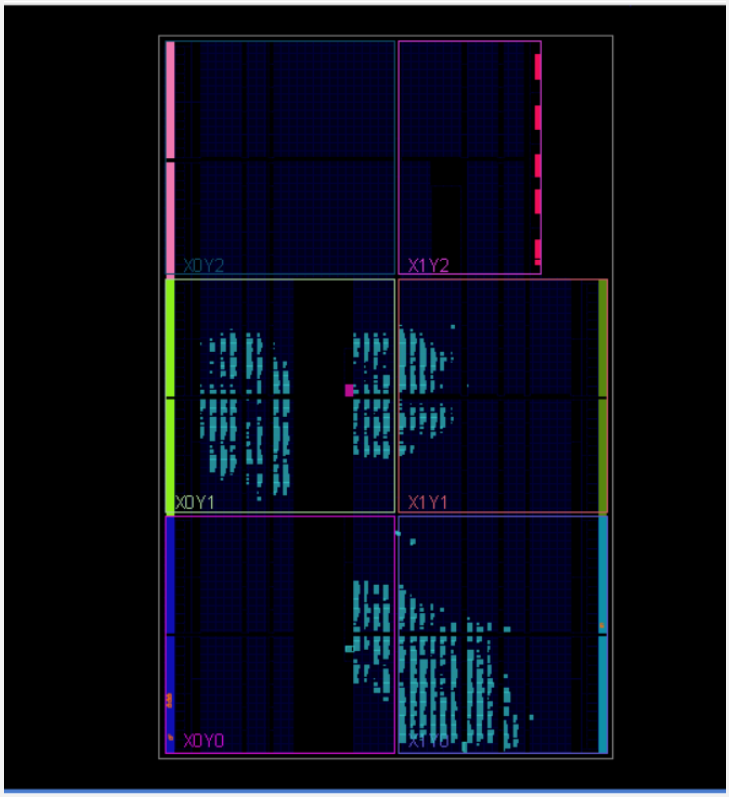

Figure31: Device snippet

- **One_hot encoding**
  - **Utilization report**

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
interface	2128	4035	283	136	1377	2020	108	772	0.5	5	2	1
dbg_hub (dbg_hub)	476	727	0	0	240	452	24	316	0	0	1	1
master (RAM)	851	2070	273	136	746	851	0	8	0	0	0	0
slave (SPI)	36	39	0	0	18	36	0	18	0	0	0	0
u_ila_0 (u_ila_0)	764	1189	10	0	383	680	84	425	0.5	0	0	0

Figure32: Utilization report

  - **Timing report**

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	1.525 ns	Worst Hold Slack (WHS):	0.049 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	7987	Total Number of Endpoints:	7971	Total Number of Endpoints:	4214

All user specified timing constraints are met.

Figure33: Timing report

- **FPGA device snippet**

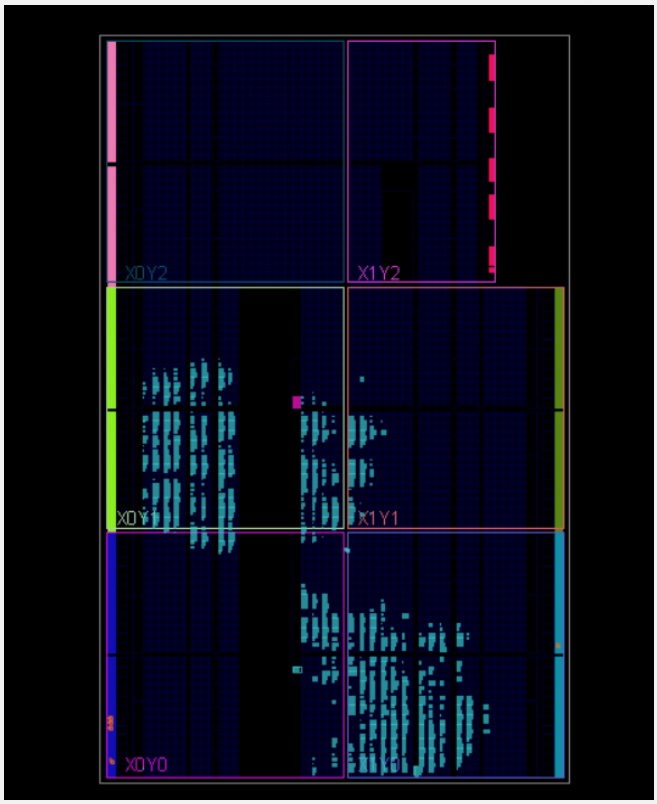

Figure34: Device snippet

- **Gray encoding**
  - **Utilization report**

Name	Slice LUTs (20800)	Slice Registers (41600)	F7 Muxes (16300)	F8 Muxes (8150)	Slice (8150)	LUT as Logic (20800)	LUT as Memory (9600)	LUT Flip Flop Pairs (20800)	Block RAM Tile (50)	Bonded IOB (106)	BUFGCTRL (32)	BSCANE2 (4)
interface	2129	4031	283	136	1403	2021	108	767	0.5	5	2	1
dbg_hub (dbg_hub)	476	727	0	0	243	452	24	311	0	0	1	1
master (RAM)	852	2070	273	136	778	852	0	8	0	0	0	0
slave (SPI)	35	39	0	0	15	35	0	17	0	0	0	0
u_ila_0 (u_ila_0)	765	1189	10	0	377	681	84	425	0.5	0	0	0

Figure35: Utilization report

  - **Timing report**

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0.466 ns	Worst Hold Slack (WHS):	0.036 ns	Worst Pulse Width Slack (WPWS):	3.750 ns
Total Negative Slack (TNS):	0.000 ns	Total Hold Slack (THS):	0.000 ns	Total Pulse Width Negative Slack (TPWS):	0.000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	7987	Total Number of Endpoints:	7971	Total Number of Endpoints:	4212

Figure36: Timing report

- **FPGA device snippet**

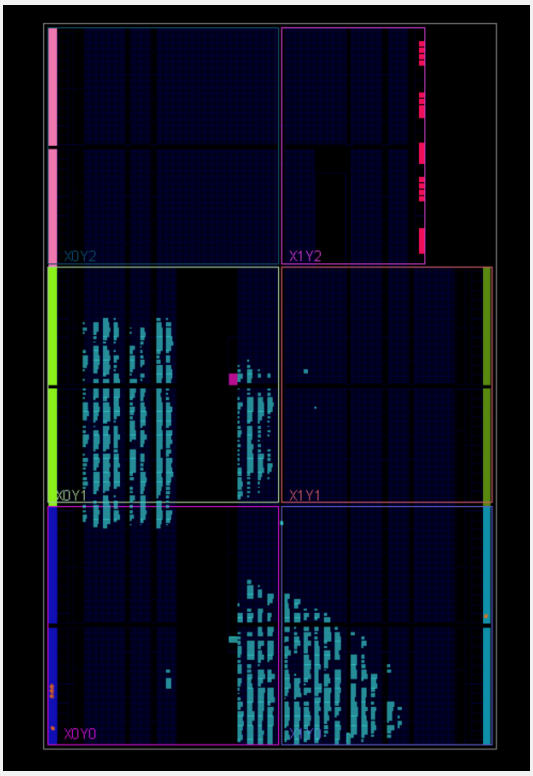

Figure37: Device snippet

Since the **one_hot encoding report** shows a slightly better WNS of **6.325 ns** (vs. 6.319 ns), it offers a tiny bit more setup slack — which means it can theoretically achieve a slightly higher maximum frequency.

Therefore, the one_hot encoding represents the best choice to achieve the highest operating frequency.

5. Snippet of the “Messages” tab showing no critical warnings or errors after running elaboration, synthesis, implementation and a successful bitstream generation. (using one_hot encoding)

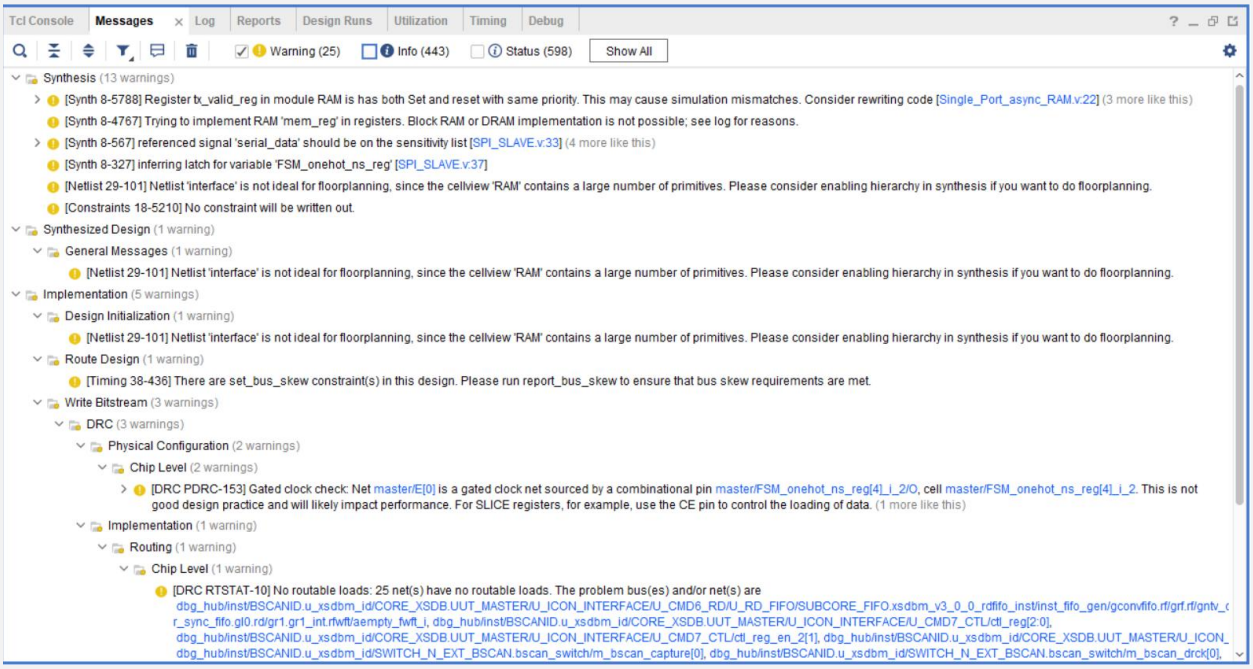

Figure38: Message tab