Faculty of Engineering

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3rd Year Computer and Systems Dep.

Computer Organization II

8255A-PPI Project Report

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The Code:

Declaration:

Type	Name
Inouts	PA, PB, PC, D
Inputs	A, RD, WR, CS , reset
Wires	PCu, PCl
Registers	PAr, PBr, PCr, Dr
Flag Registers	PAout, PBout, PCuout PClout, Dout

```
1   `timescale 1ns / 1ps
2
3   module ppi (PA,PB,PC,D,A,RD,WR,CS,reset);
4
5           inout  [7:0]PA; //8-bits of Port-A
6           inout  [7:0]PB; //8-bits of Port-B
7           inout  [7:0]PC; //8-bits of Port-C
8           inout  [7:0]D;  //8-bits of Data
9           input  [1:0] A; //2-bit for port selection
10          input  RD, // on low read  data from ports
11                     WR, // on low write data into ports
12                     CS, // on low processor selects this chip
13                     reset; // all ports became in input state
14
15
16        wire [3:0] PCu;
17        wire [3:0] PCl;
18        assign PC={PCu,PCl};
19
20                reg [7:0]PAr;
21                reg [7:0]PBr;
22                reg [7:0]PCr;
23                reg [7:0]Dr;
24
25                reg PAout,PBout,PCuout,PClout,Dout; //flags
```

```
27              //conditioning inout
28
29          assign PA =(PAout)?PAr:8'bzzzz_zzzz;
30          assign PB =(PBout)?PBr:8'bzzzz_zzzz;
31          assign PCu =(PCuout)?PCr[7:4]:4'bzzzz;
32          assign PCl =(PClout)?PCr[3:0]:4'bzzzz;
33          assign D = (Dout) ?Dr:8'bzzzz_zzzz;
```

If Ports A, B or C are supposed to be outputs, they are assigned to their respective values in the registers. However, if they are inputs, we initially assign them to 8’bzzzz_zzzz.

```
35  //on reset
36
37          always@(reset)
38
39          begin
40                  if(reset == 1)
41                  begin
42                          PAout=0;
43                          PBout=0;
44                          PCuout=0;
45                          PClout=0;
46                          Dout =0;
47                  end
48          end
49
```

When Reset is equal to “1”, all the ports are assigned to 8’bzzzz_zzzz.

BSR Mode Code

```
50  //BSR mode
51
52          always@(CS_bar or D)
53          begin
54                  if(CS_bar==0 && D[7]==1'b0 && reset==0 && A==2'b11)
55                  begin
56                          PCuout=1;
57                          PClout=1;
58                          if(D[0]==1'b1)
59                          begin
60                                  PCr[D[3:1]] <= 1'b1;
61                          end
62                          else if(D[0]==1'b0)
63                          begin
64                                  PCr[D[3:1]] <= 1'b0;
65                          end
66                  end
67          end
68
69
```

Mode 0:

A_1	A_0	RD	WR	CS	Result
0	0	0	1	0	**Input Operation** PORT A → Data Bus
0	1	0	1	0	PORT B → Data Bus
1	0	0	1	0	PORT C → Data Bus
0	0	1	0	0	**Output Operation** Data Bus → PORT A
0	1	1	0	0	Data Bus → PORT A
1	0	1	0	0	Data Bus → PORT B
1	1	1	0	0	Data Bus → PORT D

Read Mode:

```
72          always@(CS_bar or PA or PB or PC or A or D)
73          begin
74                  if(CS_bar==0 && D[7]==1'b1 && reset==0 )
75                  begin
76                    //Read mode
77
78                    if( RD_bar==0 )
79                    begin
80                          //read from port A
81                                  if(A == 2'b00)
82                                  begin
83                                    Dout<=1;
84                                    Dr<=PA;
85                                  end
86                          //read from port B
87                                  else if (A ==2'b01)
88                                  begin
89                                    Dout<=1;
90                                    Dr<=PB;
91                                  end
92
93                          //read from port C
94                                  else if (A == 2'b10)
95                                  begin
96                                    Dout<=1;
97                                    Dr<=PC;
98                                  end
99                          //assigning ports in case A=11
100                                 else if(A ==2'b11 )
101                                 begin
102                                         Dout    <= 0;
103                                         PAout   <= ~(D[4]);
104                                         PBout   <= ~(D[1]);
105                                         PCuout  <= ~(D[3]);
106                                         PClout  <= ~(D[0]);
107                                 end
108
109                 end
```

If the chip is on mode 0, according to the table above, the output is determined by the signals A, Read, Write.

If it is on Read (active low signal), the input is taken from the specific port to the data register and then to Port D as output.

Write Mode:

```
110                     //Write mode
111
112                           else if ( WR_bar==0)
113
114                                   //A write into D
115                                   if(A == 2'b00)
116                                   begin
117                                     Dout<=0;
118                                     PAr<=D;
119                                   end
120                                   //B write into D
121                                   else if (A ==2'b01)
122                                   begin
123                                     Dout<=0;
124                                     PBr<=D;
125                                   end
126                                   //C write into D
127                                   else if (A == 2'b10)
128                                   begin
129                                     Dout<=0;
130                                     PCr<=D;
131                                   end
132
133                                   else if(A ==2'b11)
134                                           begin
135                                                   Dout    <= 0;
136                                                   PAout   <= ~(D[4]);
137                                                   PBout   <= ~(D[1]);
138                                                   PCuout  <= ~(D[3]);
139                                                   PClout  <= ~(D[0]);
140                                           end
141                     end
142                   end
143   endmodule
```

If it is on Write (active low signal), the input is taken from the Data port to the a port register (depending on the value of A) and then to the Port as output.

The Test Bench:

Declaring the parameters (same as the module):

```
145  module TB(
146      );
147
148  wire [7:0] PA,PB,PC,D;
149  reg [7:0] PAr,PBr,PCr,Dr;
150
151  reg reset,CS_bar,RD_bar,WR_bar;
152  reg [1:0] A;
153
154  reg PAout;
155  reg PBout;
156  reg PCout;
157  reg  Dout;
158  assign PA = (~PAout)?PAr:8'bzzzzzzzz;
159  assign PB = (~PBout)?PBr:8'bzzzzzzzz;
160  assign PC = (~PCout)?PCr:8'bzzzzzzzz;
161  assign D  = (~Dout) ? Dr:8'bzzzzzzzz;
162
```

Test Cases:

1- Reset = 1 and CSbar=0 (regardless of all the other signals):

```
163  initial
164  begin
165  #5
166  $display("|    port A     |    port B     |    port C     |    port D     | A |  RD  |  WR  |  reset  |  CS |");
167  $monitor("|  %b  |   %b  |  %b  |  %b  |  %b  |  %b  | %b  |   %b   | %b |",PA,PB,PC,D,A,RD_bar,WR_bar,reset,CS_bar);
168  //reset
169  PAout=0;
170  PBout=0;
171  PCout=0;
172  Dout=0;
173
174  CS_bar = 1'b0;
175  reset = 1;
176  #10
177  reset = 0;
```

The expected output: 8’bxxxx_xxxx for all ports at the start

```
# |    port A     |    port B     |    port C     |    port D     | A |  RD  |  WR  |  reset  |  CS |
# |  xxxxxxxx  |   xxxxxxxx  |  xxxxxxxx  |  xxxxxxxx  |  xx  |  x  | x  |   1   | 0 |
```

2- BSR Mode

D = 8'b00001111, A = 3, Reset = 0, CSbar = 0

```
179   //BSR mode
180   A = 3;
181
182   PCout=1;
183
184   Dr = 8'b00001111;
```

The expected output: PC = 1xxx_xxxx

```
# |  xxxxxxxx  |  xxxxxxxx  |  1xxxxxxx  |  00001111  |  11  |  x  | x  |  0  | 0 |
```

3- Mode 0 (Write)

D = 8’b1000_0000, A = 3, RDbar = 1, WRbar = 0

```
187   //mode 0 writing on ports
188
189   PAout=1;
190   PBout=1;
191   PCout=1;
192   Dout=0;
193
194   A=3;
195   Dr= 8'b10000000;
196   RD_bar = 1'b1;
197   WR_bar = 1'b0;
```

The Expected output: