THE AMERICAN UNIVERSITY IN CAIRO
School of Sciences and Engineering

Department of Computer Science and Engineering

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CSCE 330402/ Digital Design II

Project 2 - MS2

Plan and Prototype 1

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Project Brief and Objectives

In Figure 2, it shows how the given RTL verilog code is synthesized using yosys tool to the below given gate level netlist, consisting of a multiplexer and a register bank (consisting of multiple flip flops), where the output of the register bank is fed back to the multiplexer while the the enable signal is set to 0, while when the enable signal is set to 1, D_IN value is fed to the multiplexer and the dataflow process continues.

The aforementioned gate level structure is fully functional and operational however, it consumes a high amount of dynamic power. The optimal solution for this issue is to reduce the high power consumption by removing this structure into another efficient structure, Integrated Clock Gating (ICG), which is shown below in Figure 2. This structure uses Integrated Clock Gating (ICG) methodology where a latch connected to AND gate with enable and clock inputs, connected to the flip flop.

The goal of this project is to develop a utility that is able to check all the given gate level netlist scripts and parse it to identify the first structure (MUX and fliplflops) and replace it by the optimized structure (using the ICG). This process is identified as Automatic Clock Gating.

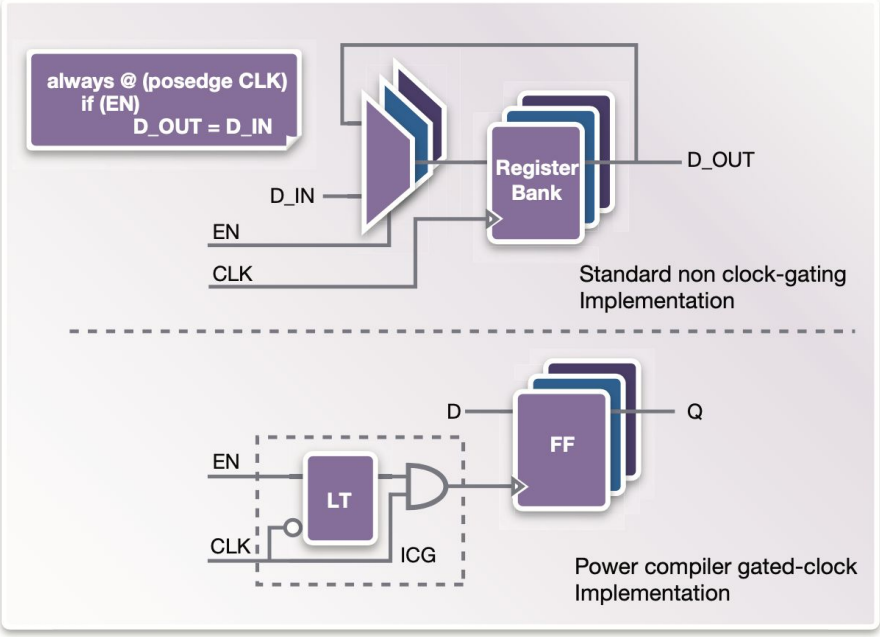
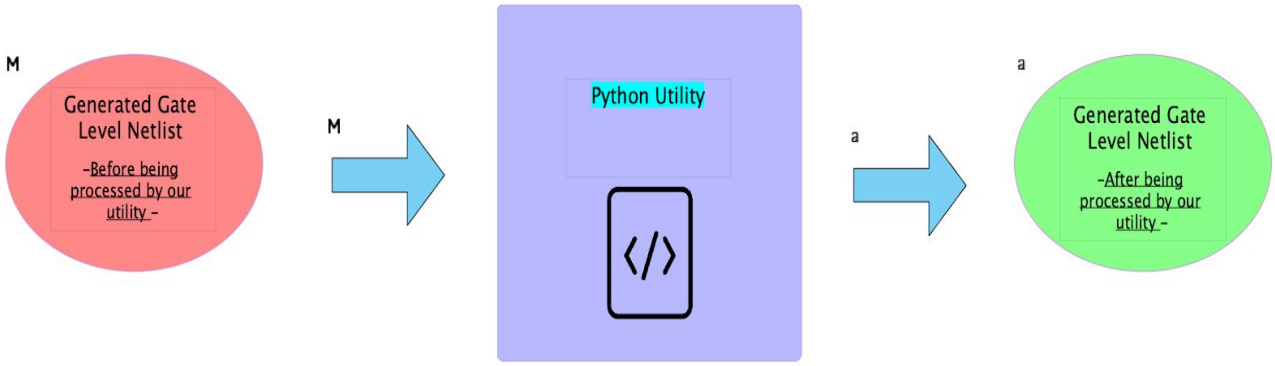


Figure 2: Power Compiler performs automatic clock gating to reduce dynamic power consumption.

The mechanism of the utility that we are going to develop is shown below, where the generated gate level netlist script is provided to our utility to be processed by identifying removing the high power consuming structure and replacing it with the optimized gate level structure using Integrated Clock Gating (ICG).



Identification of the Used Programming Languages and Libraries

In this project, we are planning to develop the utility that will parse the given gate level netlist script and modify it as explained above using Python programming language supported by pyverilog library. We have chosen this programming language and specifically this python library as it will help us to parse the given verilog code (provided gate level netlist) and generate the modified power efficient version of it.

This library allows us to visualize all the provided verilog code in the gate level netlist script by displaying a complete syntax analysis report [inputs/wires/always statements…..etc.]. Also, it will allow us to generate the updated verilog code by manipulating it using python.

Project Plan

We are planning to develop a complete functional utility that will be able to parse the given gate level netlist and generate the modified gate level netlist version of it which is power optimized using ICG.

References

- Power Optimization in Design Compiler, Synopsys Datasheet.