Name: Solution COMP228 Marks: /50 → 48
ID: Midterm
Answer All Questions in the Spaces Provided

1(a) Identify the layer of abstraction to which the following components belong.

Cache:	control
Sequential Circuit:	logic
Program Counter:	machine
ALU:	control
Control Unit:	control

(b) Moore's law affects most but not all of the following aspects of a computer system. Identify those that it does not affect. Explain why.
(i) clock rate, (ii) memory size, (iii) disk size, (iv) ISA, (v) control layer details, (vi) parallel processing.
Answer: Clock rate, memory size increases because of scaling (miniaturization of transistor). ISA is affected with increases in word size and memory size, and the complexity of instructions. Control layer (implementation) of the ISA employs more parallel processing and buffering, as cost of transistors is correspondingly reduced. Disk size is not directly affected by the Moore's law but by the disk technology itself.

(c) Explain the role of a bus arbiter and the main disadvantages of daisy-chained arbitration.
Answer:
A bus arbiter is responsible to arbitrate among all competing bus masters by selecting every time a single master to use the bus (when it becomes available). Daisy-chained arbitration has two drawbacks: the acknowledge signal propagates down the chain sequentially and may take more time, and a fixed priority is assigned among the devices in the chain, potentially leaving those down the chain suffering from starvation or unresponsiveness.

(d) There are three distinct factors that affect the execution time of a program. What are they? Identify at which layers of computer abstraction these factors arise.
Answer:
(i) number of instructions executed: depends on ISA and programming/translation skills.
(ii) average number of cycles per instruction: depends on the control layer implementation details (how much parallelism and hence time needed in executing an instruction).
(iii) clock rate: depends on technology and control layer implementation (how much work needs to be done in a clock cycle).