**Instructor:** Tadeusz Obuchowicz
**Date:** Tuesday, March 1 , 2016
**Instructions:** Answer all 4 questions questions in the answer booklets provided.
**Time Allowed:** up to 2 hours.
**Materials Allowed:** Any computer organization hardcopy textbook, course lecture notes in
hardcopy format, ENCS approved electronic calculators.

**Question 0:** (in computing, we often start counting from 0 ...) [ 25 points ]

**(a)** Convert $(21.23)_4$ into its base-5 representation with up to 4 significant digits after the "base-5 decimal point".

**(b)** Convert $(57.6875)_{10}$ into its base-6 representation.

**(c)** Convert $(21)_{16}$ into its base-8 representation.

**(d)** Convert $(0.0001)_2$ into its base-4 representation.

**Question 1:** [ 25 points ]

**(a)** Give the range of integers representable using 6-bit sign-magnitude notation.

**(b)** Give the range of integers representable using 6-bit two's complement notation.

**(c)** Perform the operation:

$$
\begin{array}{rr}
 & (-16) \\
+ & (+\ 1) \\
\hline
= & -15
\end{array}
$$

using 6-bit two's complement arithmetic. Indicate whether overflow has occurred.

**(d)** Perform the operation:

$$
\begin{array}{rr}
 & -32 \\
\times & (-1) \\
\hline
= & +32
\end{array}
$$

using 6-bit two's complement multiplication following the "pencil-paper" method using sign extension.

**(e)** Convert the following IEEE 754 32-bit floating point format number into its equivalent decimal value:

0    1 0 0 0 0 0 0 0    0 1 0 0  0 0 0 0  0 0 0 0  0 0 0 0  0 0 0 0  0 0 0

**Question 2:** [ 25 points ]

Consider the hardware shown in Figure 1 consisting of a 4-bit D-type register, two 2-1 multiplexers, and a 4-bit parallel adder (with one of the adder inputs connected to the constant value of "0001") .
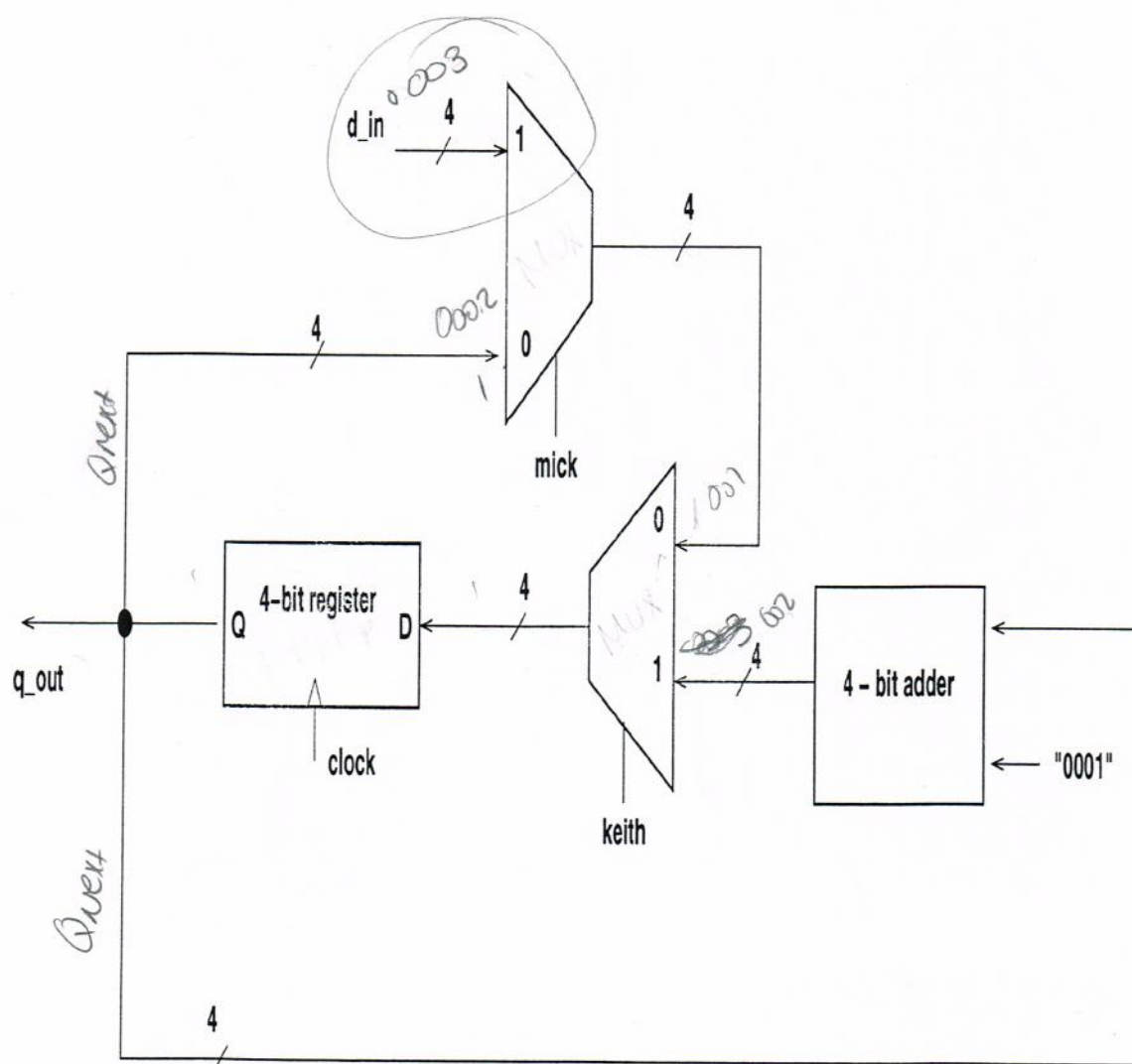


Figure 1: Two muxes, a register, and an adder.

**(a)** Complete the following table which explains the functionality of the given hardware:

**Table 1: Functional Description of hardware in Figure 1**

| keith | mick | q_out(present) | q_out(next clock) |
|---|---|---|---|
| 0 | 0 | q_out | same q_out |
| 0 | 1 | q_out | ????? |
| 1 | 0 | q_out | ????? |
| 1 | 1 | q_out | ????? |

**(b)** Explain in words the functionality of this circuit. Express your answer in a manner similar to:

*"This hardware organization is a 4-bit register capable of being loaded at the next rising clock edge with the two's complement of the value presently stored within the register when the signal keith = '1' and mick = '0', or the register may be cleared to "0000" when keith = '0' and mick = '1'."*

Of course, the hardware performs something completely different. The above is given merely as an example of how you should express your answer.

**(c)** Complete the timing diagram given on the last page of this exam. **You may remove the last page and insert it into your answer booklet. WRITE YOUR NAME AND ID NUMBER IN THE SPACE PROVIDED ON THE LAST PAGE.** You may assume 0 delay for the 4 -bit register. Indicate the value stored in the 4-bit register (qout) between the lines labelled START and END.

**Question 3:** [ 25 points ]

A digital logic circuit with output F and three inputs A,B, and C is specified with the following truth table:

**Table 2: Truth Table for Question 3**

| A | B | C | F |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 |

**Table 2: Truth Table for Question 3**

| A | B | C | F |
|---|---|---|---|
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 |

(a) Explain in words why the grouping of 1's in the following K-map is not a valid grouping.



(b) Properly minimize F using a Karnaugh map.