Youssef Zaafan Ateya

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- **Date of birth:** 11 / 09 / 2000 I **Military service status:** Performed

OBJECTIVE

- Detail-oriented Software Testing Engineer with a strong foundation in test design, execution, and defect management. Skilled in manual and automated testing, SDLC/STLC processes, and quality assurance methodologies, aiming to ensure high-quality software delivery and contribute to continuous improvement in agile, tech-driven environments.

EDUCATION

- **Electronics and communication Engineering - Higher Technological Institute 10th of Ramadan (2018-2023)**
  - Accumulative Grade**: Excellent (85.75%)**
  - Rank: **7**
  - Graduation Project Grade: **Excellent**

- **Graduation Project: Digital Design of Blowfish algorithm used in Security Systems, sponsored by Nile University (2022-2023)**
  - Developed a digital hardware implementation of the **Blowfish encryption algorithm** for security systems, incorporating a **UART communication protocol** for data exchange. Applied advanced techniques to prevent **clock domain crossing (CDC)** and reduce power consumption, including **synchronizers, clock gating,** and **clock dividers**. Conducted **white-box verification** to ensure functional correctness and implemented the final design on FPGA hardware.
    - Skills: Verilog, Python
    - Tools: Xilinx Vivado, ModelSim, Draw.io, VS Code

COURSES

- **Software Testing Bootcamp – Digital Egypt Pioneers Initiative (DEPI) (July 2025 - Present)**
  - In progress training covers software testing across the SDLC, including static testing techniques, test analysis and design, and managing test activities. Hands-on practice with test tools (Selenium, Postman) for functional and API testing. Additional modules include testing fundamentals, Java programming basics, and prompt engineering, focusing on designing and executing effective testing strategies aligned with industry standards.

- **Software Testing – Sprints X Microsoft Summer Camp (July 2025 - Present)**
  - In progress training covers software testing fundamentals (SDLC testing, static testing, test techniques, test management, tool support) and Agile testing principles, practices, methods, and tools, with hands-on experience in test case design, bug reporting, and test execution following industry standards.

- **Programming with Python – SprintUp (May 2025)**
  - Completed training in software engineering fundamentals (SDLC, design, APIs, diagrams, configuration management with Git/GitHub) and Python programming (syntax, control flow, functions, OOP, data structures, file handling, and exception handling).

- **Digital Verification Analyst Diploma (Under supervision Eng. Sherif Hosny) (Sep 2023 - Nov 2023)**
  - Studied verification fundamentals, SystemVerilog, and the Universal Verification Methodology (UVM), with practical experience in simulation tools and debugging techniques.

- **Digital IC Design Diploma (Under supervision Eng. Ali El-Temsah) (July 2022 - Sep 2022)**
  - Trained in RTL design and verification (Verilog, TCL scripting), low-power design, clock domain crossing, RTL synthesis (Design Compiler), full ASIC flow execution, DFT insertion, advanced self-checking testbench development, static timing analysis, and post-layout/formal verification.

- **Advanced Diploma: Embedded Systems - SIGN ED (July 2021- Oct 2021)**
  - Basic concepts of embedded systems, C programming, and data structures (linked list, stack, queue).

Technical Skills

- Programming & Scripting: Java, C/C++, Python, Object-Oriented Programming (OOP), TCL scripting, Bash, Cshell, Linux, Data Structures
- Software Testing: Test Techniques, Reporting Techniques
- Hardware Description Languages: Verilog, SystemVerilog, VHDL
- Embedded Systems: Basic Embedded Concepts, Microcontroller Driver Development
- Verification: Universal Verification Methodology (UVM), Formal Verification
- Tools & Platforms: Selenium, Postman, Xilinx Vivado, ModelSim, VS Code, Git & GitHub
- Project Management: Jira
- Office Tools: Microsoft Word, Excel, PowerPoint

Key Projects

- **UVM-Based Verification of Digital Peripherals**
  - Designed and implemented **UVM verification environments** for multiple digital peripherals, including combinational and sequential circuits, UART, SPI memory, I^2C memory, AXI memory, and ARB RAM. Each project was developed in a dedicated GitHub repository, featuring modular UVM components (driver, monitor, scoreboard, coverage) and applying industry-standard verification practices for functional correctness and coverage closure.

- **RTL-to-GDS Implementation of Low-Power Configurable Multi-Clock Digital System**
  - Designed and verified RTL blocks including ALU, Register File, FIFO, Clock Modules, Controller, and UART TX/RX. Performed synthesis and timing closure using Synopsys Design Compiler, followed by functional equivalence verification with Formality. Executed the complete ASIC flow to GDSII generation with post-layout validation.
    - Skills: Verilog, TCL scripting
    - Tools: VS Code, ModelSim, Synopsys Design Compiler, Formality

- **SPI Protocol Implementation in SystemVerilog**
  - Developed and verified SPI Master and Slave modules in SystemVerilog, including a self-checking testbench to validate data transmission and reception for both ends of the communication.
    - Skills: SystemVerilog
    - Tools: VS Code, ModelSim

TRAINING

- Jelecom Analog and Digital Electronics basics (Aug 2020 – Sep 2020)
- Telecom Egypt CCNA Diploma (Aug 2021 – Sep 2021)
- IBSC Security Systems (Aug 2019 – Sep 2019)

Volunteering & Student Activities

- PI Creation Robotics Club (Jan 2019 – Mar 2019)
- Instructor in PI Creation student activity (July 2019 – Nov 2019)
- DSC HTI 10th of Ramadan branch (Feb 2020 – July 2020)
- Charity Association: volunteer at Ressala (Jun 2017)

Languages:

- English: Very good at writing, reading, speaking, and listening