VHDL

3- Wave form & Simulation

VHSIC Hardware Description Language

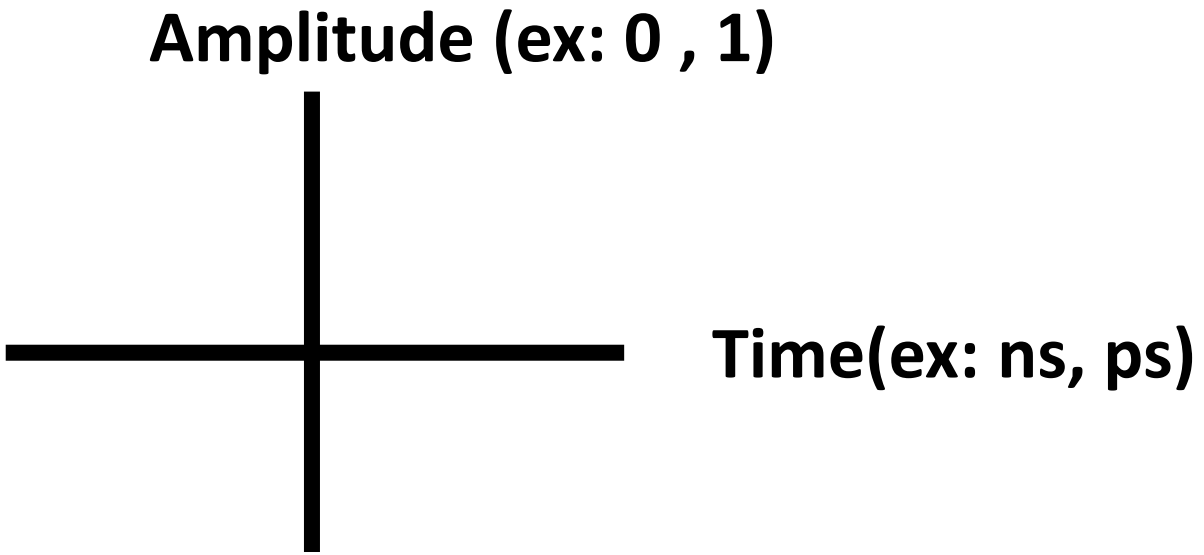
What is signal

Signals can be input or output to the system or inner signal between components of the system

What is wave form

A waveform in VHDL represents the graphical depiction of the behavior of signals over time.

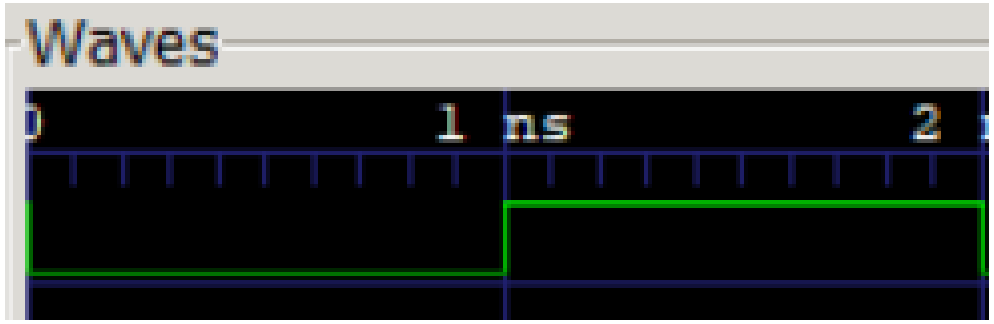
Simulation in VHDL refers to the process of digitally modeling and analyzing the behavior of a digital circuit design before its physical implementation



Bit → 0 or 1

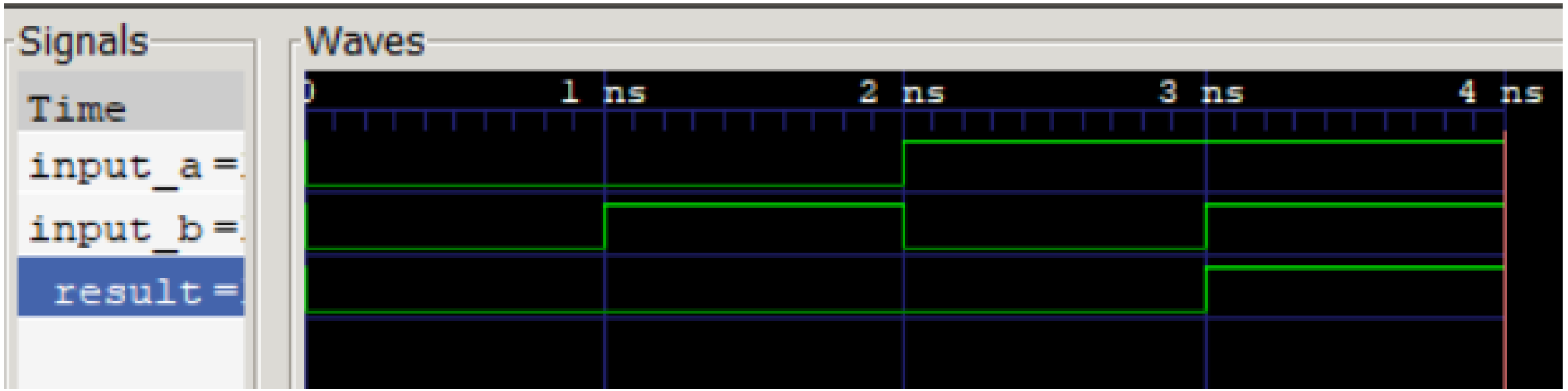
→ low or high

→ OFF or ON

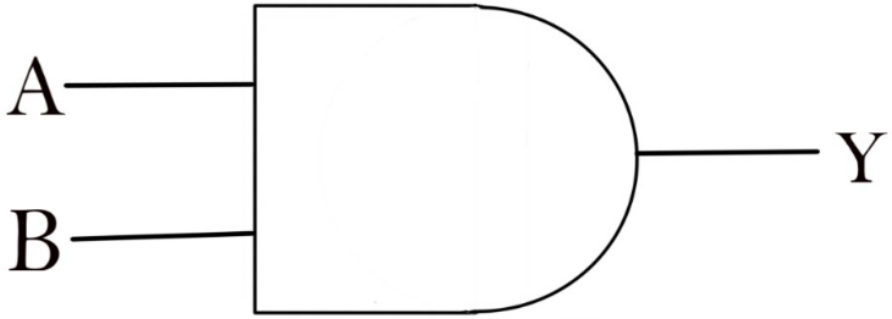


Low **High**

Can be more than one signal

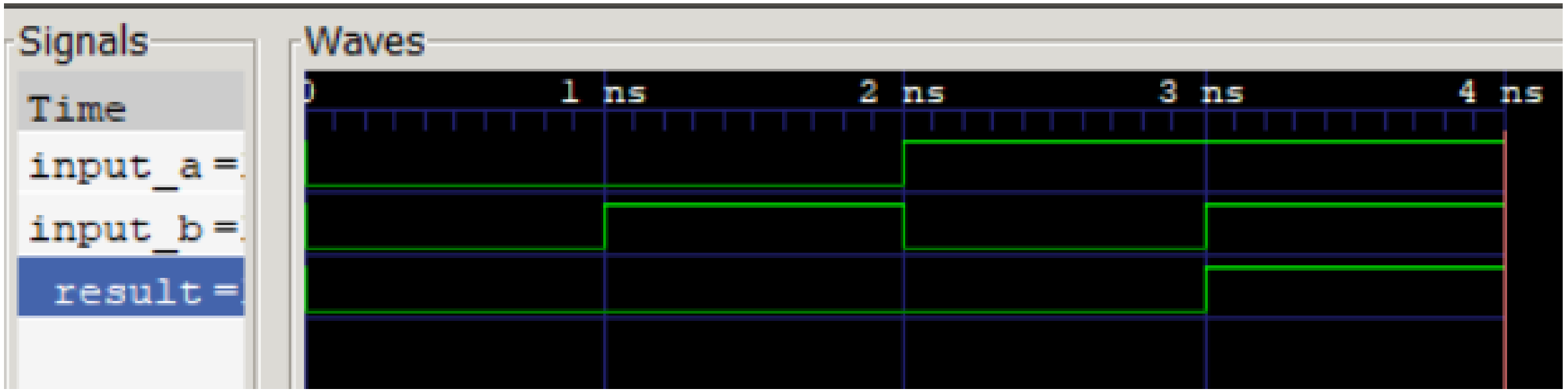


Simulation for AND



A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Simulation for AND



Thank You