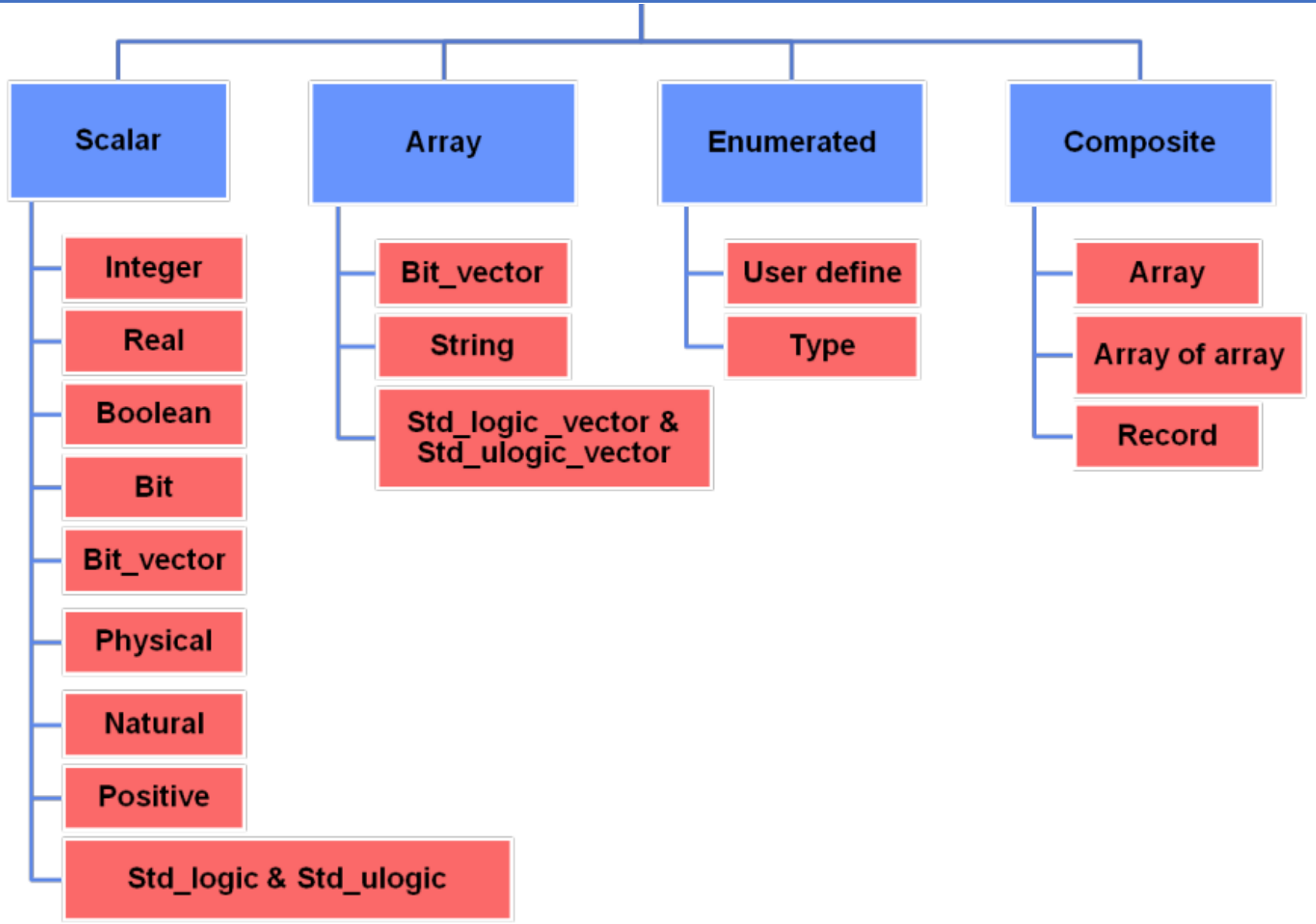
VHDL

5- Data Types

VHSIC Hardware Description Language

Data Types


Scalar
Integer
Real
Boolean
Bit
Bit_vector
Physical
Natural
Positive
Std_logic & Std_ulogic
Array
Bit_vector
String
Std_logic _vector &
Std_ulogic_vector
Enumerated
User define
Type
Composite
Array
Array of array
Record

- **BIT**

The BIT data type can only have the value 0 or 1.

written ‘0’ , ‘1’;

- **BIT_VECTOR**

The BIT_VECTOR data type is the vector version of the BIT type consisting of two or more bits.

Written “111010” , “101011”

- **STD_LOGIC**

- The STD_LOGIC data type can have the value X, 0, 1 or Z.

- X – unknown
- 0 – logic 0
- 1 – logic 1
- Z – high impedance (open circuit) / tristate buffer

written ‘0’,’1’,’Z’,’X’

- **STD_LOGIC_VECTOR**

- The vector version of the STD_LOGIC data type. Each bit in the set of bits that make up the vector can have the value X, 0, 1 or Z

  written “101” , “ZZZ” , “XXX”

- **STD_LOGIC_VECTOR**

- The vector version of the STD_LOGIC data type. Each bit in the set of bits that make up the vector can have the value X, 0, 1 or Z

  written “101” , “ZZZ” , “XXX”

- **Unsigned and signed**

- represent unsigned integers

Data Types

- boolean (true, false)

```
variable var1: boolean := false;
```

- integer (32 bit, -2,147,483,647 to +2,147,483,647

```
signal x: integer range 0 to 256 :=16;
```

- real (from -1.0e38 to +1.0e38)

```
constant pi : real := 3.14159;
```

- Physical

```
signal delay_time : time := 10 ns;  -- 10 nanoseconds
signal wire_length : length := 1.5 m;  -- 1.5 meters
```

Thank you