VHDL

2- Environment Setup

VHSIC Hardware Description Language

VHDL Introduction

- Model Sim for Simulation
- Quartus for Real Time using FPGA
- GTK wave for simulation
- GHDL
- Visual Studio Code

Test the installation

- Code to simulate logical and between 2 bits

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity and_gate is
    Port (
        input_a : in  std_logic;
        input_b : in  std_logic;
        result  : out std_logic
    );
end and_gate;

architecture Behavioral of and_gate is
begin
    result <= input_a and input_b;
end Behavioral;
```

Test the installation

- Code to simulate test bench logical and between 2 bits

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
entity and_gate_tb is
end and_gate_tb;
architecture Behavioral of and_gate_tb is
    signal input_a,input_b,result : std_logic;
    component and_gate
        port (input_a, input_b : in std_logic;
            result  : out std_logic
        );
    end component;
begin
    dut : and_gate port map (input_a ,input_b ,result );
    stimulus : process
    begin
        -- Test case 1: 1 AND 1
        input_a <= '1';
        input_b <= '1';
        wait for 10 ns;
        -- Test case 2: 1 AND 0
        input_a <= '1';
        input_b <= '0';
        wait for 10 ns;
        wait;
    end process stimulus;
end Behavioral;
```