VHDL

7- Entity & Architecture

VHSIC Hardware Description Language

- **Entity:** This wrapper effectively describes how the black box interfaces with the outside world

```
entity my_entity is
    port(
    a : in std_logic ;
    b : in std_logic;
    y : out std_logic ); --do not forget the semicolon
end my_entity; -- do not forget this semicolon either
```

- **Architecture:** Explain how the black box work, what are the function that the black box do

```
-- Architecture definition
architecture arch_name of my_entity is
    begin
        -- Behavior description (logical AND operation)
        y <= a and b;
    end architecture arch_name;
```

Thank You