VHDL

4- Introduction into Basic Syntax

VHSIC Hardware Description Language

- VHDL is a Case insensitive

```
a : in bit;
A : in bit;
```

```
LIBRARY IEEE;
USE IEEE.STD_LOGIC_1164.ALL;
```

- VHDL is not sensitive to white space

```
library ieee;
use ieee.std_logic_1164.all;
```

```
    library          ieee;
     use      ieee.std_logic_1164.all;
```

- VHDL is a Case insensitive
- VHDL is not sensitive to white space

- **Comments**

```
-- write comment here
```

- **Reserved Words**

Listing 2.7: A short list of VHDL reserved words.

access	after	alias	all	attribute	block
body	buffer	bus	constant	exit	file
for	function	generic	group	in	is
label	loop	mod	new	next	null
of	on	open	out	range	rem
return	signal	shared	then	to	type
until	use	variable	wait	while	with

Thank You