2021 Digital IC Design

Homework 1: 4-bit Ripple Carry Adder

1. Introduction:

The ripple carry adder (RCA) circuit can be built using a cascade architecture of 1-bit full-adders. As a result, a 4-bit RCA comprises four 1-bit full-adders, which is shown in Fig. 1. In addition, a full-adder can also be constructed by two half-adders and one OR gate. Assume that *x* and *y* are 1-bit input signals and *s* and *c* are outputs standing for *sum* and *carry*. The computation of the half adder can be represented as equation (1). Fig. 2 illustrates the architecture of a half adder and a full adder. In this homework, please design a 4-bit ripple carry adder according to Fig. 1. You are suggested to design the circuit using hierarchy modules including series of half adders and full adders. The values are considered as unsigned integers.

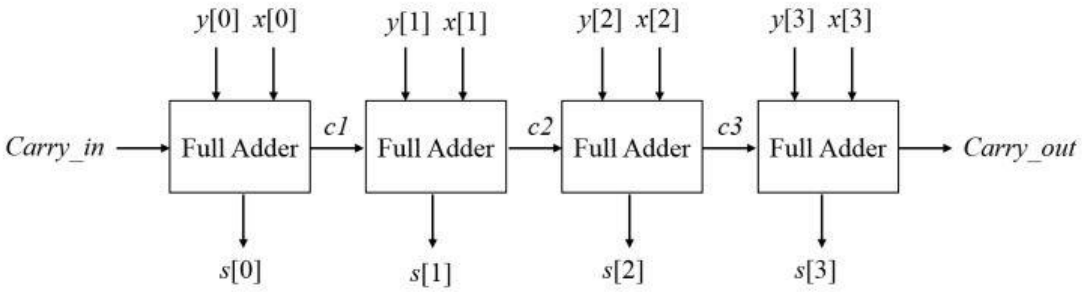

Fig. 1. The architecture of a 4-bit ripple carry adder.

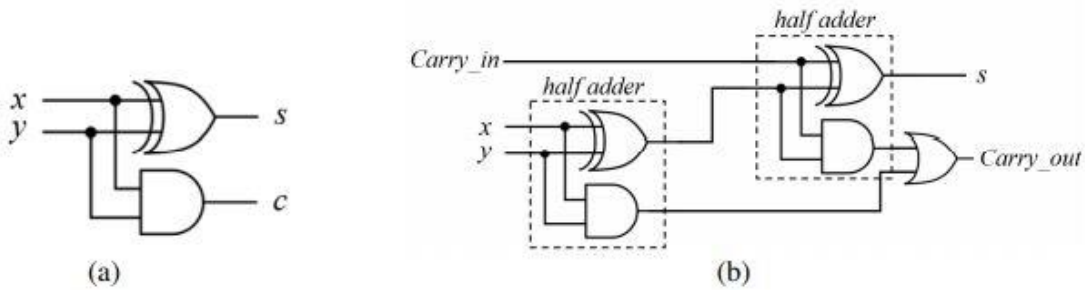

Fig. 2. The architecture of (a) an half-adder and (b) a full adder.

$$s = x \oplus y$$
$$c = x \cdot y \quad \textbf{(1)}$$

2. Design Specifications:

2.1 Block Overview

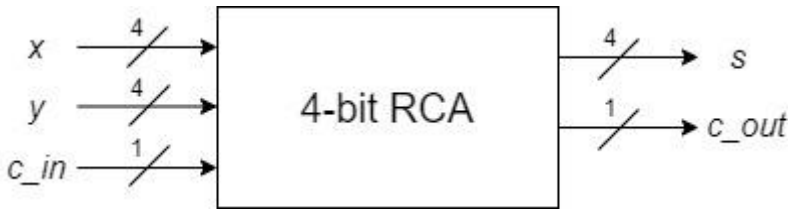

Fig. 3. The block overview.

2.2 I/O Interface

Signal Name	I/O	width	Description
x	I	4	augend
y	I	4	summand
c_in	I	1	carry in
s	O	4	sum
c_out	O	1	carry out

2.3 File Description

File Name	Description
HA.v	The module of half-adder.
FA.v	The module of full adder.
RCA.v	The module of ripple carry adder, which is the top module in this design.
RCA_tb.v	The testbench file. The content in this file is **not allowed** to be modified.

3. Scoring:

3.1 Functional Simulation **[70%]**

All of the result should be generated correctly, and you will get the following message in ModelSim simulation.

```
#          496 data is correct
#          497 data is correct
#          498 data is correct
#          499 data is correct
#          500 data is correct
#          501 data is correct
#          502 data is correct
#          503 data is correct
#          504 data is correct
#          505 data is correct
#          506 data is correct
#          507 data is correct
#          508 data is correct
#          509 data is correct
#          510 data is correct
#          511 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
```

Fig. 4. Functional simulation result.

3.2 Gate-Level Simulation **[30%]**

3.2.1 Synthesis

Your code should be synthesizable. After it is synthesized in Quartus, a file named *RCA.vo* will be obtained.

3.2.2 Simulation

All of the result should be generated correctly using RCA.vo, and you will get the following message in ModelSim simulation.

```
#          504 data is correct
#          505 data is correct
#          506 data is correct
#          507 data is correct
#          508 data is correct
#          509 data is correct
#          510 data is correct
#          511 data is correct
# --------------------PASS--------------------
# All data have been generated successfully!
```

Fig. 5. Gate-level simulation result.

Device：**Cyclone II EP2C70F896C8**

4. Submission:

4.1 Submitted files

You should classify your files into three directories and compress them to .zip format. The naming rule is HW1_studentID_name.zip. If your file is not named according to the naming rule, you will lose five points.

	RTL category
*.v	All of your Verilog RTL code
	Gate-Level category
*.vo	Gate-Level netlist generated by Quartus
*.sdo	Gate-Level netlist generated by Quartus
	Documentary category
*.pdf	The report file of your design (in pdf).

4.2 Report file

Please follow the spec of report. You are asked to describe how the circuit is designed as detailed as possible, and the flow summary result is necessary in the report.

Flow Summary	
Flow Status	Successful - Mon Mar 22 14:57:10 2021
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	RCA
Top-level Entity Name	RCA
Family	Cyclone II
Device	EP2C70F896C8
Timing Models	Final
Total logic elements	10 / 68,416 (< 1 %)
Total combinational functions	10 / 68,416 (< 1 %)
Dedicated logic registers	0 / 68,416 (0 %)
Total registers	0
Total pins	14 / 622 (2 %)
Total virtual pins	0
Total memory bits	0 / 1,152,000 (0 %)
Embedded Multiplier 9-bit elements	0 / 300 (0 %)
Total PLLs	0 / 4 (0 %)

Fig. 6. The flow summary.

4.3 Note

Please submit your .zip file to folder HW1 in moodle.

Deadline: 2021/4/12 23:55

If you have any problem, please contact TA by email

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