2021 Digital IC Design Homework 1

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| NAME | | 蔣有為 | | | | | | |
| Student ID | | P76104231 | | | | | | |
| **Simulation Result** | | | | | | | | |
| Functional simulation | Pass | | Gate-level simulation | | | Pass | Gate-level simulation time | 102500 ns |
|  | | | | | (your post-sim result) | | | |
| **Synthesis Result** | | | | | | | | |
| Total logic elements | | | | 10 / 68,416 ( < 1 % ) | | | | |
| Total memory bit | | | | 0 / 1,152,000 ( 0 % ) | | | | |
| Embedded multiplier 9-bit element | | | | 0 / 300 ( 0 % ) | | | | |
| Clock Width (Cycle) | | | | 10 | | | | |
|  | | | | | | | | |
| **Description of your design** | | | | | | | | |
| 1. Half Adder   A half-adder is combined with one XOR gate and one And gate for designing.  In this part, it only has two input about x, y and two output about s, c.   1. Full Adder   I used two Half Adder for components and with a OR gate to combine the Full Adder. In this part, it has two more port ( carry\_in, and carry\_out ).   1. Ripple Adder 2. It is a 4-bit RCA, so it needs 4 times to calculate each bit. In this part, it combines 4 Full Adder, each one will use one bit. Carry\_in is for the starting port ,after its calculation it will propagate for next adder’s carry\_in, and so on.   Finally, it will produce 4-bit Ripple Adder. | | | | | | | | |