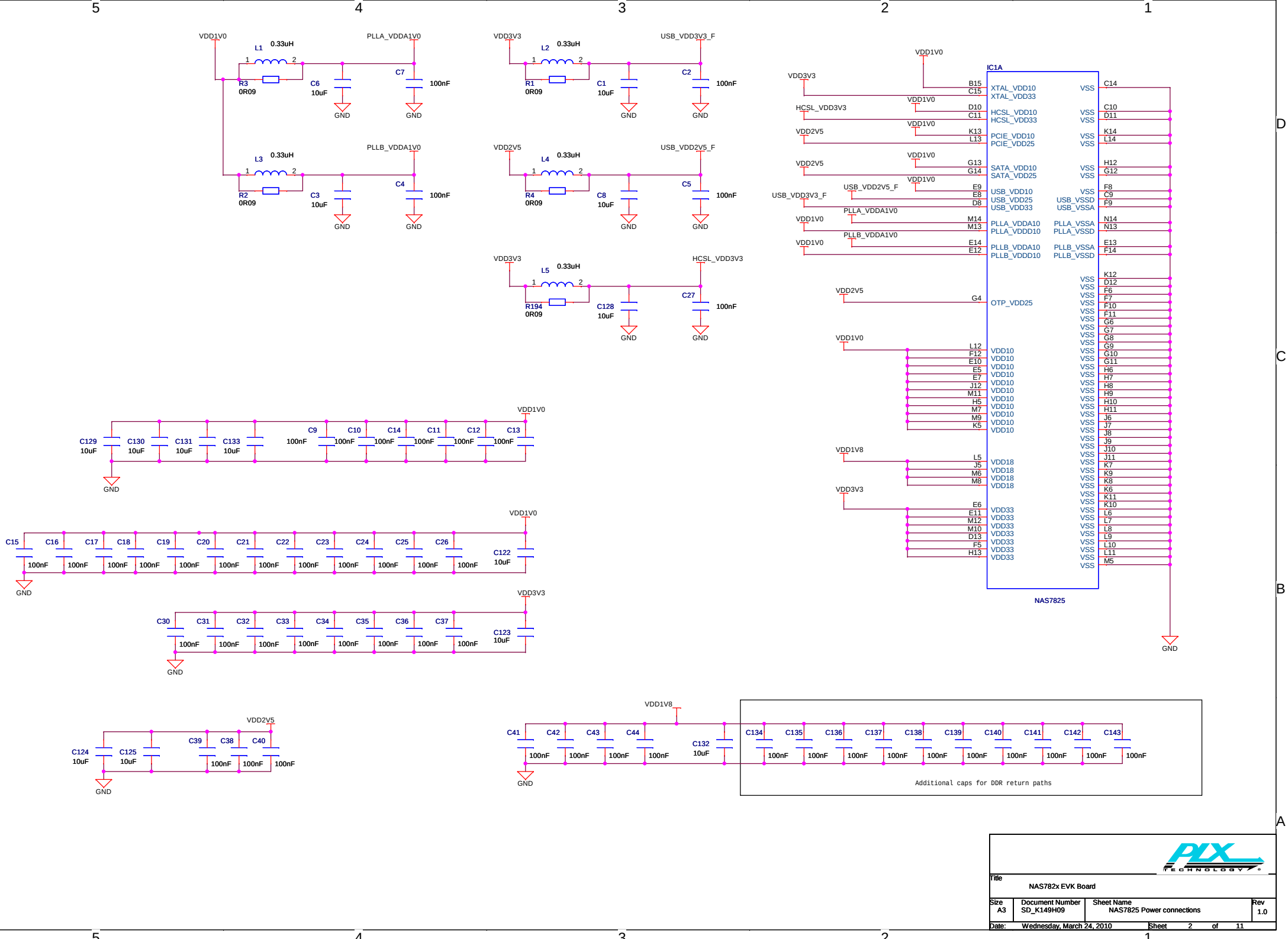
# NAS782x EVK Board

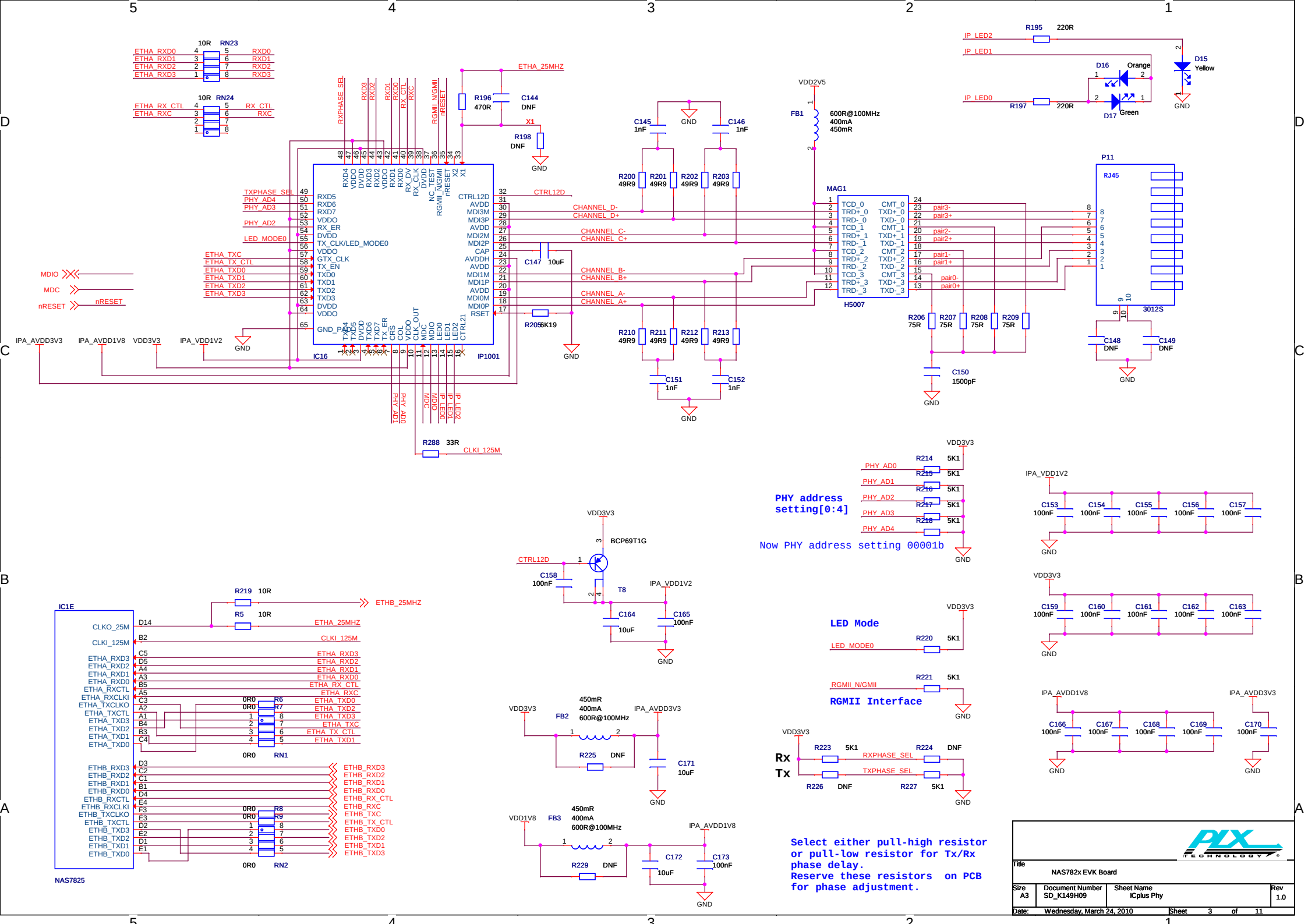
# Doc No: SD_K149H09

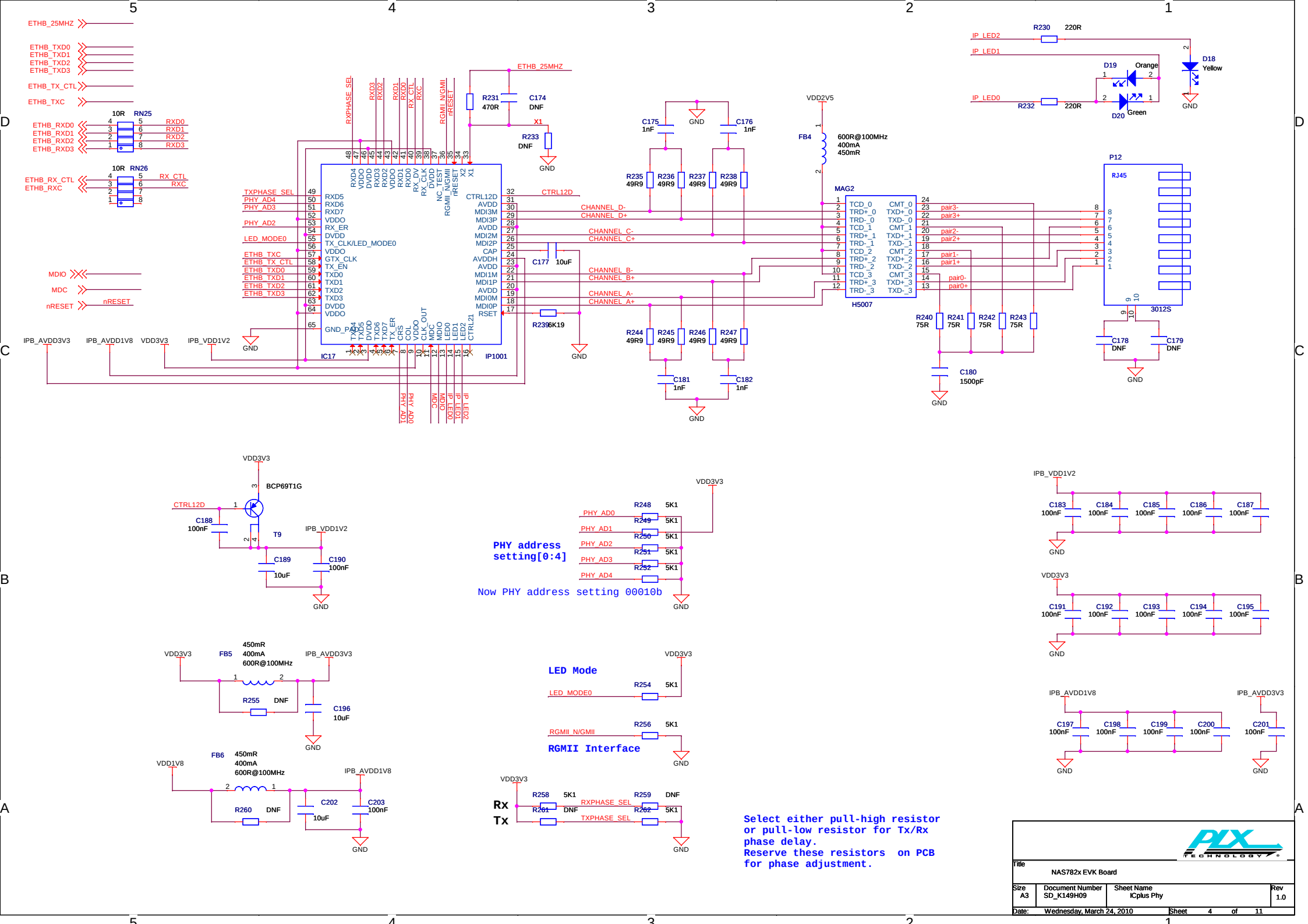
| Overall Revision: | 1.0 | 1.1 | 1.2 |
|---|---|---|---|
| Sheet Number \| Rev'n | | | |
| 2 | 1.0 | 1.0 | 1.0 |
| 3 | 1.0 | 1.0 | 1.0 |
| 4 | 1.0 | 1.0 | 1.0 |
| 5 | 1.0 | 1.0 | 1.0 |
| 6 | 1.0 | 1.0 | 1.0 |
| 7 | 1.0 | 1.0 | 1.0 |
| 8 | 1.0 | 1.1 | 1.2 |
| 9 | 1.0 | 1.1 | 1.1 |
| 10 | 1.0 | 1.0 | 1.0 |
| 11 | 1.0 | 1.0 | 1.0 |
| 12 | 1.0 | 1.0 | 1.0 |

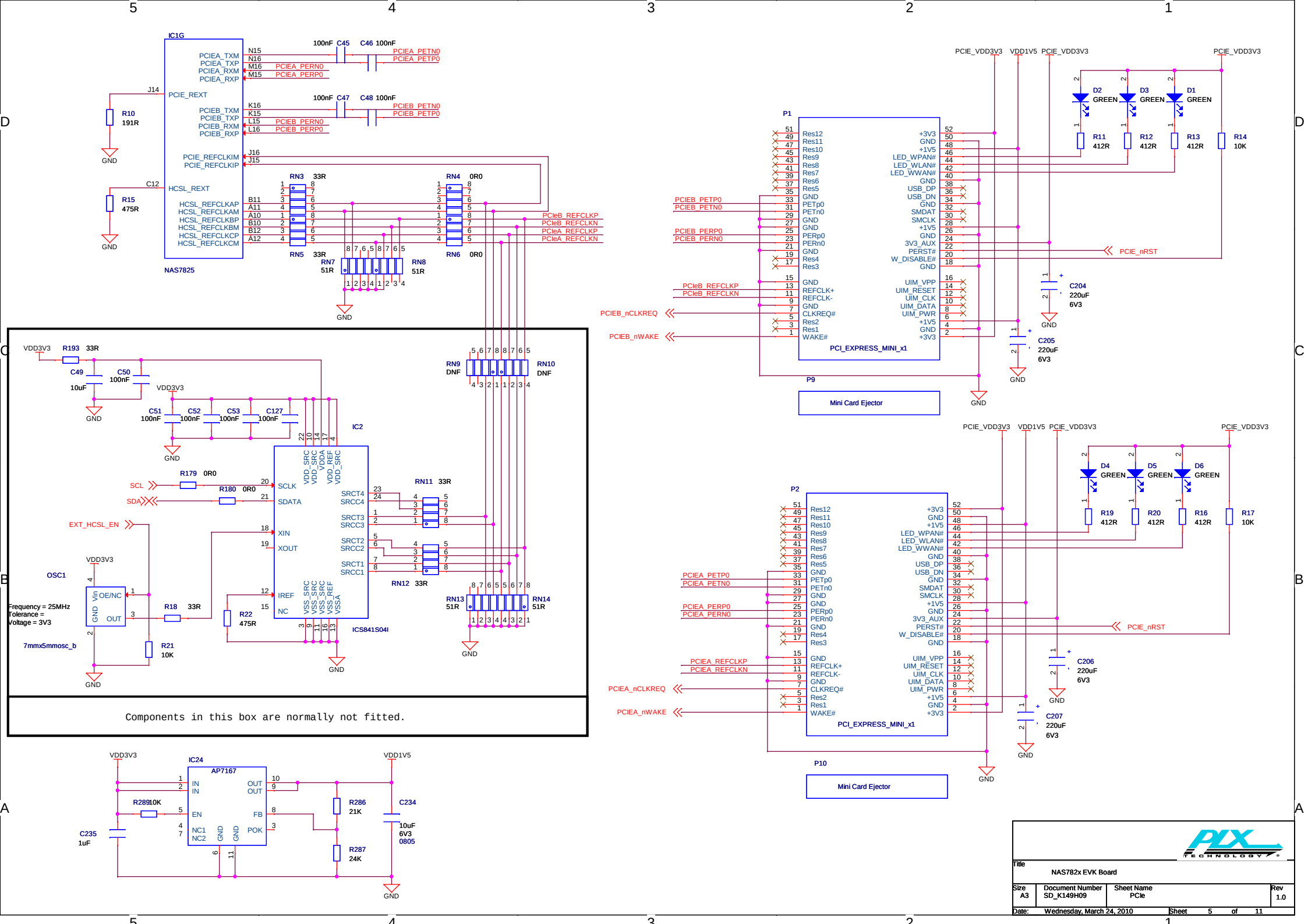
| | | | |
|---|---|---|---|
| Title: NAS782x EVK Board | | | |
| Size: A3 | Document Number: SD_K149H09 | Sheet Name: Front Page | Rev: 1.2 |
| Date: Wednesday, March 24, 2010 | Sheet 1 of 11 | | |

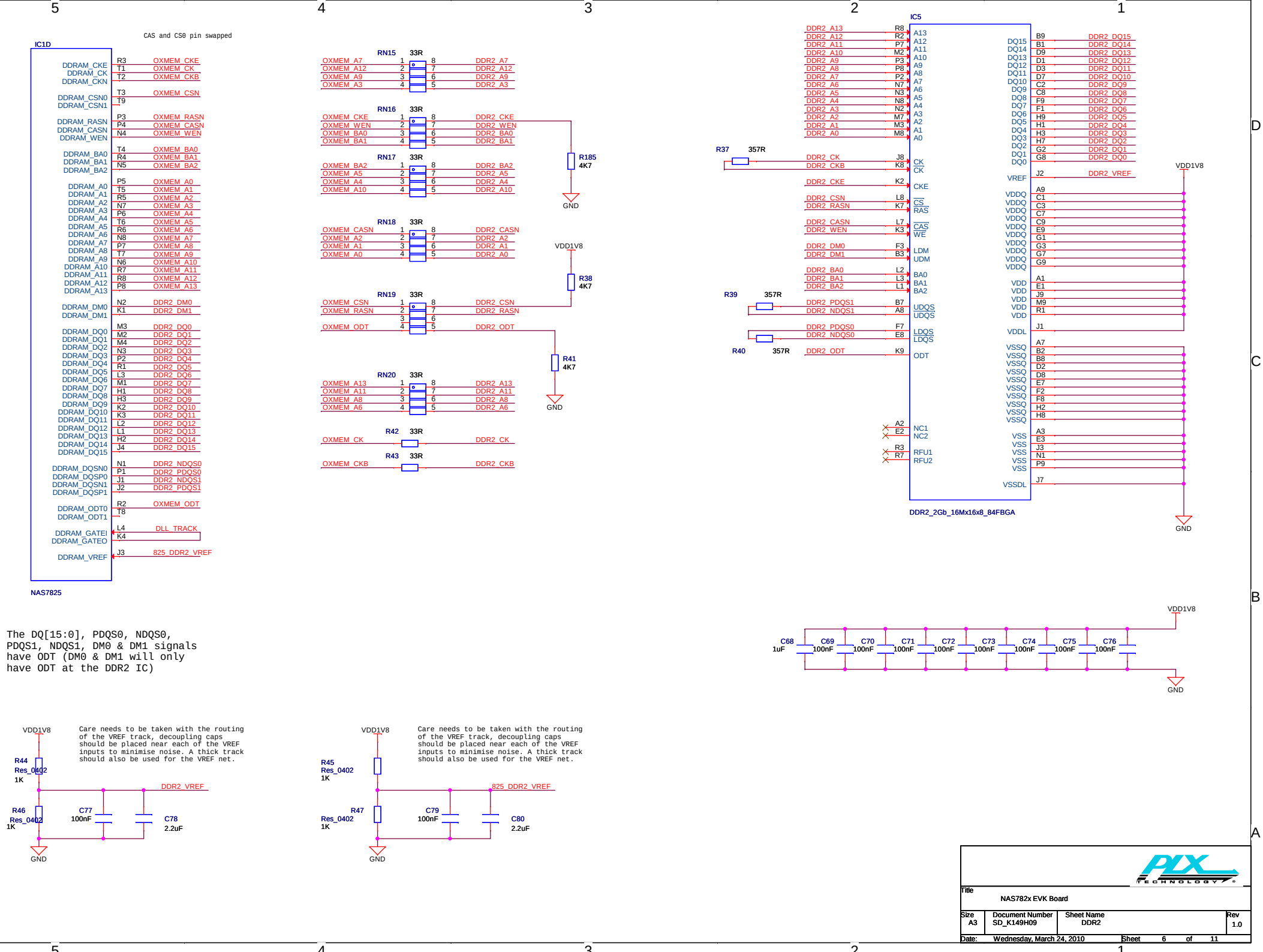


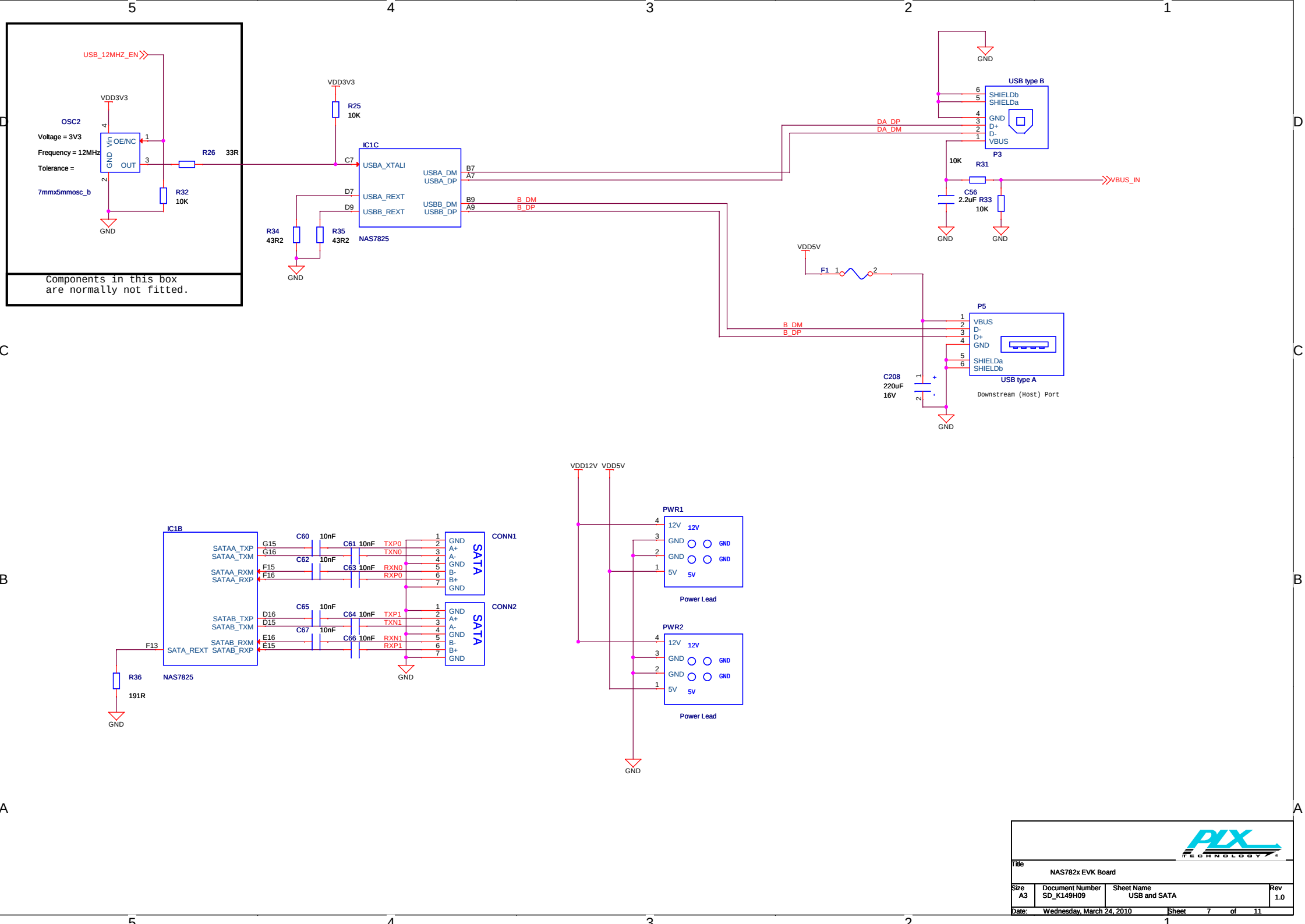

| | |
|---|---|
| Title | NAS782x EVK Board |
| Size | A3 |
| Document Number | SD_K149H09 |
| Sheet Name | NAS7825 Power connections |
| Rev | 1.0 |
| Date: | Wednesday, March 24, 2010 |
| Sheet | 2 of 11 |


RN23 10R
ETHA_RXD0
ETHA_RXD1
ETHA_RXD2
ETHA_RXD3
RXD0
RXD1
RXD2
RXD3
RN24 10R
ETHA_RX_CTL
ETHA_RXC
RX_CTL
RXC
ETHA_25MHZ
R196 470R
C144 DNF
X1
R198 DNF
GND
RXPHASE_SEL
RGMII_N/GMII
nRESET
IC16
IP1001
TXPHASE_SEL
PHY_AD4
PHY_AD3
PHY_AD2
LED_MODE0
ETHA_TXC
ETHA_TX_CTL
ETHA_TXD0
ETHA_TXD1
ETHA_TXD2
ETHA_TXD3
MDIO
MDC
nRESET
IPA_AVDD3V3
IPA_AVDD1V8
VDD3V3
IPA_VDD1V2
CTRL12D
CHANNEL_D-
CHANNEL_D+
CHANNEL_C-
CHANNEL_C+
CHANNEL_B-
CHANNEL_B+
CHANNEL_A-
CHANNEL_A+
C145 1nF
C146 1nF
C147 10uF
R205 6K19
R200 49R9
R201 49R9
R202 49R9
R203 49R9
R210 49R9
R211 49R9
R212 49R9
R213 49R9
C151 1nF
C152 1nF
R288 33R
CLKI_125M
VDD2V5
FB1 600R@100MHz 400mA 450mR
MAG1
H5007
R195 220R
IP_LED2
IP_LED1
IP_LED0
D16 Orange
D17 Green
D15 Yellow
R197 220R
P11
RJ45
3012S
pair3-
pair3+
pair2-
pair2+
pair1-
pair1+
pair0-
pair0+
R206 75R
R207 75R
R208 75R
R209 75R
C148 DNF
C149 DNF
C150 1500pF
PHY address setting[0:4]
Now PHY address setting 00001b
R214 5K1
R215 5K1
R216 5K1
R217 5K1
R218 5K1
PHY_AD0
PHY_AD1
PHY_AD2
PHY_AD3
PHY_AD4
IPA_VDD1V2
C153 100nF
C154 100nF
C155 100nF
C156 100nF
C157 100nF
C158 100nF
BCP69T1G
T8
C164 10uF
C165 100nF
C159 100nF
C160 100nF
C161 100nF
C162 100nF
C163 100nF
LED Mode
LED_MODE0
R220 5K1
RGMII_N/GMII
R221 5K1
RGMII Interface
Rx
Tx
R223 5K1
R224 DNF
R226 DNF
R227 5K1
RXPHASE_SEL
TXPHASE_SEL
IPA_AVDD1V8
IPA_AVDD3V3
C166 100nF
C167 100nF
C168 100nF
C169 100nF
C170 100nF
IC1E
NAS7825
R219 10R
R5 10R
ETHB_25MHZ
CLKO_25M
CLKI_125M
ETHA_RXD3
ETHA_RXD2
ETHA_RXD1
ETHA_RXD0
ETHA_RX_CTL
ETHA_RXC
ETHA_RXCLKI
ETHA_TXCLKO
ETHA_TXCTL
ETHA_TXD3
ETHA_TXD2
ETHA_TXD1
ETHA_TXD0
R6 0R0
R7 0R0
RN1 0R0
ETHB_RXD3
ETHB_RXD2
ETHB_RXD1
ETHB_RXD0
ETHB_RX_CTL
ETHB_RXC
ETHB_TXC
ETHB_TX_CTL
ETHB_TXD0
ETHB_TXD2
ETHB_TXD1
ETHB_TXD3
R8 0R0
R9 0R0
RN2 0R0
FB2 450mR 400mA 600R@100MHz
R225 DNF
C171 10uF
FB3 450mR 400mA 600R@100MHz
R229 DNF
C172 10uF
C173 100nF
Select either pull-high resistor or pull-low resistor for Tx/Rx phase delay.
Reserve these resistors on PCB for phase adjustment.
PLX TECHNOLOGY
Title
NAS782x EVK Board
Size A3
Document Number SD_K149H09
Sheet Name ICplus Phy
Rev 1.0
Date: Wednesday, March 24, 2010
Sheet 3 of 11

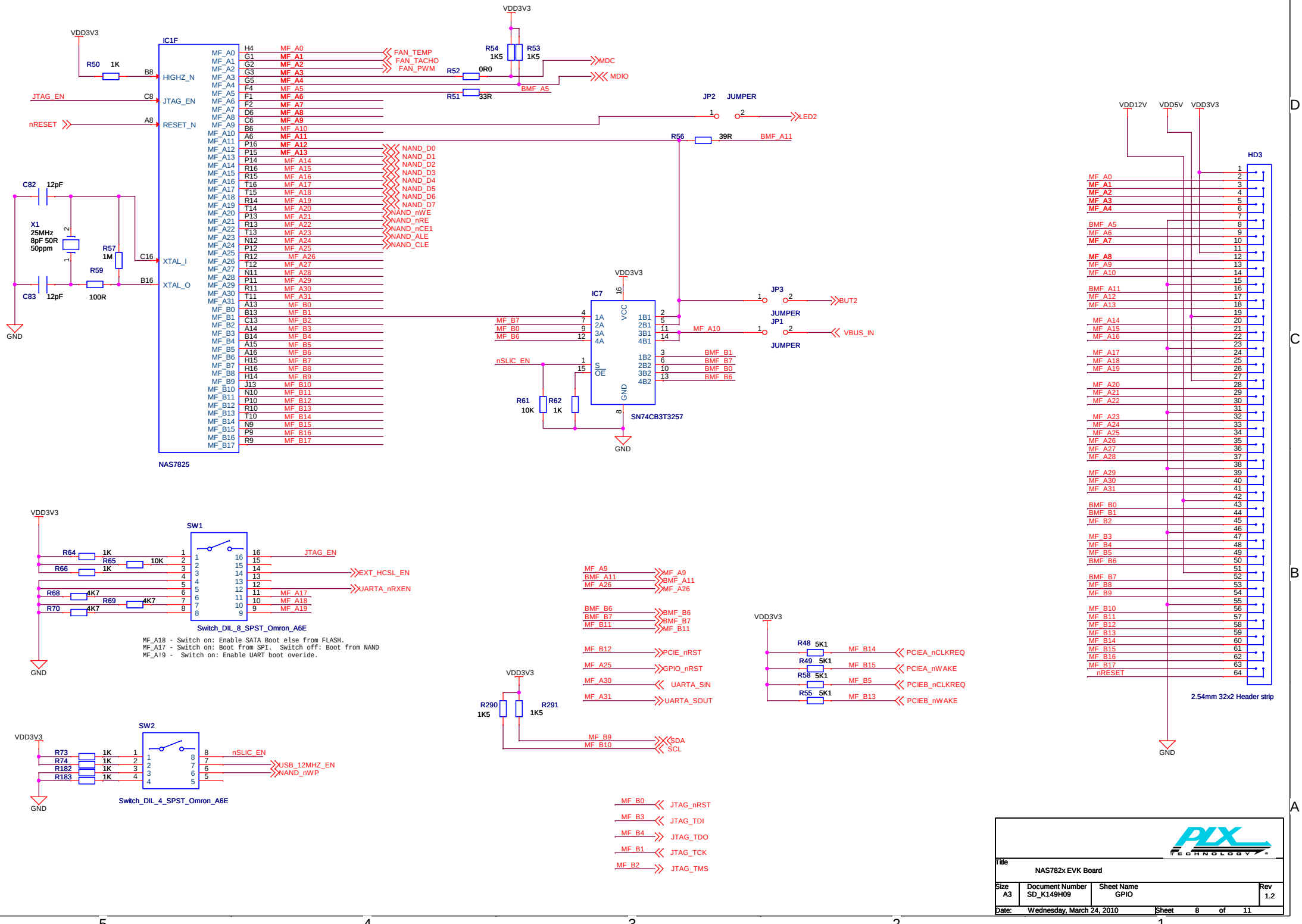

ETHB_25MHZ
ETHB_TXD0
ETHB_TXD1
ETHB_TXD2
ETHB_TXD3
ETHB_TX_CTL
ETHB_TXC
ETHB_RXD0
ETHB_RXD1
ETHB_RXD2
ETHB_RXD3
ETHB_RX_CTL
ETHB_RXC
MDIO
MDC
nRESET
RN25
RN26
IC17
IP1001
R231 470R
C174 DNF
X1
R233 DNF
C175 1nF
C176 1nF
C177 10uF
R239 6K19
R235 49R9
R236 49R9
R237 49R9
R238 49R9
R244 49R9
R245 49R9
R246 49R9
R247 49R9
C181 1nF
C182 1nF
VDD2V5
FB4 600R@100MHz 400mA 450mR
MAG2
H5007
R240 75R
R241 75R
R242 75R
R243 75R
C180 1500pF
P12
RJ45
3012S
C178 DNF
C179 DNF
R230 220R
R232 220R
D18 Yellow
D19 Orange
D20 Green
IP_LED2
IP_LED1
IP_LED0
IPB_AVDD3V3
IPB_AVDD1V8
VDD3V3
IPB_VDD1V2
GND
BCP69T1G
T9
C188 100nF
C189 10uF
C190 100nF
PHY address setting[0:4]
R248 5K1
R249 5K1
R250 5K1
R251 5K1
R252 5K1
Now PHY address setting 00010b
FB5 450mR 400mA 600R@100MHz
R255 DNF
C196 10uF
FB6 450mR 400mA 600R@100MHz
R260 DNF
C202 10uF
C203 100nF
LED Mode
R254 5K1
R256 5K1
RGMII Interface
Rx
Tx
R258 5K1
R261 DNF
R259 DNF
R262 5K1
RXPHASE_SEL
TXPHASE_SEL
Select either pull-high resistor or pull-low resistor for Tx/Rx phase delay.
Reserve these resistors on PCB for phase adjustment.
C183 100nF
C184 100nF
C185 100nF
C186 100nF
C187 100nF
C191 100nF
C192 100nF
C193 100nF
C194 100nF
C195 100nF
C197 100nF
C198 100nF
C199 100nF
C200 100nF
C201 100nF
Title
NAS782x EVK Board
Size A3
Document Number SD_K149H09
Sheet Name ICplus Phy
Rev 1.0
Date: Wednesday, March 24, 2010
Sheet 4 of 11


IC1G
NAS7825
PCIEA_TXM
PCIEA_TXP
PCIEA_RXM
PCIEA_RXP
PCIE_REXT
PCIEB_TXM
PCIEB_TXP
PCIEB_RXM
PCIEB_RXP
PCIE_REFCLKIM
PCIE_REFCLKIP
HCSL_REXT
HCSL_REFCLKAP
HCSL_REFCLKAM
HCSL_REFCLKBP
HCSL_REFCLKBM
HCSL_REFCLKCP
HCSL_REFCLKCM
PCIEA_PETN0
PCIEA_PETP0
PCIEA_PERN0
PCIEA_PERP0
PCIEB_PETN0
PCIEB_PETP0
PCIEB_PERN0
PCIEB_PERP0
R10 191R
R15 475R
C45 100nF
C46 100nF
C47 100nF
C48 100nF
RN3 33R
RN4 0R0
RN5 33R
RN6 0R0
RN7 51R
RN8 51R
PCIeB_REFCLKP
PCIeB_REFCLKN
PCIeA_REFCLKP
PCIeA_REFCLKN
GND
P1
PCI_EXPRESS_MINI_x1
P9
Mini Card Ejector
PCIE_VDD3V3
VDD1V5
D1 GREEN
D2 GREEN
D3 GREEN
R11 412R
R12 412R
R13 412R
R14 10K
C204 220uF 6V3
C205 220uF 6V3
PCIE_nRST
PCIEB_nCLKREQ
PCIEB_nWAKE
IC2
ICS841S04I
VDD3V3
R193 33R
C49 10uF
C50 100nF
C51 100nF
C52 100nF
C53 100nF
C127 100nF
R179 0R0
R180 0R0
SCL
SDA
EXT_HCSL_EN
OSC1
7mmx5mmosc_b
Frequency = 25MHz
Tolerance =
Voltage = 3V3
R18 33R
R21 10K
R22 475R
RN9 DNF
RN10 DNF
RN11 33R
RN12 33R
RN13 51R
RN14 51R
Components in this box are normally not fitted.
P2
P10
D4 GREEN
D5 GREEN
D6 GREEN
R19 412R
R20 412R
R16 412R
R17 10K
C206 220uF 6V3
C207 220uF 6V3
PCIEA_nCLKREQ
PCIEA_nWAKE
IC24
AP7167
R289 10K
R286 21K
R287 24K
C234 10uF 6V3 0805
C235 1uF
Title
NAS782x EVK Board
Size A3
Document Number SD_K149H09
Sheet Name PCIe
Rev 1.0
Date: Wednesday, March 24, 2010
Sheet 5 of 11

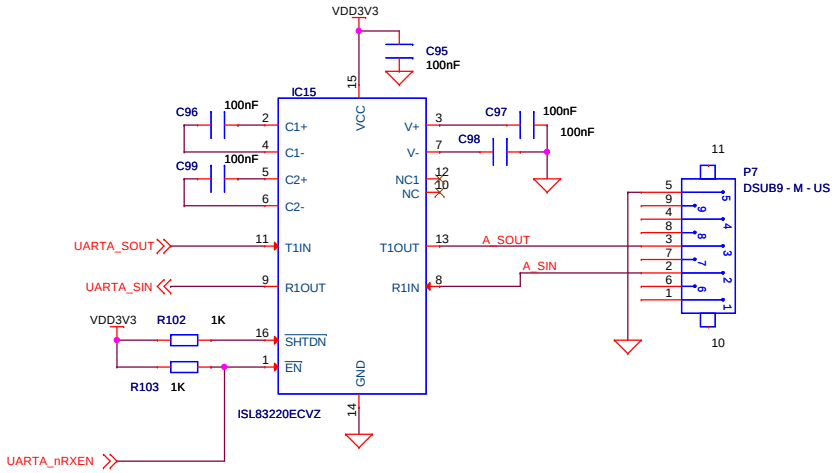

CAS and CS0 pin swapped
IC1D
NAS7825
RN15 33R
RN16 33R
RN17 33R
RN18 33R
RN19 33R
RN20 33R
R42 33R
R43 33R
R185 4K7
R38 4K7
R41 4K7
VDD1V8
GND
IC5
DDR2_2Gb_16Mx16x8_84FBGA
R37 357R
R39 357R
R40 357R
The DQ[15:0], PDQS0, NDQS0, PDQS1, NDQS1, DM0 & DM1 signals have ODT (DM0 & DM1 will only have ODT at the DDR2 IC)
C68 1uF
C69 100nF
C70 100nF
C71 100nF
C72 100nF
C73 100nF
C74 100nF
C75 100nF
C76 100nF
R44 Res_0402 1K
R46 Res_0402 1K
C77 100nF
C78 2.2uF
R45 Res_0402 1K
R47 Res_0402 1K
C79 100nF
C80 2.2uF
Care needs to be taken with the routing of the VREF track, decoupling caps should be placed near each of the VREF inputs to minimise noise. A thick track should also be used for the VREF net.
DDR2_VREF
825_DDR2_VREF
Title
NAS782x EVK Board
Size A3
Document Number SD_K149H09
Sheet Name DDR2
Rev 1.0
Date: Wednesday, March 24, 2010
Sheet 6 of 11

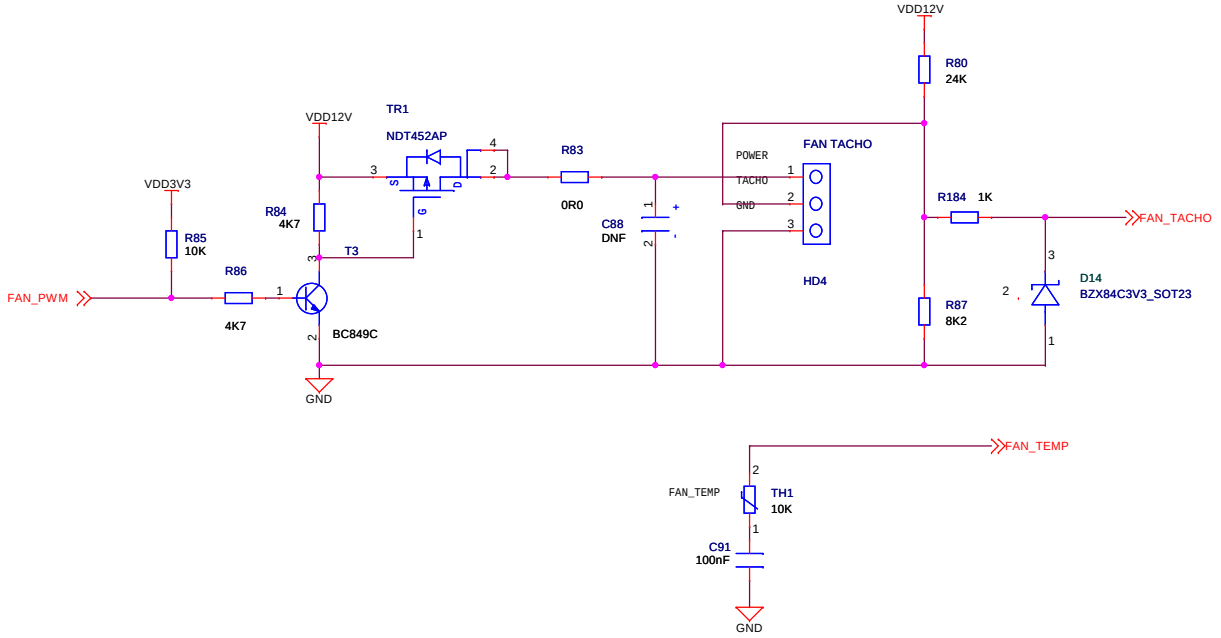


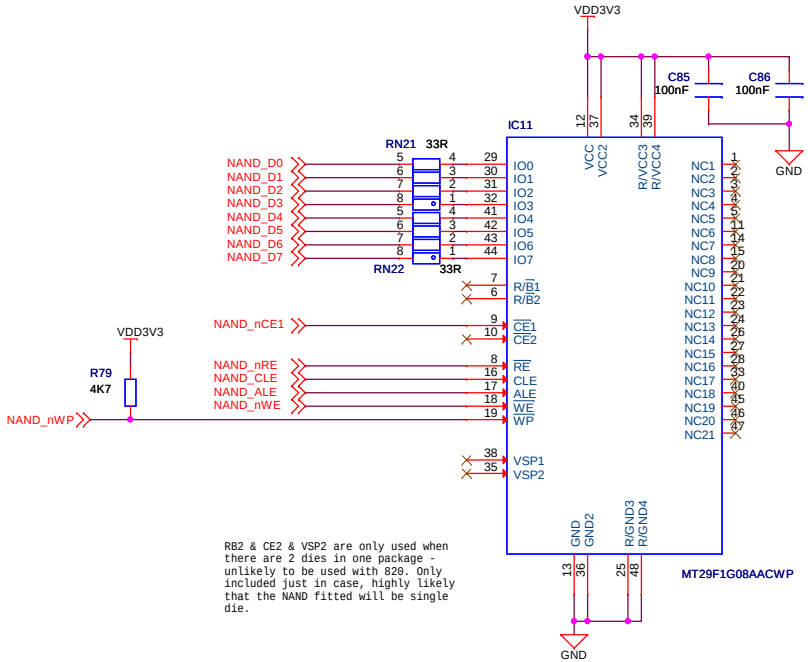

| | | | |
|---|---|---|---|
| Title | NAS782x EVK Board | | |
| Size A3 | Document Number SD_K149H09 | Sheet Name USB and SATA | Rev 1.0 |
| Date: Wednesday, March 24, 2010 | Sheet 7 of 11 | | |

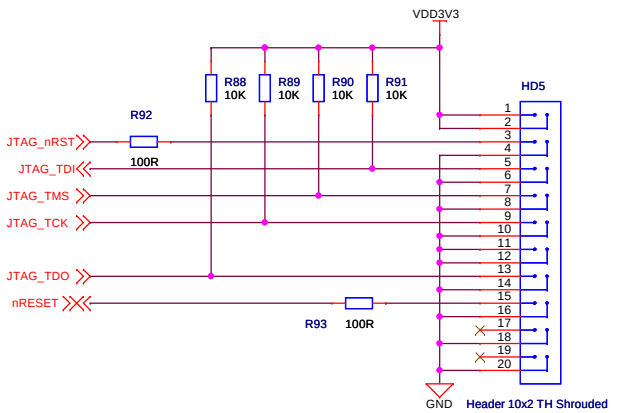


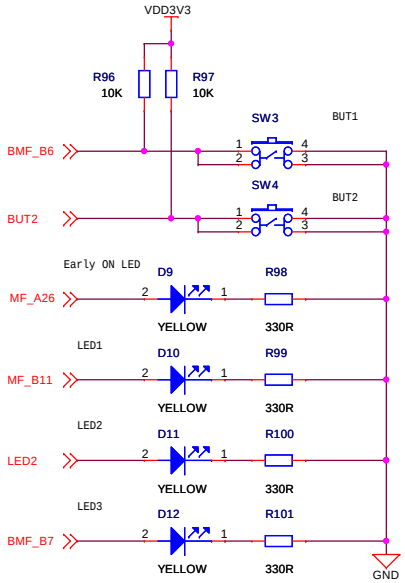

| | | | |
|---|---|---|---|
| Title | NAS782x EVK Board | | |
| Size A3 | Document Number SD_K149H09 | Sheet Name GPIO | Rev 1.2 |
| Date: Wednesday, March 24, 2010 | | Sheet 8 of 11 | |



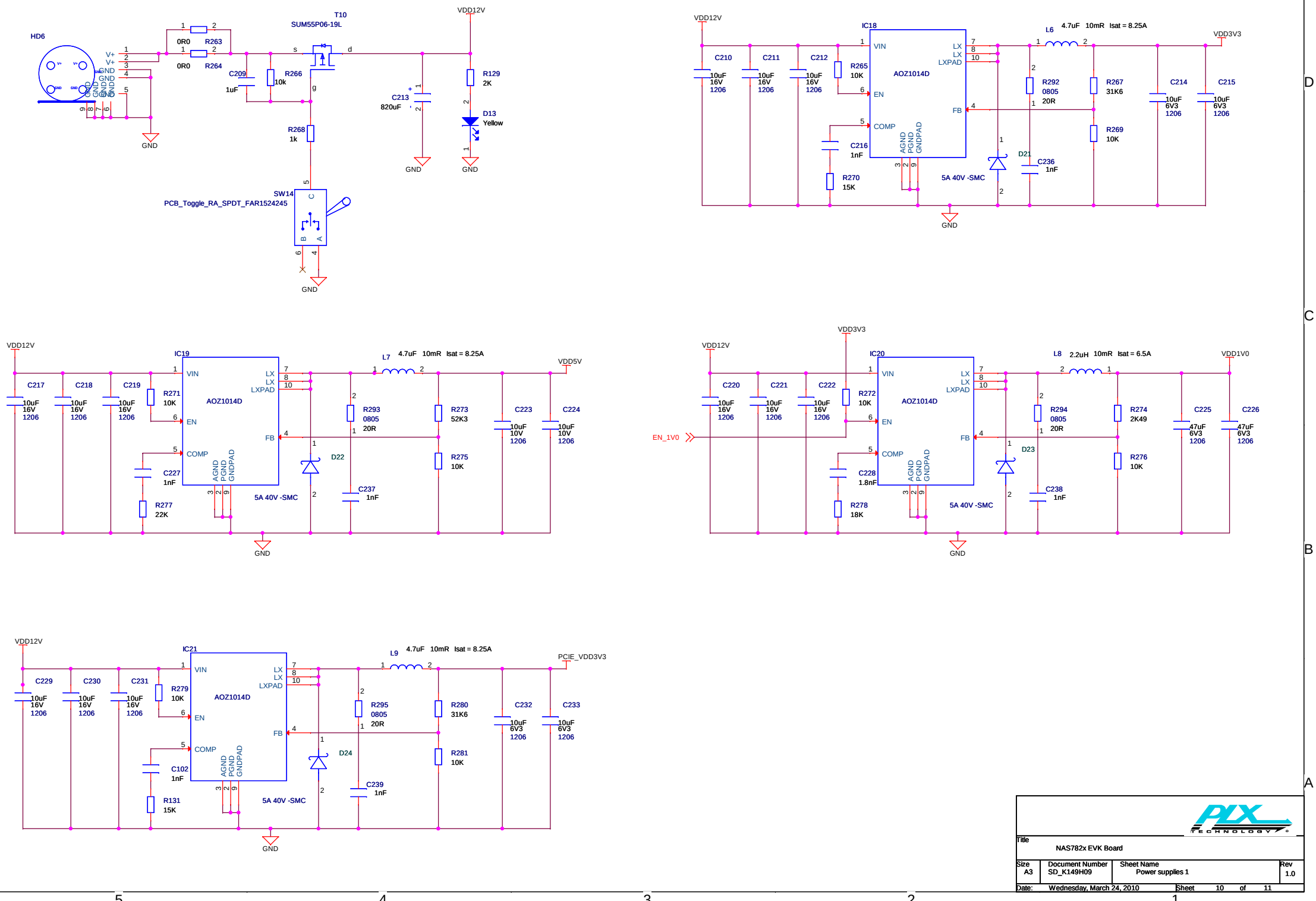



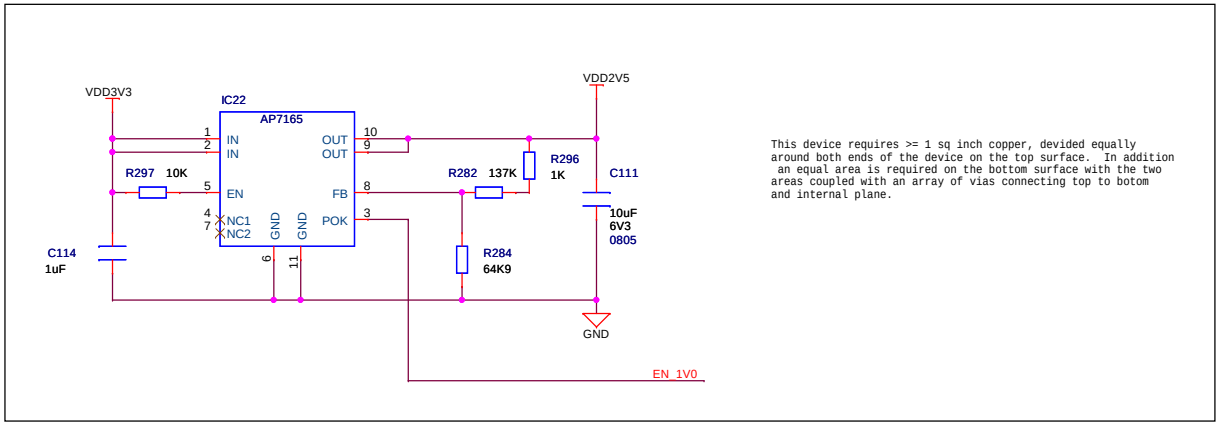




FID1 FID2 FID3 FID4 FID5 FID6 FID7 FID8 FID9 FID10 FID11 FID12

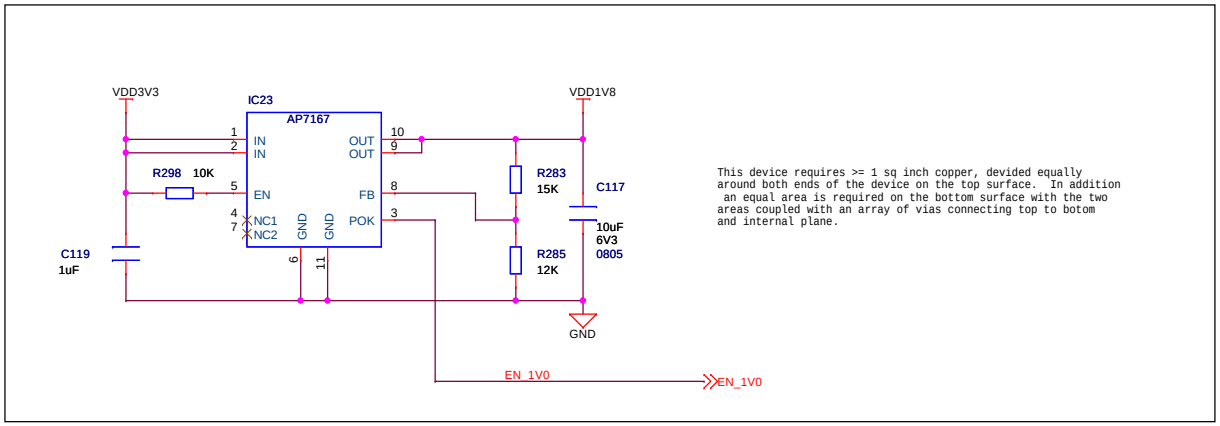
| | | | |
|---|---|---|---|
| Title: NAS782x EVK Board | | | |
| Size: A3 | Document Number: SD_K149H09 | Sheet Name: Miscellaneous | Rev: 1.1 |
| Date: Wednesday, March 24, 2010 | Sheet 9 of 11 | | |



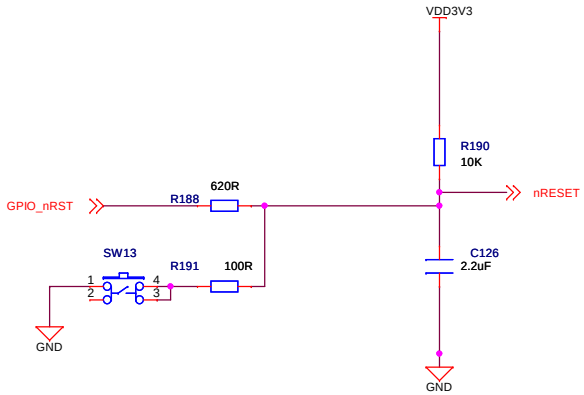

| | | | |
|---|---|---|---|
| Title | NAS782x EVK Board | | |
| Size A3 | Document Number SD_K149H09 | Sheet Name Power supplies 1 | Rev 1.0 |
| Date: Wednesday, March 24, 2010 | Sheet 10 of 11 | | |




This device requires >= 1 sq inch copper, devided equally around both ends of the device on the top surface. In addition an equal area is required on the bottom surface with the two areas coupled with an array of vias connecting top to botom and internal plane.




This device requires >= 1 sq inch copper, devided equally around both ends of the device on the top surface. In addition an equal area is required on the bottom surface with the two areas coupled with an array of vias connecting top to botom and internal plane.




The RESET circuit assumes te 3V3 rail has a rise time of ~4mS. The values chosen give about 20mS from VDD3V3 =3V to nRESET crossing 1.5V.

PLX TECHNOLOGY

| | | | |
|---|---|---|---|
| Title: NAS782x EVK Board | | | |
| Size: A3 | Document Number: SD_K149H09 | Sheet Name: Power supplies 2 | Rev: 1.0 |
| Date: Wednesday, March 24, 2010 | Sheet 11 of 11 | | |