# NAS 7825 Data Sheet

**Version 1.00**
**August 05 2010**
**DS-0068**

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|---|---|
| Website | www.plxtech.com |
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Document number: DS-0068

## Features

- Highly integrated network-attached storage (NAS) system-on-chip (SoC) specifically designed for consumer market
- Dual-core ARM11MP processor architecture with MMU
  - Each core running at 750MHz
- Network coprocessor with TCP/IP acceleration for higher throughput at lower CPU utilization
- Hardware security engine for added security protection
  - AES-128/256-bit based encryption and hashing functions supports for fast secure connection and enhanced protection
- DDR2 SDRAM controller 16-bit interface supports combinations up to 512Mbytes addressable density
- 64Kbyte on-chip SRAM
- 5 channel DMA controller
- 64-bit wide internal processor buses
- Two USB 2.0 host or device controllers
- 1Kbit One-Time Programmable (OTP) eFUSE memory
- Two 10/100/1000 integrated Ethernet MACs with RGMII interface
- Two PCIe interfaces for a variety of applications including IEEE 802.11
- Two integrated SATA 3G host ports with hardware RAID 0 and RAID 1 engines
- Integrated fan tachometer/thermistor controller and Pulse Width Modulation (PWM) outputs
- SPI serial NOR flash, SLC and MLC NAND support
- PCM/TDM interface for connection to voice CODEC/SLAC
- Boot modes:
  - Direct from SATA hard disk (no flash needed)
  - NOR or NAND (SLC/MLC)
- 65nm CMOS process with 1.0V core and 3.3V standard I/O
- 17mm x 17mm 256 pin FBGA (1.0mm ball pitch)
- Highly optimized Linux kernel for high throughput per CPU clock
- Supported file systems: XFS, EXT3, and NTFS

# Device Overview

The NAS 7825 is a next generation network-attached storage (NAS) system-on-chip (SoC). The NAS 7825 delivers a wide array of applications such as media server and automatic backup, combined with easy-to-use software. This makes it ideal for end users who need to store and share their digital information.

The NAS 7825 supports two separate RGMII interfaces for avoiding congestion between ports for high throughput implementations. One application is in the NAS plus router, where one RGMII is the LAN interface and the other is the WAN interface.

The NAS 7825 also supports two PCIe x1 Gen1 interfaces. PCIe is becoming the standard for a variety of applications.

The NAS 7825 supports two hard disks in RAID 0 or RAID 1 configuration. A unique advantage of the NAS 7825 is its support of RAID 0 and RAID 1 in hardware. Hardware support provides higher performance with lower CPU utilization.

The NAS 7825 has an outstanding price/performance ratio with a high level of integration and includes advanced encryption capabilities in hardware. There are two USB 2.0 ports: one acts as a host port, the other can act as a host or device port. These support additional expansion possibilities such as using USB hard disk drives, print server functionality and many other applications. The benefits of the NAS 7825 are:

- Dual-core ARM11MP processor architecture, with each core running at 750MHz clock speed:
  - Dual core architecture enables development of custom applications for differentiation without impacting basic NAS functionality
  - Dual core provides superior multi-application/client processing capabilities
  - Each core can be dedicated to specific applications or share application processing
  - Dual, independent 32K I-cache and D-cache are more resilient to pollution by multiple applications
  - Improved performance/power ratio compared to higher clock processors
- Advanced security features:
  - Hardware-based encryption engine with AES 128/256 bit with SHA-1 SHA-2 hashing functions
  - Digital Transmission Content Protection over Internet Protocol (DTCP/IP)—(product family option) provides added security to copy protected content to other trusted devices within the home
- Higher memory density support, up to 512Mbytes, for supporting advanced applications

- Flexible boot options:
  - Boot directly from the HDD:
    Lowest cost option
    Mac addresses can be programmed in chip One-Time Programmable (OTP) memory
    Redundant images and fully robust in-field upgrades
  - Boot from serial flash and hard disk:
    U-Boot or U-Boot plus simple kernel in flash
  - Secure boot from flash and hard disk:
    Code is CRC checksummed (256b AES) and encrypted with 128b AES
    JTAG and other interfaces disabled
  - Nand flash
    Holds U-Boot, kernel and rootfs (application system software)

## Usage Models

The NAS 7825 has various usage models, including:

- Standalone NAS
- Converged NAS plus router
- Companion chip in PVR/DVR
- Companion chip in set-top box
- Other media server appliances such as internet radio

Figure 1 and Figure 2 show some possible usage models for the NAS 7825.

Figure 1 NAS 7825 Router or Gateway Usage Model

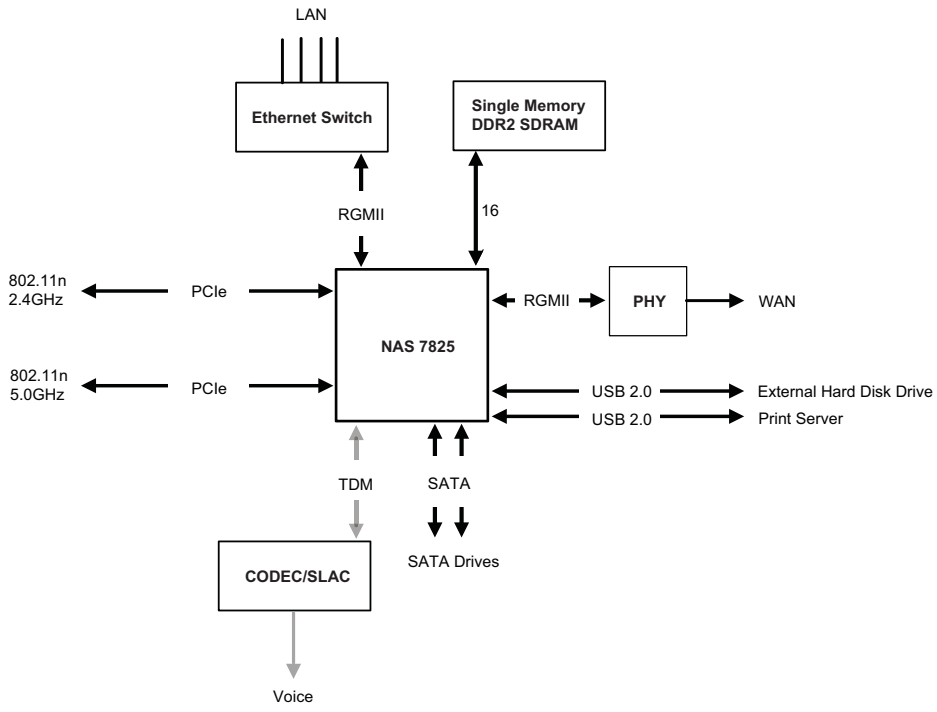
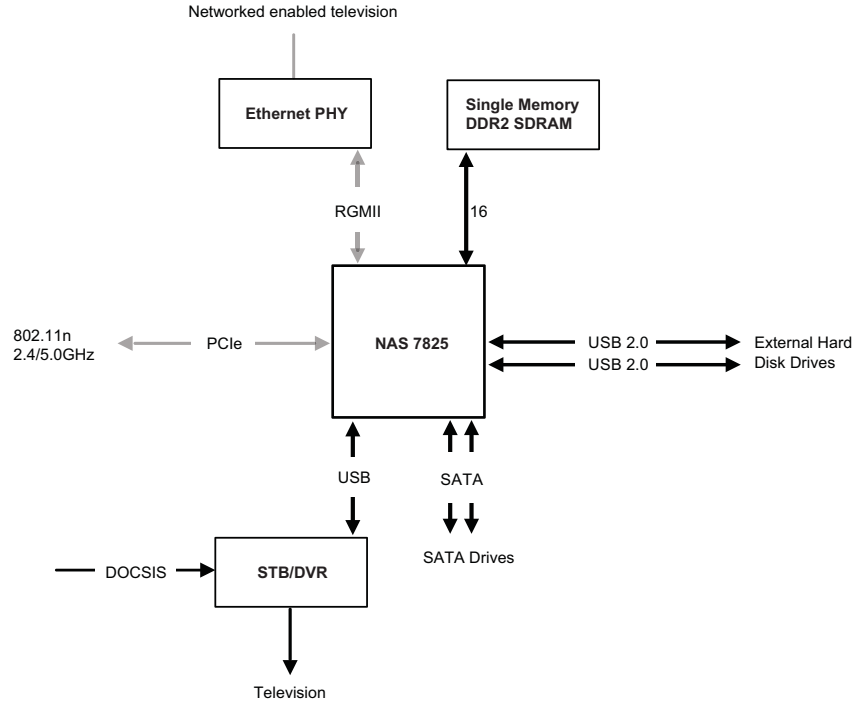


Figure 2 NAS 7825 Set-top Box or DVR Usage Model




## Power Consumption

The following table gives typical and maximum power consumption figures for the NAS 7825 running a NAS application under Linux.

| Supply rail | Standby (mW) | | Active (mW) | | Notes |
|---|---|---|---|---|---|
| | Typ | Max | Typ | Max | |
| 1.0V core + PLLs | 100 | 158 | 480 | 1422 | 1 |
| 3.3V I/O | 33 | 74 | 170 | 186 | 2 |
| 1.8V DDRAM I/O | 18 | 20 | 176 | 194 | 3 |
| PHYs (3.3V and 2.5V) | 6 | 9 | 365 | 392 | |
| Total | 224 | 224 | 1097 | 2101 | 4,5,6 |

**Notes:**

1 750MHz ARM operation.

2 Standby can be reduced further by turning off clocks but the above assumes wake-on-LAN is required, so RGMII I/O cannot be shut down.

3 For Standby, the DDRAM is in self-refresh or is left unrefreshed while the DDR PHY is disabled; all clocks are stopped.

4 Measurements for typical silicon, nominal supply voltages, 25°C.

5 Measurements for slow silicon, maximum supply voltages, 60°C ambient.

6 The following table gives the power specification for each supply rail for power supply design.

The following table gives NAS 7825 power supply specification details.

| Rail | Maximum power supply (mW) | Notes |
|---|---|---|
| VDD10<br>XTAL_VDD10<br>HCSL_VDD10 | 1800 | |
| VDD33<br>XTAL_VDD33 | 400 | |
| VDD18 | 200 | |
| USB_VDD10 | 50 | |
| USB_VDD25 | 50 | |
| USB_VDD33 | 100 | |
| SATA_VDD10 | 50 | |
| SATA_VDD25 | 100 | |
| PCIE_VDD10 | 50 | |
| PCIE_VDD25 | 100 | |
| HCSL_VDD33 | 150 | |
| OTP_VDD25 | 500 | During fuse programming only |
| PLLA_VDDD10<br>PLLB_VDDD10<br>PLLA_VDDA10<br>PLLB_VDDA10 | 50 | |

# Operating Conditions

Table 1 details the maximum ratings for the device.

Table 1 Absolute Maximum Device Ratings

| Symbol | Parameter | Rating | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | DC supply voltage | 1.0V | 1.2 | V |
| $V_{IN}$ | DC input voltage | 1.8V input buffer<br>3.3V input buffer<br>3.3V interface/5V tolerant input buffer | 2.2<br>5.25<br>5.25 | V |
| $V_{OUT}$ | DC output voltage | 1.8V output buffer<br>3.3V output buffer<br>3.3V interface/5V tolerant output buffer | 2.2<br>3.6<br>3.6 | V |
| $T_{STG}$ | Storage temperature | Storage temperature | –65 ... 150 | °C |

Table 2 details the required operating conditions for the device.

Table 2 Recommended Operating Conditions

| Symbol | Parameter | Rating | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | DC supply voltage | 1.0V core (recommended 1.025V)<br>3.3V I/O<br>1.8V DDR I/O<br>2.5V PHY I/O | 0.95<br>3.14<br>1.7<br>2.325 | 1.1<br>3.46<br>1.9<br>2.75 | V |
| $V_{IN}$ | DC input voltage | 1.8V input buffer<br>3.3V input buffer<br>3.3V interface/5V tolerant input buffer | | 1.9<br>3.46<br>5.25 | V |
| $V_{OUT}$ | DC output voltage | 1.8V output buffer<br>3.3V output buffer<br>3.3V interface/5V tolerant output buffer | | 1.9<br>3.46<br>3.46 | V |
| $T_A$ | Ambient temperature range | | 0 | 60 | °C |

## Thermal Data

Thermal resistance (junction to ambient) $\theta_{Ja}$ = 20.0ºC/W in still air.

Maximum junction temperature $T_{Jmax}$ = 110ºC.

# Pinout and Package Information

The NAS 7825 is supplied as a 256 pin FBGA package.

Figure 3 shows the NAS 7825 pin layout.

Figure 3 NAS 7825 Pin Layout Top View

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | ETHA_ TDX3 | ETHA_ TXCTL | ETHA_ RXD0 | ETHA_ RXD1 | ETHA_ RXCLKI | MF_A11 | USBA_DP | RESET_N | USBB_DP | NC | HCSL_ REFCLKAM | HCSL_ REFCLKCM | MF_B0 | MF_B3 | MF_B5 | MF_B6 |
| B | ETHB_ RXD0 | CLKI_ 125M | ETHA_ TXD1 | ETHA_ TXD2 | ETHA_ RXCTL | MF_A10 | USBA_ DM | HIGHZ_N | USBB_DM | NC | HCSL_ REFCLKAP | HCSL_ REFCLKCP | MF_B1 | MF_B4 | XTAL_ VDD10 | XTAL_O |
| C | ETHB_ RXD1 | ETHB_ RXD2 | ETHA_ TXCLKO | ETHA_ TXD0 | ETHA_ RXD3 | MF_A9 | USBA_ XTALI | JTAG_EN | USB_ VSSD | VSS | HCSL_ VDD33 | HCSL_ REXT | MF_B2 | VSS | XTAL_ VDD33 | XTAL_I |
| D | ETHB_ TXD1 | ETHB_ TXD3 | ETHB_ RXD3 | ETHB_ RXCTL | ETHA_ RXD2 | MF_A8 | USBA_ REXT | USB_ VDD33 | USBB_ REXT | HCSL_ VDD10 | VSS | VSS | VDD33 | CLKO_ 25M | SATAB_ TXM | SATAB_ TXP |
| E | ETHB_ TXD0 | ETHB_ TXD2 | ETHB_T XCTL | ETHB_ RXCLKI | VDD10 | VDD33 | VDD10 | USB_ VDD25 | USB_ VDD10 | VDD10 | VDD33 | PLLB_ VDDD10 | PLLB_ VSSA | PLLB_ VDDA10 | SATAB_ RXP | SATAB_ RXM |
| F | MF_A6 | MF_A7 | ETHB_ TXCLKO | MF_A5 | VDD33 | VSS | VSS | VSS | USB_ VSSA | VSS | VSS | VDD10 | SATA_ REXT | PLLB_ VSSD | SATAA_ RXM | SATAA_ RXP |
| G | MF_A1 | MF_A2 | MF_A3 | OTP_ VDD25 | MF_A4 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | SATA_ VDD10 | SATA_ VDD25 | SATAA_ TXP | SATAA_ TXM |
| H | DDRAM_ DQ8 | DDRAM_ DQ14 | DDRAM_ DQ9 | MF_A0 | VDD10 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | VDD33 | MF_B9 | MF_B7 | MF_B8 |
| J | DDRAM_ DQSN1 | DDRAM_ DQSP1 | DDRAM_ VREF | DDRAM_ DQ15 | VDD18 | VSS | VSS | VSS | VSS | VSS | VSS | VDD10 | MF_B10 | PCIE_ REXT | PCIE_ REFCLKIP | PCIE_ REFCLKIM |
| K | DDRAM_ DM1 | DDRAM_ DQ10 | DDRAM_ DQ11 | DDRAM_ GATEO | VDD10 | VSS | VSS | VSS | VSS | VSS | VSS | VSS | PCIE_ VDD10 | VSS | PCIEB_ TXP | PCIEB_ TXM |
| L | DDRAM_ DQ13 | DDRAM_ DQ12 | DDRAM_ DQ6 | DDRAM_ GATEI | VDD18 | VSS | VSS | VSS | VSS | VSS | VSS | VDD10 | PCIE_ VDD25 | VSS | PCIEB_ RXM | PCIEB_ RXP |
| M | DDRAM_ DQ7 | DDRAM_ DQ1 | DDRAM_ DQ0 | DDRAM_ DQ2 | VSS | VDD18 | VDD10 | VDD18 | VDD10 | VDD33 | VDD10 | VDD33 | PLLA_ VDDD10 | PLLA_ VDDA10 | PCIEA_ RXP | PCIEA_ RXM |
| N | DDRAM_ DQSN0 | DDRAM_ DM0 | DDRAM_ DQ3 | DDRAM_ WEN | DDRAM_ BA2 | DDRAM_ A10 | DDRAM_ A3 | DDRAM_ A7 | MF_B15 | MF_B11 | MF_A28 | MF_A24 | PLLA_ VSSD | PLLA_ VSSA | PCIEA_ TXM | PCIEA_ TXP |
| P | DDRAM_ DQSP0 | DDRAM_ DQ4 | DDRAM_ RASN | DDRAM_ CASN | DDRAM_ A0 | DDRAM_ A4 | DDRAM_ A8 | DDRAM_ A13 | MF_B16 | MF_B12 | MF_A29 | MF_A25 | MF_A21 | MF_A14 | MF_A13 | MF_A12 |
| R | DDRAM_ DQ5 | DDRAM_ ODT0 | DDRAM_ CKE | DDRAM_ BA1 | DDRAM_ A2 | DDRAM_ A6 | DDRAM_ A11 | DDRAM_ A12 | MF_B17 | MF_B13 | MF_A30 | MF_A26 | MF_A22 | MF_A19 | MF_A16 | MF_A15 |
| T | DDRAM_ CK | DDRAM_ CKN | DDRAM_ CSN0 | DDRAM_ BA0 | DDRAM_ A1 | DDRAM_ A5 | DDRAM_ A9 | DDRAM_ ODT1 | DDRAM_ CSN1 | MF_B14 | MF_A31 | MF_A27 | MF_A23 | MF_A20 | MF_A18 | MF_A17 |

Table 3 details the pin allocations for the device. In Table 3, Type format is [(W)X] where the following conventions apply:

| W—Supply | | X—Type | |
|---|---|---|---|
| 3V3+ | 5V tolerant 3.3V | I | Input |
| – | 3.3V | O | Output |
| 1V8_ | 1.8V SSTL-18 (for DDR2) | B | Bidirectional |
| | | A | Analog |
| | | P | Power |

| Table 3 NAS 7825 Pin Allocations (Sheet 1 of 4) | | | | |
|---|---|---|---|---|
| Pin | No. Bits | Type | Name | Description |
| Clocks, Reset and Mode (6 pins) | | | | |
| B16 | 1 | O | XTAL_O | Reference clock output. Crystal oscillator output |
| C16 | 1 | I | XTAL_I | 25MHz reference clock input; either crystal oscillator or external clock |
| B8 | 1 | I | HIGHZ_N | Force all inputs to high impedance |
| C8 | 1 | I | JTAG_EN | Enable JTAG |
| A8 | 1 | I | RESET_N | Reset input |
| D14 | 1 | O | CLKO_25M | 25MHz reference clock out |
| Ethernet A Interface (13 pins) | Note: Multi-function I/O pins are needed for MDIO pins | | | |
| A2 | 1 | O | ETHA_TXCTL | Transmit combined enable and error |
| A1, B4, B3, C4 | 4 | O | ETHA_TXD[3:0] | Transmit data @ 125MHz (1Gbps), 25MHz (100Mbps), 5MHz (10Mbps) |
| C3 | 1 | O | ETHA _TXCLKO | Transmit clock |
| B5 | 1 | I | ETHA _RXCTL | Receive combined data valid and error |
| C5, D5, A4, A3 | 4 | I | ETHA _RXD[3:0] | Receive data @ 125MHz (1Gbps) ), 25MHz (100Mbps), 5MHz (10Mbps) |
| A5 | 1 | I | ETHA _RXCLKI | Receive clock |
| B2 | 1 | I | CLKI_125M | Reference clock in 125MHz |
| Ethernet B Interface (12 pins) | Note: Multi-function I/O pins are needed for MDIO pins | | | |
| E3 | 1 | O | ETHB_TXCTL | Transmit combined enable and error |
| D2, E2, D1, E1 | 4 | O | ETHB _TXD[3:0] | Transmit data @ 125MHz (1Gbps), 25MHz (100Mbps), 5MHz (10Mbps) |
| F3 | 1 | O | ETHB _TXCLKO | Transmit clock |
| D4 | 1 | I | ETHB _RXCTL | Receive combined data valid and error |
| D3, C2, C1, B1 | 4 | I | ETHB _RXD[3:0] | Receive data @ 125MHz (1Gbps) ), 25MHz (100Mbps), 5MHz (10Mbps) |
| E4 | 1 | I | ETHB _RXCLKI | Receive clock |
| SDRAM (51 pins) | | | | |
| T1 | 1 | 1V8_O | DDRAM _CK | Differential clock (non-inverted) |
| T2 | 1 | 1V8_O | DDRAM _CKN | Differential clock (inverted) |
| R3 | 1 | 1V8_O | DDRAM _CKE | Clock enable |
| T9, T3 | 2 | 1V8_O | DDRAM _CSN[1:0] | Chip selects |
| P3 | 1 | 1V8_O | DDRAM _RASN | Read address strobe |
| P4 | 1 | 1V8_O | DDRAM _CASN | Column address strobe |
| N4 | 1 | 1V8_O | DDRAM _WEN | Write enable |
| N5, R4, T4 | 3 | 1V8_O | DDRAM _BA[2:0] | Bank address |
| P8, R8, R7, N6, T7, P7, N8, R6, T6, P6, N7, R5, T5, P5 | 14 | 1V8_O | DDRAM_A[13:0] | Address |
| T8, R2 | 2 | 1V8_O | DDRAM _ODT[1:0] | On-die termination control to SDRAM |

Table 3 NAS 7825 Pin Allocations (Sheet 2 of 4)

| Pin | No. Bits | Type | Name | Description |
|---|---|---|---|---|
| J2, P1 | 2 | 1V8_B | DDRAM _DQSP[1:0] | Data in/out strobes (non-inverted) |
| J1, N1 | 2 | 1V8_B | DDRAM _DQSN[1:0] | Data in/out strobes (inverted) |
| K1, N2 | 2 | 1V8_O | DDRAM _DM[1:0] | Data mask |
| J4, H2, L1, L2, K3, K2, H3, H1, M1, L3, R1, P2, N3, M4, M2, M3 | 16 | 1V8_B | DDRAM _DQ[15:0] | Data input/output |
| J3 | 1 | A | DDRAM _VREF | Voltage reference (0.9V) for SSTL-18 |
| K4 | 1 | 1V8_O | DDRAM _GATEO | Loop back to MEM_GATEI. For DQS cleaning |
| L4 | 1 | 1V8_I | DDRAM _GATEI | Loop back from MEM_GATEO. For DQS cleaning |
| SATA Port A (5 pins) | | | | |
| F13 | 1 | A | SATA_REXT | External 191Ω ±1% reference resistor |
| G15 | 1 | AO | SATAA _TXP | Transmit differential data (+); differential outputs to the PHY. Terminals transmit NRZ data at 1.5 or 3.0Gbps |
| G16 | 1 | AO | SATAA _TXM | Transmit differential data (-); differential outputs to the PHY. Terminals transmit NRZ data at 1.5 or 3.0Gbps |
| F15 | 1 | AI | SATAA _RXM | Receive differential data (-); differential inputs to the PHY. Terminals receive NRZ data at 1.5 or 3.0Gbps |
| F16 | 1 | AI | SATAA _RXP | Receive differential data (+); differential inputs to the PHY. Terminals receive NRZ data at 1.5 or 3.0Gbps |
| SATA Port B (4 pins) | | | | |
| E15 | 1 | AI | SATAB_RXP | Receive differential data (+); differential inputs to the PHY. Terminals receive NRZ data at 1.5 or 3.0Gbps |
| E16 | 1 | AI | SATAB _RXM | Receive differential data (); differential inputs to the PHY. Terminals receive NRZ data at 1.5 or 3.0Gbps |
| D15 | 1 | AO | SATAB _TXM | Transmit differential data (); differential outputs to the PHY. Terminals transmit NRZ data at 1.5 or 3.0Gbps |
| D16 | 1 | AO | SATAB _TXP | Transmit differential data (+); differential outputs to the PHY. Terminals transmit NRZ data at 1.5 or 3.0Gbps |
| PCIe Port A (7 pins) | | | | |
| J14 | 1 | A | PCIE_REXT | External 191Ω ±1% reference resistor |
| J15 | 1 | AI | PCIE_REFCLKIP | HCSL reference clock input |
| J16 | 1 | AI | PCIE_REFCLKIM | HCSL reference clock input |
| N16 | 1 | AO | PCIEA _TXP | Transmit differential data (+) |
| N15 | 1 | AO | PCIEA _TXM | Transmit differential data (-) |
| M16 | 1 | AI | PCIEA _RXM | Receive differential data (-) |
| M15 | 1 | AI | PCIEA _RXP | Receive differential data (+) |
| PCIe Port B (4 pins) | | | | |
| K15 | 1 | AO | PCIEB _TXP | Transmit differential data (+) |
| K16 | 1 | AO | PCIEB _TXM | Transmit differential data (-) |
| L15 | 1 | AI | PCIEB _RXM | Receive differential data (-) |

Table 3 NAS 7825 Pin Allocations (Sheet 3 of 4)

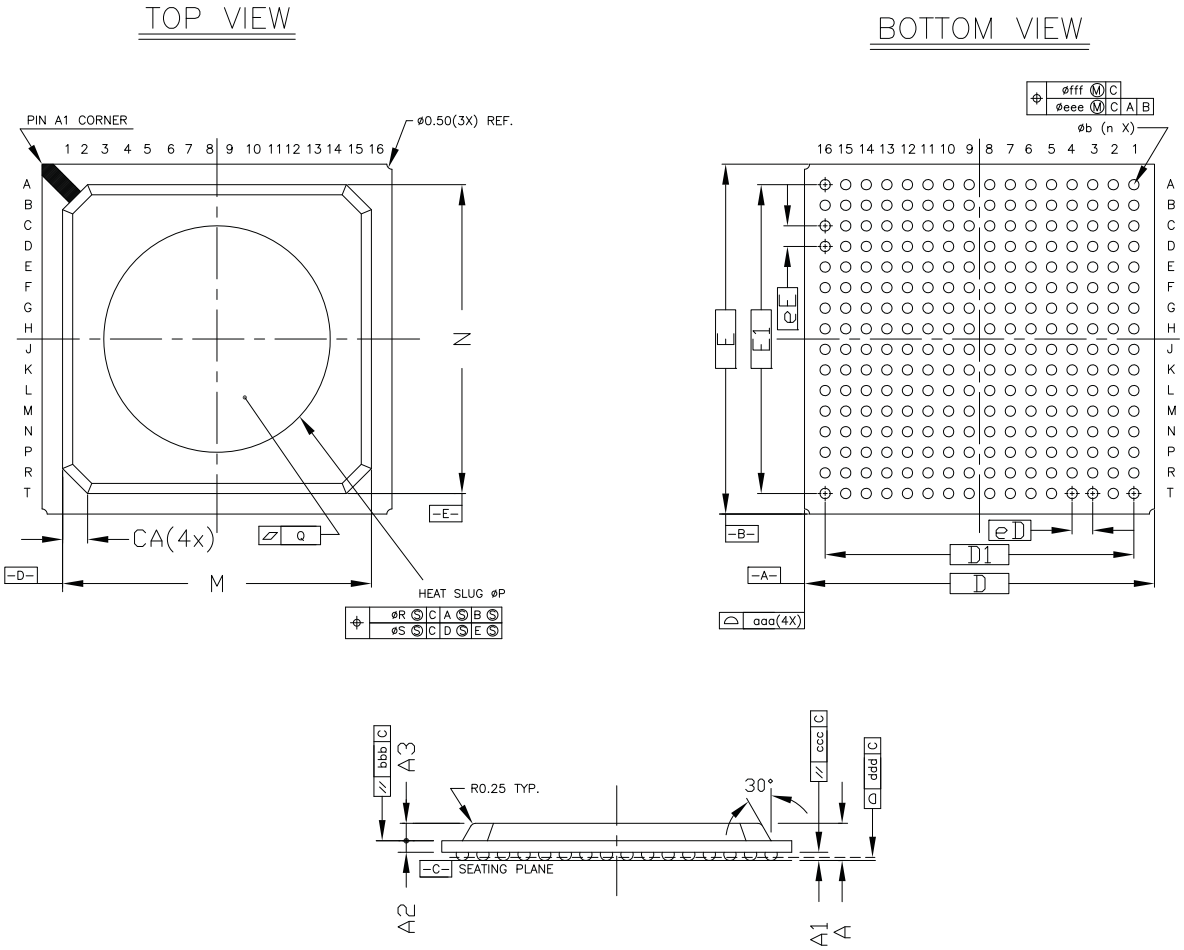
| Pin | No. Bits | Type | Name | Description |
|---|---|---|---|---|
| L16 | 1 | AI | PCIEB _RXP | Receive differential data (+) |
| **HCSL Reference Clocks** ( 7 pins) | | | | |
| C12 | 1 | A | HCSL_REXT | External 475Ω ±1% reference resistor |
| A11, B11 | 2 | AO | HCSL_ REFCLKA[M/P] | 100MHz HCSL differential reference clock output. Intended for PCIEA endpoint |
| A12, B12 | 2 | AO | HCSL_ REFCLKC[M/P] | 100MHz HCSL differential reference clock output. Intended for loopback to PCIE_REFCLKI[M/P] |
| **USB 2.0 Port A** (4 pins) | | | | |
| A7 | 1 | 3V3+B | USBA_DP | Differential data 480Mbps (+) |
| B7 | 1 | 3V3+B | USBA_DM | Differential data 480Mbps (-) |
| D7 | 1 | A | USBA_REXT | External 43.2Ω ±1% reference resistor |
| C7 | 1 | I | USBA_XTALI | Alternative 12MHz clock (Note that 12MHz can be generated internally) |
| **USB2.0 Port B** (3 pins) | | | | |
| A9 | 1 | 3V3+B | USBB_DP | Differential data 480Mbps (+) |
| B9 | 1 | 3V3+B | USBB _DM | Differential data 480Mbps(-) |
| D9 | 1 | A | USBB _REXT | External 43.2Ω ±1% reference resistor |
| **Multi-function I/O** (50 pins) | | | | |
| T11, R11, P11, N11, T12, R12, P12, N12, T13, R13, P13, T14, R14, T15, T16, R15, R16, P14, P15, P16, A6, B6, C6, D6, F2, F1, F4, G5, G3, G2, G1, H4 | 32 | B | MF_A[31:0] | Multi-function I/O pins. Uses depend on pin multiplexing, including general purpose I/O, UART, PWM and static memory bus interface signals |
| R9, P9, N9, T10, R10, R10, P10, N10, J13, H14, H16, H15, A16, A15, B14, A14, C13, B13, A13 | 18 | B | MF_B[17:0] | Multi-function I/O pins. Uses depend on pin multiplexing, including general purpose I/O, UART, PWM and static memory bus interface signals |
| **Power and Ground** (83 pins) | | | | |
| C10, C14, D11, D12, F6, F7, F8, F10, F11, G6, G7, G8, G9, G10, G11, G12, H6, H7, H8, H9, H10, H11, H12, J6, J7, J8, J9, J10, J11, K6, K7, K8, K9, K10, K11, K12, K14, L6, L7, L8, L9, L10, L11, L14, M5 | 45 | P | VSS | Ground |
| J5, L5, M6, M8 | 4 | P | VDD18 | 1.8V SDRAM interface supply |
| M14, M13 | 2 | P | PLLA_VDD[A/D]10 | System PLL 1.0V supply (analog and digital) |
| N14, N13 | 2 | P | PLLA_VSS[A/D] | System PLL ground |
| E12, E14 | 2 | P | PLLB_VDD[A/D]10 | Secondary PLL 1.0V supply (analog and digital) |
| E13, F14 | 2 | P | PLLB_VSS[A/D] | Secondary PLL ground (analog and digital) |
| E5, E7, E10, F12, H5, J12, K5, L12, M7, M9, M11 | 12 | P | VDD10 | 1.0V supply |

Table 3 NAS 7825 Pin Allocations (Sheet 4 of 4)

| Pin | No. Bits | Type | Name | Description |
|---|---|---|---|---|
| M10, M12, D13, E6, E11, F5, H13 | 7 | P | VDD33 | 3.3V supply |
| G4 | 1 | P | OTP_VDD25 | OTP 2.5V supply |
| G13 | 1 | P | SATA_VDD10 | SATA 1.0V supply |
| G14 | 1 | P | SATA_VDD25 | SATA 2.5V supply |
| F9, C9 | 2 | P | USB_VSS[A/D] | USB ground |
| E9 | 1 | P | USB_VDD10 | USB 1.0V supply |
| D8 | 1 | P | USB_VDD33 | USB 3.3V supply |
| E8 | 1 | P | USB_VDD25 | USB 2.5V supply |
| L13 | 1 | P | VDD25 | 2.5V supply |
| B15 | 1 | P | XTAL_VDD10 | 1.0V supply |
| C15 | 1 | P | XTAL_VDD33 | 3.3V supply |
| K13 | 1 | P | PCIE_VDD10 | PCIe 1.0V supply |
| L13 | 1 | P | PCIE_VDD25 | PCIe 2.5V supply |
| D10 | 1 | P | HCSL_VDD10 | HCSL buffer 1.0V supply |
| C11 | 1 | P | HCSL_VDD33 | HCSL buffer 3.3V supply |
| G4 | 1 | P | OTP_VDD25 | OTP 2.5V supply |
| Not Connected (2 pins) | | | | |
| A10, B10 | 2 | | NC | These pins must not be connected |

Figure 4 shows the package for the NAS 7825.

Figure 4 NAS 7825 Package



The following table explains the symbols used in Figure 4.

| Item | | Symbol | Dimensions |
|---|---|---|---|
| Body size | X | D | 17.000 |
| | Y | E | 17.000 |
| Ball pitch | X | eD | 1.000 |
| | Y | eE | 1.000 |
| Total thickness | | A | 1.810 ±0.190 |
| Mold thickness | | A3 | 0.850 Ref. |
| Substrate thickness | | A2 | 0.560 Ref. |
| Ball diameter | | | 0.500 |
| Stand off | | A1 | 0.300 ~ 0.500 |
| Ball width | | b | 0.400 ~ 0.600 |
| Mold area | X | M | 15.000 |
| | Y | N | 15.000 |
| H/S exposed size | | P | 10.000 ~ 11.000 |
| H/S coplanarity | | Q | 0.100 |
| H/S shift with substrate edge | | R | 0.300 |
| H/S shift with mold area | | S | 0.555 |
| Chamfer | | CA | 1.21 Ref. |
| Package edge tolerance | | aaa | 0.200 |
| Substrate flatness | | bbb | 0.250 |
| Mold flatness | | ccc | 0.350 |
| Coplanarity | | ddd | 0.200 |
| Ball offset (package) | | eee | 0.250 |
| Ball offset (ball) | | fff | 0.100 |
| Ball count | | n | 256 |
| Edge ball center to center | X | D1 | 15.000 |
| | Y | E1 | 15.000 |

## DDR2 Choices and Constraints

This section gives an overview of our recommendations and gives notice of constraints when designing DDR2 memory combinations with the NAS 7825.

Use a single DDR2 device where possible, because the DDR interface has tight timing requirements and the loading on the interface signals is reduced when using a single device compared to two devices.

Use 8 bit wide DDR2 devices when using two DDR2 devices, in preference to two 16 bit wide devices. This is because the two 8 bit wide devices have a single DDR2 load on the data bus, which improves the DDR2 interface timings.

The following table gives all DDR2 device combinations that provide specific total system memory requirements. The **Preference** column indicates the recommended combinations for the different total memory sizes.

| Memory Size MBytes | Memory Organisation | No. of Devices | Preference | Notes |
|---|---|---|---|---|
| 64 | One rank of 512Mb, x16 | 1 | 1 | |
| 128 | One rank of 1Gb, x16 | 1 | 1 | |
| 256 | One rank of 2Gb, x16 | 1 | 1 | |
| | 2 x one rank of 1Gb, x8 | 2 | 2 | Needs series and parallel termination with termination regulator |
| | Two ranks of 1Gb, x16 | 2 | 3 | Needs series and parallel termination with termination regulator. Requires modified software: contact PLX Technology Sales Support |
| 512 | Two ranks of 2Gb, x16 | 2 | 1 | Needs series and parallel termination with termination regulator. Requires modified software: contact PLX Technology Sales Support |

For more information on DDR2 design choices, see GS-0100: *PCB Design Guidelines*.

## Ordering Information

The order codes for the NAS 7825 are:

- Device only: NAS7825-AABC F
- Rapid Development Kit (RDK): NAS7825-AA RDK

## Revision Information

The following table documents the revisions of this guide.

| Revision | Date | Modification |
|---|---|---|
| 1.00 | August 05 2010 | No longer preliminary. |
| 0.60 | July 12 2010 | Addition of Power Consumption, Thermal Data, DDR2 Choices and Constraints; update to Operating Conditions, Pinout and Package Information |
| 0.50 | January 28 2010 | Corrected Pinout and Package Information |
| 0.40 | January 21 2010 | Updates to Features, Pinout and Package Information, Ordering Information |
| 0.20 | October 13 2009 | First publication (preliminary) |

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