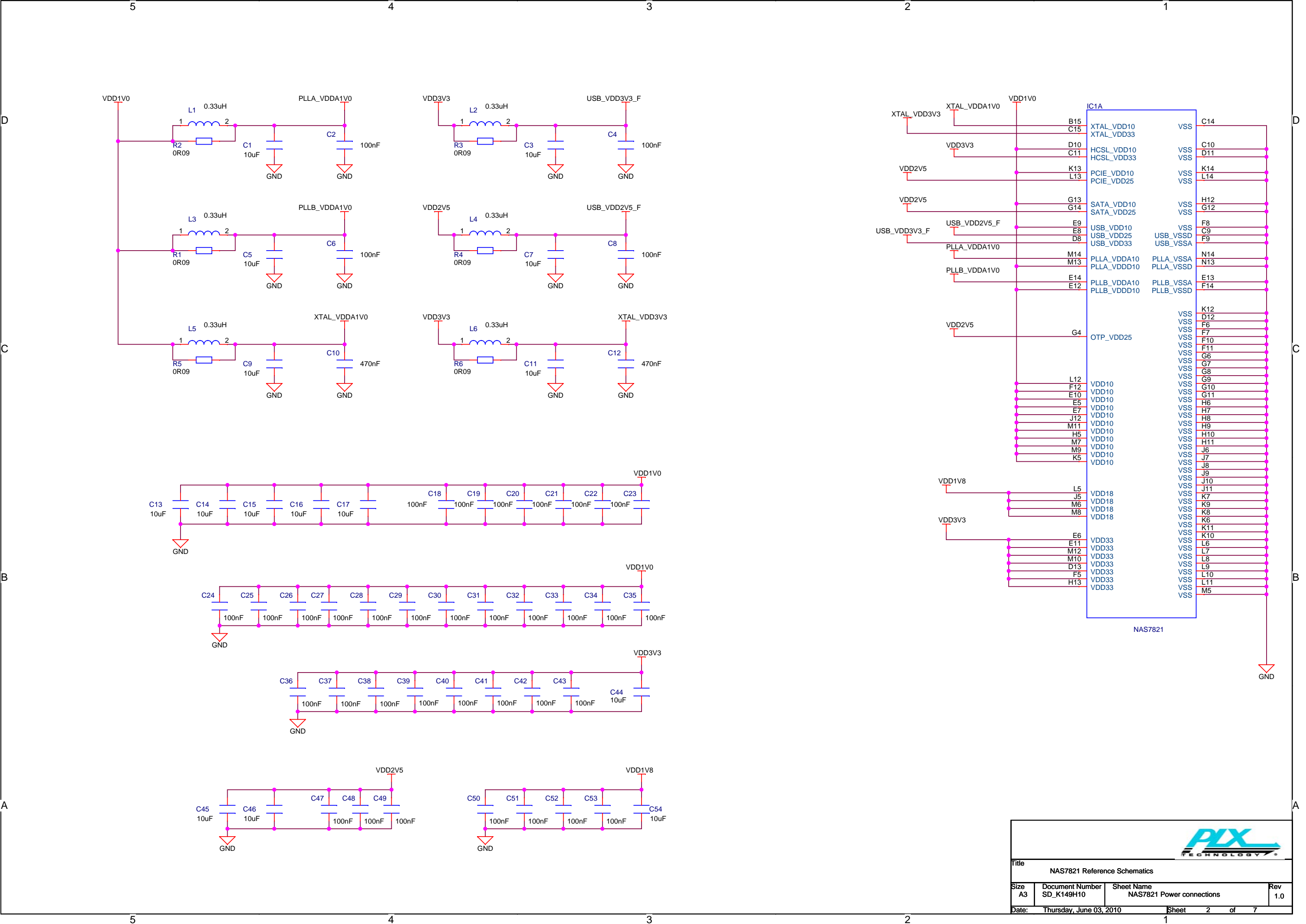
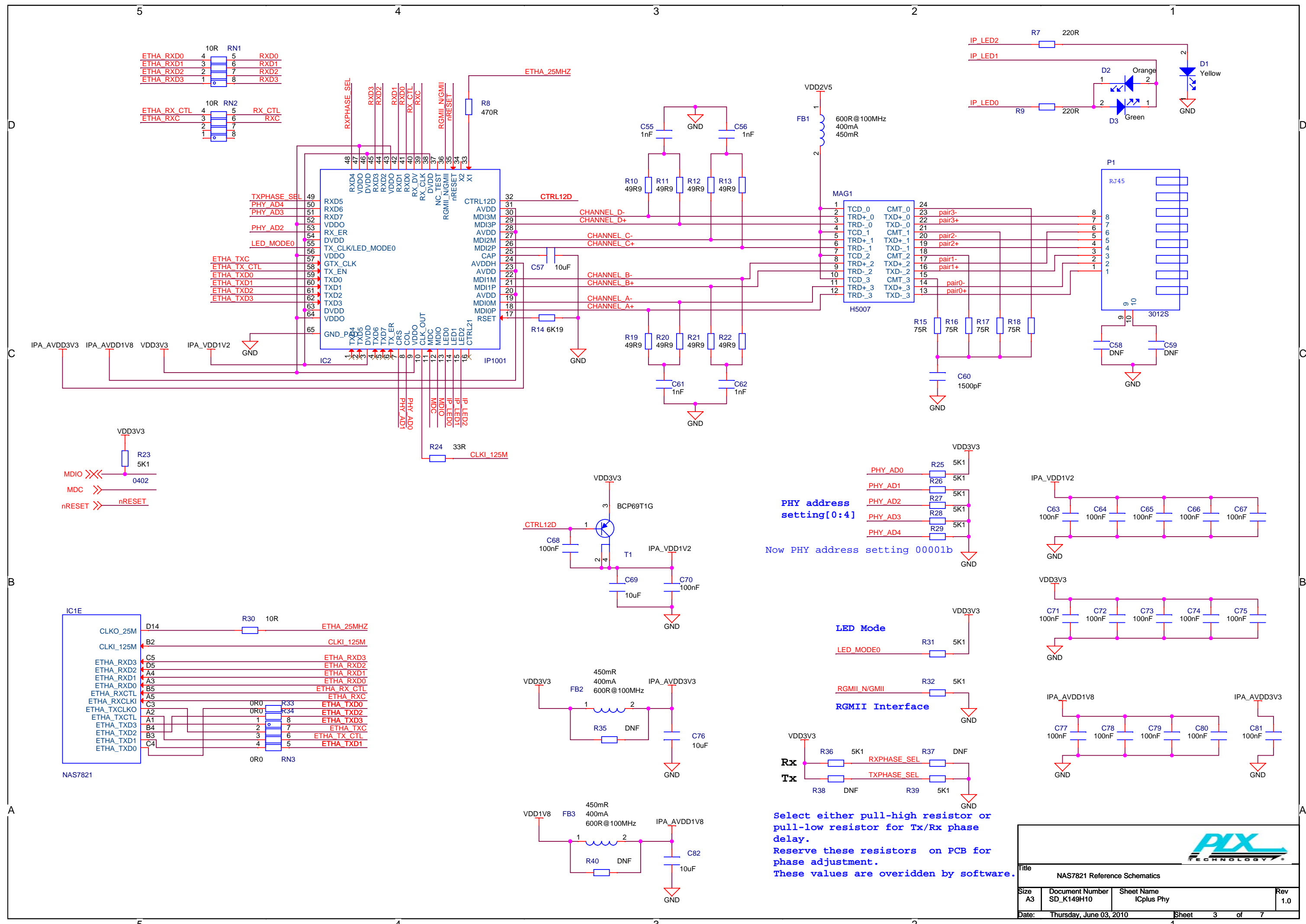


NAS7821/0 Reference Schematic

Doc No: SD_K149H10

Overall Revision:	1.0	1.1
Sheet Number Rev'n	-----	-----
2	1.0	1.0
3	1.0	1.0
4	1.0	1.1
5	1.0	1.0
6	1.0	1.0
7	1.0	1.0



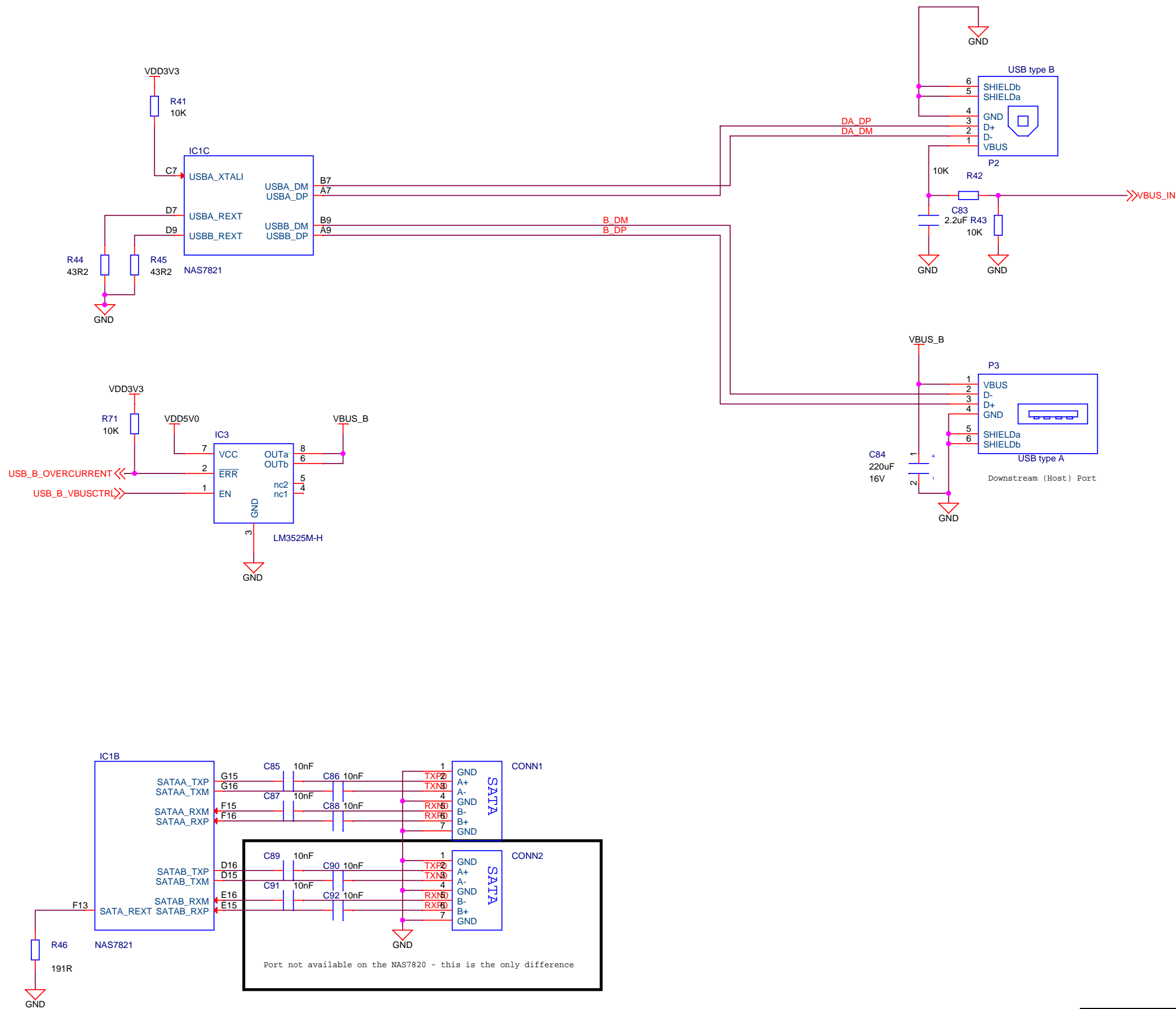


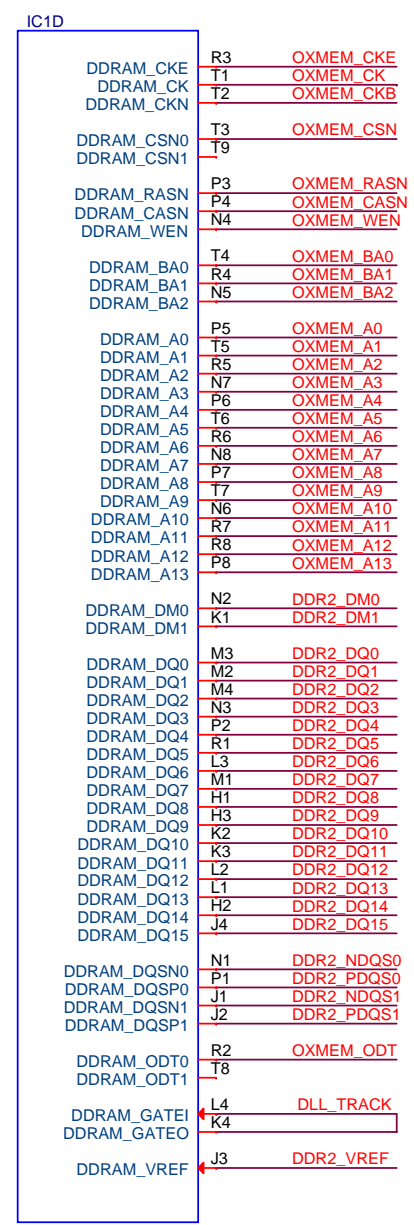
PHY address setting[0:4]
Now PHY address setting 00001b

LED Mode
LED_MODE0

RGMII Interface
RGMII_N/GMII

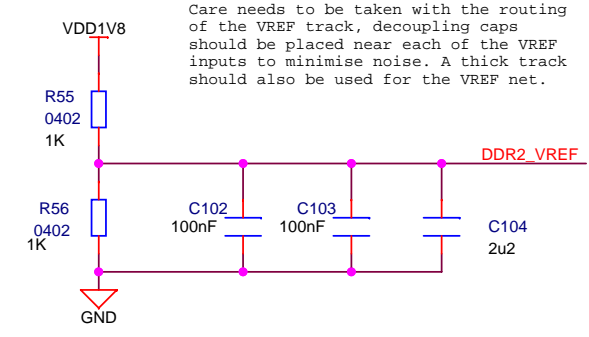
Select either pull-high resistor or pull-low resistor for Tx/Rx phase delay.
Reserve these resistors on PCB for phase adjustment.
These values are overridden by software.



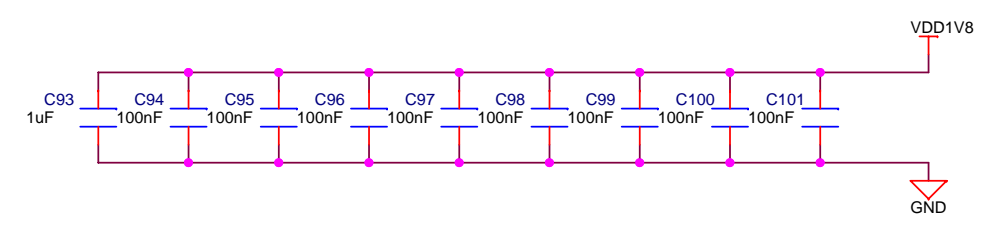
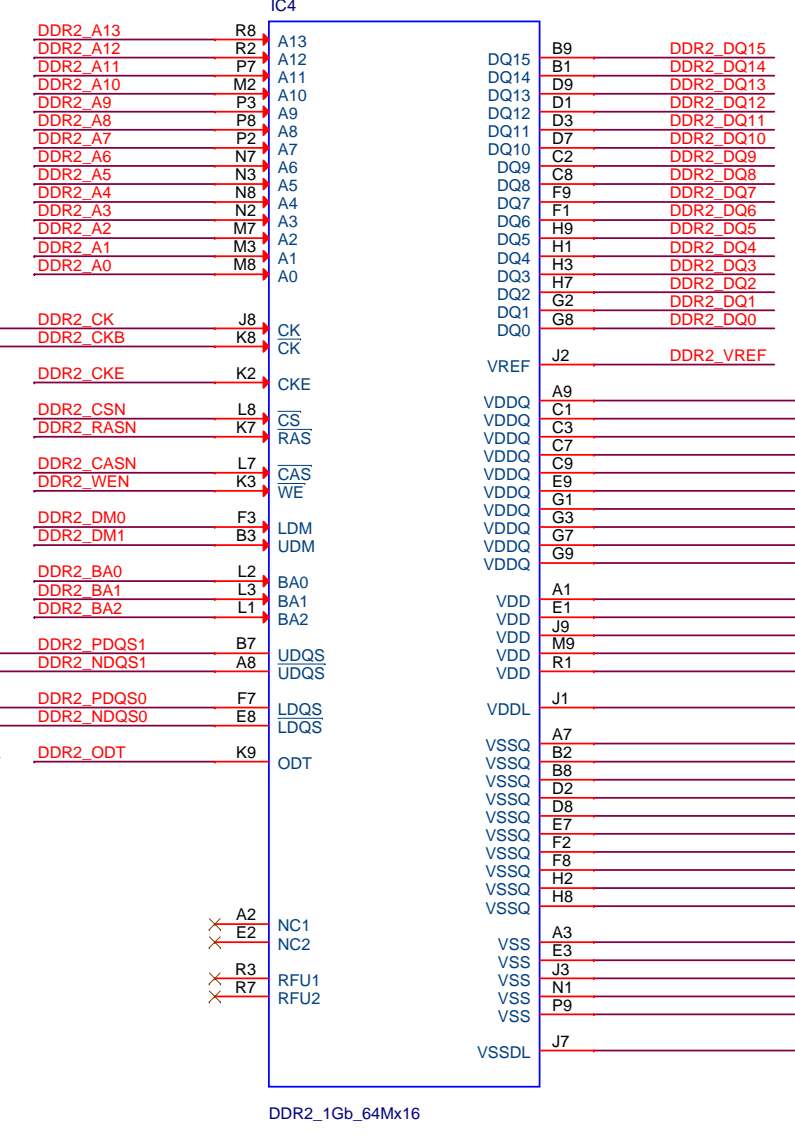
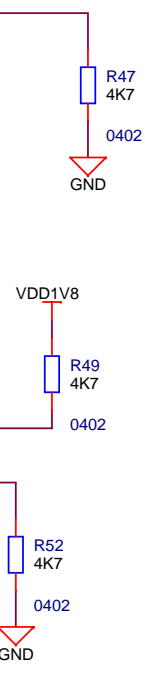
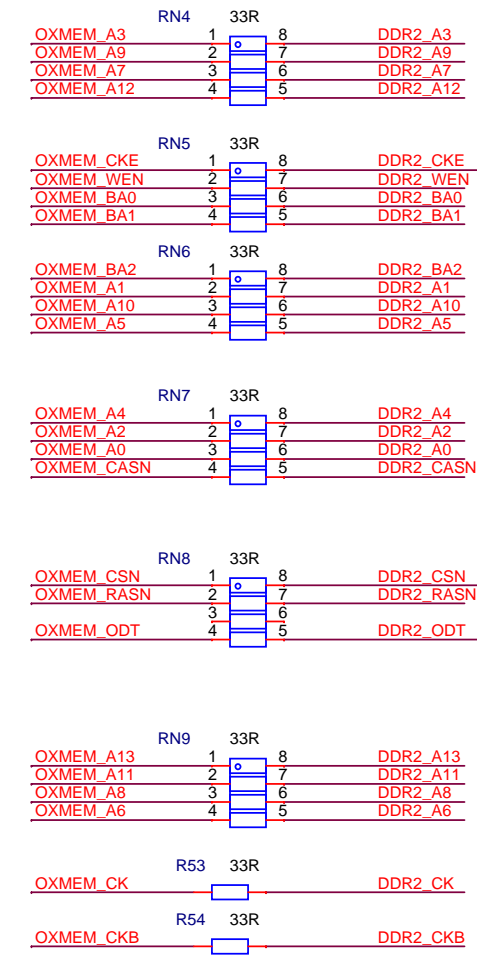


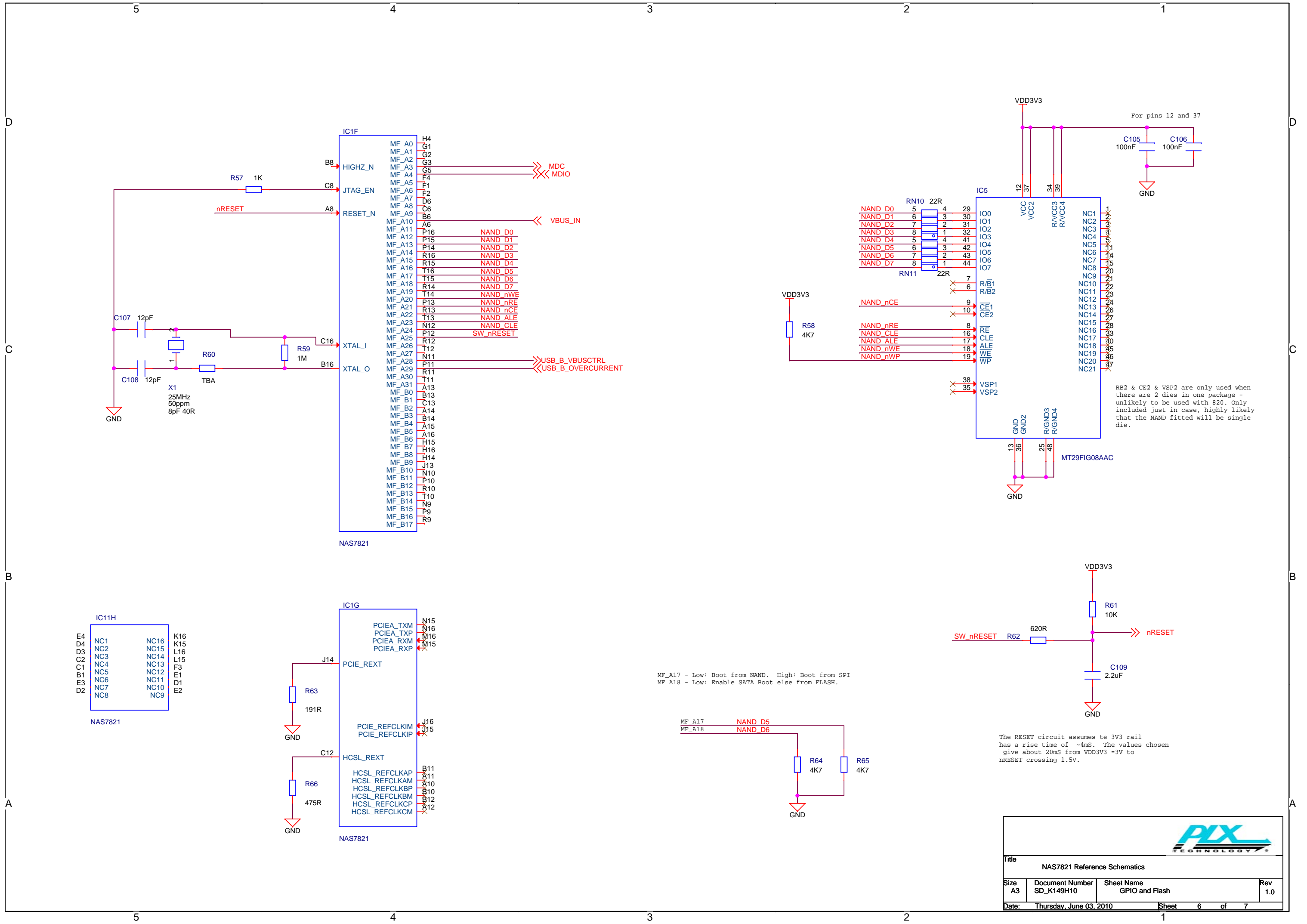
NAS7821

The DQ[15:0], PDQS0, NDQS0, PDQS1, NDQS1, DM0 & DM1 signals have ODT (DM0 & DM1 will only have ODT at the DDR2 IC)



Care needs to be taken with the routing of the VREF track, decoupling caps should be placed near each of the VREF inputs to minimise noise. A thick track should also be used for the VREF net.





NOTE THAT THIS SCHEMATIC ASSUMES THAT THERE WILL BE AN EXTERNALLY GENERATED 12V & 5V SUPPLY (required by the hard drive as well)

This power supply design shows a potential implementation. Other schemes can be used. Ensure that the power supply requirements for the gigabit PHY and the NAS7821 are met. Refer to the appropriate datasheets.

