作業系統概論 HW2 Report

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I–2. Potential issues with the programs

1. access time degradation: when several processors try to access the same memory location it causes contention. Trying to access nearby memory locations may cause false sharing.
2. lack of data coherence: whenever one cache is updated with information that may be used by other processors, the change needs to be reflected to the other processors, otherwise the different processors will be working with incoherent data.

How to fix above two issues: cache coherence protocols (with Write Propagation and Transaction Serialization)

Write Propagation: Changes to the data in any shared memory must be propagated to other copies in the peer memories.

Transaction Serialization: Reads/Writes to a single memory location must be seen by all processors in the same order.