Survey Of Several Recent Full Adder Designs

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***Abstract*—This paper presents three hybrid full adder designs respectively proposed from 2021, 2020, and 2018. Those designs are involved in techniques such as XOR-XNOR gate, CMOS, Gate Diffusion Input(GDI), Transmission Gate(TG), and multi-threshold-voltage(MTV). For every design, detail of the FA circuit, the goal of the designers, performance simulation results performed by the designers are presented. After comparing three designs in terms of power consumption, propagation delay, and transistor count or area overhead, After comparing three designs in terms of power consumption, propagation delay, and transistor count or area overhead,**

***Index Terms*—Full Adder, 1-bit Adder, Hybrid, CMOS, MVT, GDI**

I. Introduction

Addition operation plays an important role in very-large-scale integration(VLSI) since it is most common and frequently used in arithmetic operations. With the development of modern technology, more and more techniques and design have emerged, to pursue a goal of making the chips less performance delay, less silicon area overhead, and less power consumption. As is discovered that hybrid logic full design has many merits than the single logic design, circuit designers are more interested in hybrid logic.

Recently in 2021, a 22T XOR-XNOR-based hybrid full adder design [1] was proposed which uses an XOR-XNOR module combined with the sum-generation module which uses TG technique and the carry-generation module which use CCMOS technique.

Back in 2020, an 18T hybrid full adder design [2] came out. This design is also a three modules cell based on a XOR-XNOR circuit. With this fundamental circuit, two 4T circuits, which use the GDI technique and TG technique respectively, are driven to generate sum and carry.

Further move backward to 2018, a 14T MVT-GDI-based hybrid full adder design was proposed [3]. This 5 modules FA cell adopts GDI logic and MTV transistor logic and also swing restoring gate.

This paper presents all three FA designs in a fixed order from module design detail to the purpose of FAs designers, and FAs performance simulation results performed by the designers.

In section II, the 22T XOR-XNOR-based hybrid FA is discussed as FA-1. Then in section III, the 18T hybrid FA is discussed as FA-2. Section IV, the 14T MVT-GDI-based hybrid FA is discussed as FA-3. After that, in section V, the overall comparison of three FA design is presents. Section VI gives the conclusion.

II. FA-1: XOR-XNOR-based Hybrid FA

A. Design

The FA-1 [1] design contains three modules to realize a 1-bit full adder. Firstly, an XOR-XNOR circuit will take original inputs A and B as its input and produce two signals, one is from the XNOR gate marked as S_{xnor_out} and the other is from the XOR gate marked as S_{xor_out}. Then, a TG-based circuit as the second module will take both signal and the input carry C_{in} to calculate the Sum while a third module will then use the C_{in} along with A, B and signals S_{xnor_out}, S_{xor_out} to generate the carry C_{out}.

Fig. 1 presents the block diagram of the design.

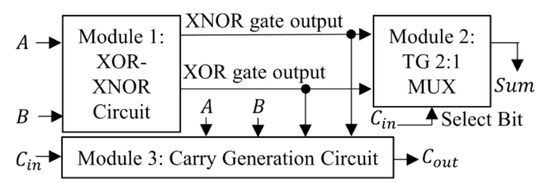

Fig. 1. Block Diagram of FA-1

1) *Module 1:* XOR-XNOR Circuit

The circuit consists of 10 transistors as is shown in Fig. 2.

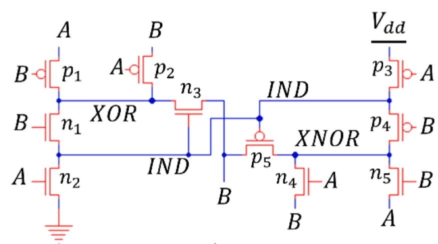

Fig. 2. XOR-XNOR Circuit of FA-1

For all the possible A, B inputs, table I presents all the output patterns also the responsible transistors within the circuit. As the table presented, it is clear that at least one transistor path can provide full swing output to prevent threshold voltage loss.

2) *Module 2:* Sum Generation Circuit

From the Table II, two paths for the Sum generation can be concluded:

when C_{in} = 0:

$$Sum = A \oplus B$$

TABLE I
OPERATION TABLE OF THE XOR-XNOR CIRCUIT OF FA-1

XOR Circuit					
	Input		**Output Transistor Path**		**Output**
Pattern no.	A	B	Full Swing Transistor Path	Non-Full Swing Transistor Path	Output Signal/logic
1.	0	0	n_3	p_1/p_2	$B/0$
2.	0	1	p_2	n_1/n_3	$B/1$
3.	1	0	p_1	None	$A/1$
4.	1	0	n_1 and n_2	None	0
XNOR Circuit					
	Input		**Output Transistor Path**		**Output**
Pattern no.	A	B	Full Swing Transistor Path	Non-Full Swing Transistor Path	Output Signal/logic
1.	0	0	p_3 and p_4	None	1
2.	0	1	n_5	None	$A/0$
3.	1	0	n_4	p_4/p_5	$B/0$
4.	1	0	p_5	n_4/n_5	$B/1$

TABLE II
TRUE-FALSE TABLE OF FA

Inputs			**Outputs**	
C_{in}	A	B	C_{out}	Sum
0	0	0	0	0
	0	1	0	1
	1	0	0	1
	1	1	1	0
1	0	0	0	1
	0	1	1	0
	1	0	1	0
	1	1	1	1

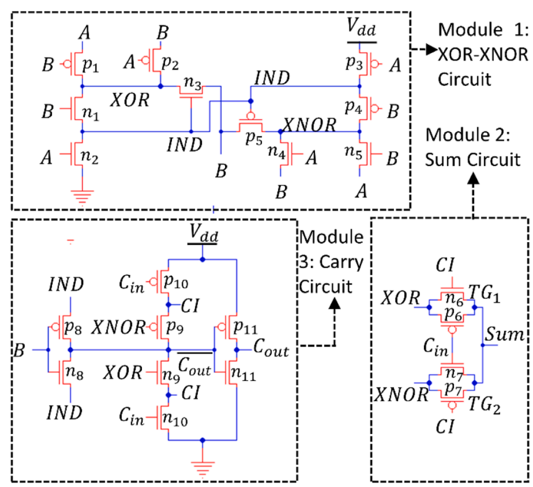

Fig. 3. FA-1 Circuit

when C_{in} = 1:

$$Sum = A \odot B$$

For input selection, a 2:1 Multiplexer(2:1 MUX) based on Transmission Gate(TG) has been used for figuring the Sum.

As is given in Fig. 3, two TGs are used for implementing 2:1 MUX logic and with this manner, the Sum generation circuit can also provide full swing output.

3) Module 3: Carry Generation Circuit

As per Fig. 3, the Carry generation circuit uses a CCMOS logic-based inverter at the output. With this logic, the output voltage level of this circuit is either V_{dd} or G_{nd} level. It is a good design for the extensibility of the circuit since the design of the carry generation logic is the most important factor of the scalability of the wide word length adders.

B. Discussion

FA-1 shows impressive improvements compared to many other FAs. The designers are intended to solve the voltage degradation issue with the hybrid logic-based design, hence they design the XOR-XNOR-based circuit to produce full swing output for its next stage and choose TG for implementing the sum generation circuit.

Finally, for the purpose of high-speed calculations and good scalabilities, they apply the CCMOS technique at the output terminial. The designed carry generation circuit can be extended to multiple bits adder structures with no additional voltage level restoring buffers. Furthermore, this logic can reduce the carry chain delay with involving just one pull-up and pull-down transistors.

As for the area overhead, a total of 22 transistors are used to produce this FA, namely, 10 on module one, 4 on module 2, and 8 on module 3.

According to the designers' simulation in terms of average power(AP), propagation delay(PD), area delay product(ADP), power delay product(PDP) on 1-bit FA, compare with the conventional CMOS FA [4] and other recent FA designs [5], [6], [3], this design achieves many improvements which can be shown in Table III.

Again, based on the presenters' simulations of the word-length adder architecture [1], the FA-1 continues to rank first in these performance comparisons with its scalability advantages, especially on 16-bit and 32-bit.

TABLE III
SIMULATIONS PERFORMED BY THE DESIGNERS OF FA-1

FA Cell	TC	Performance					Improvements with Respect to CCMOS FA				
		Area (μm^2)	AP (μW)	PD (ps)	ADP (μm^2.ps)	PDP (αJ)	Area(%)	AP(%)	PD(%)	ADP(%)	PDP(%)
[4] CCMOS	28	10.13	1.28	60.3	610.84	77.18	0.00	0.00	0.00	0.00	0.00
[5] Bhattacharyya's	16	7.58	**0.62**	98.7	748.15	61.19	25.17	**51.56**	-63.68	-22.48	20.72
[6] Kandpal's	20	9.18	0.92	54.06	496.27	49.74	9.38	28.13	10.35	18.76	35.55
[3] Sanapala's	14	**7.38**	0.75	56.7	415.45	42.53	**27.15**	41.41	5.97	31.99	44.90
[1] FA-1	22	8.17	0.85	**38.5**	**267.40**	**32.73**	19.35	33.59	**36.15**	**56.22**	**57.59**

Performed in 1V for 45nm technology

III. FA-2: 18T HYBRID FA

A. Design

The FA-2 [2] design contains three modules. Same as FA-1 [1], the module 1 of the FA-2 is an XOR-XNOR circuit that sending out two signals to drive Module 2 and Module 3 for the calculation of Sum and $Carry$.

Module 1 from FA-2 first take A and B and produce signal H (result of $A \oplus B$) and signal $\overline{H}$ (result of $A \odot B$). Module 2 then take H and C_{in} to calculate the Sun ($C_{in} \oplus H$). Module 3 finally figure the C_{out} out from the input A and C_{in} also count in the selection between H and $\overline{H}$.

The expressions of those outcomes can be:

$$Sum = H\overline{C_{in}} + \overline{H}C_{in} = A \oplus B \oplus C_{in}$$

$$C_{out} = HC_{in} + \overline{H}A$$

1) Module 1: XOR-XNOR Circuit

The structure of module 1 is presented in Fig. 4. To avoid the lack of voltage level, a feedback loop is attached to the XOR output and XNOR output for reaching the power required to drive the next two modules. So it use a pMOS transistor as Mpf, a nMOS transistor as Mnf. Any weak logic signal produced by the XOR gate or the XNOR gate (when $A = B$) will be handle by the feedback loop and obtains perfect logic signal at the H or $\overline{H}$ output. For example, if $A = B = 0$, weak logic 0 will be produce at the XOR gate as H, but it still turns ON the Mpf and then logic 1 passes to the Mnf, thus a perfect logic 0 is taken at the H.

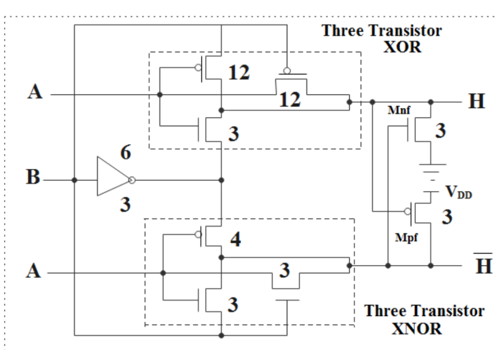

Fig. 4. Module 1 of FA-2

2) Module 2: Sum Generation Circuit

The structure of module 2 is presented in Fig. 5. Sum generate implementation of FA-2 is an XOR gate with Gate Diffusion Input technique. So it can generate the full swing output. When using GDI on the XOR gate, it is required that an inverter provide a perfect signal to the inputs. But since it retrieves such signal from module 1, the implementation of this module will only need 4 transistors to finish the task.

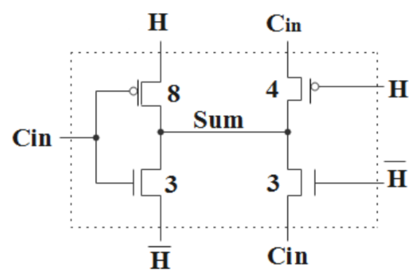

Fig. 5. Module 2 of FA-2

3) Module 2: Carry Generation Circuit

The structure of module 3 is presented in Fig. 6. The circuit is a 4 pass transistors(PT) 2-to-1 MUX, and it will provide a full swing output by a pMOS and an nMOS conducted in each of the input patterns. For instance, when $H = A = 0$, Mp1 and Mn2 turn on, a logic 0 goes through these transistors, C_{out} obtains perfect 0.

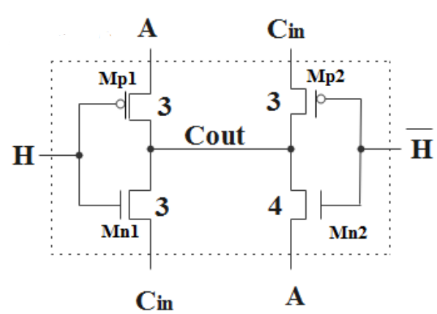

Fig. 6. Module 3 of FA-2

B. Discussion

FA-2 design is a lean logic cell for the addition operation. The designers were well aware of the problems such as bad performance happens at low supply voltages and the stability of the produced output at different loading conditions. The design combined feedback loop design, GDI design, and PT technique all together to solve these problems.

With respect of area overhead, 18 transistors are used to bulid this cell. 10 on module 1, 4 on module 2, and 4 on module 3.

As simulations performed by the designers which presented in Table IV, FA-2 shows its advantages on power consumption, speed, and PDP aspects compared with one old hybrid CMOS FA [7] and one hybrid FA [5].

TABLE IV
SIMULATIONS PERFORMED BY THE DESIGNERS OF FA-2

FA Cell	**TC**	**Performance**		
		AP(μW)	PD(ps)	PDP(fJ)
[7] Hybrid CCMOS	24	6.21	143	0.888
[5] New Hybrid	16	1.1766	91.3	0.107
[2] FA-2	18	**1.104**	**85.22**	**0.0941**

Performed in 1.2V for 90nm technology

IV. FA-3: GDI-BASED HYBRID FA

A. Design

The FA-3 [3] design, whose structure is illustrated in Fig. 7, consists of five logic modules. One XOR/XNOR circuit, two MUX circuits, one Swing Restored Transmission Gate(SRTG) circuit, and one Swing Restored Pass Transistor(SRPT) circuit.

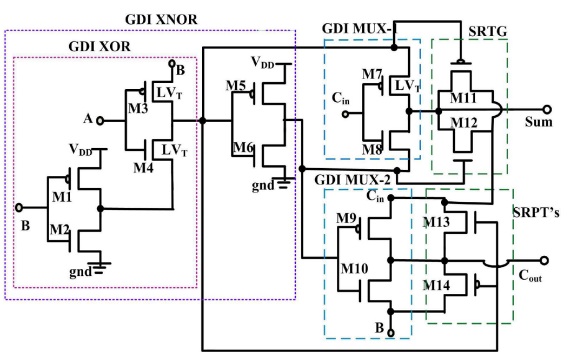

Fig. 7. FA-3 Circuit

The first module, a XOR/XNOR block, is assembled using GDI design style. Different from FA-2, module 1 of FA-3 needs a series of inverters to cope with voltage drop issues and, thus, to work with standard V_T(threshold voltage) devices.

The second module, a GID MUX-1 block, handles the output from both XOR gate and XNOR by a control input C_{in} then figures the sum out. So the function can be represented as:

$$Sum = \overline{C_{in}}(A \oplus B) + C_{in}(A \odot B)$$

The third module, another GID MUX-2 block handles the inputs C_{in} and B by control line from the output($A \odot B$) of XNOR logic. The function can be represented as:

$$C_{out} = (\overline{A \odot B})C_{in} + (A \odot B)B$$

The rest of the two modules are used for full swing logic generation which means a SRTG at the output of the sum and two SRPTs at the carry output.

The functional pattern of the overall circuit is shown in Table VII and Table V.

TABLE V
THE OUTPUTS OF THE FUNCTION TABLE OF FA-3

Input Patterns	Sum	C_{out}
1	0	0
2	1	0
3	1	0
4	0	1
5	V_{DD}-V_T(M4)	0
6	0	1
7	0	1
8	1	1

B. Discussion

FA-3 design focuses on providing a full logic swing at ultra-low-voltage(ULV) situation also considering the area overhead and power saving. To achieve those purposes, the designers choose techniques like multi-threshold voltage(MTV) transistors(in the threshold drop paths), GDI design style(to reduce the occupied area), and swing restoring gates at the output(for full swing output and faster speed).

Three of the five modules are using GDI technique so that the cell require less transistors to perform the function.

Overall, 14 transistors are used in consists of FA-3, briefly saying, 6 in module 1, rest of each module needs 2 transistors.

The designers perform simulations on FA-3 which can be shown in Table VI. Notice that the simulation was conducted at ULV condition, FA-3 has the best performance in terms of delay, energy, and energy delay product(EPD).

TABLE VI
SIMULATIONS PERFORMED BY THE DESIGNERS OF FA-3

FA Cell	**TC**	Area (μm^2)	AP (pW)	Delay (µs)	Energy (αJ)	EDP (yJs)
[4] CCMOS	28	8.536	2.523	1.534	3.87	5.937
[5] 16T Hybrid	16	7.27	2.506	0.978	2.451	2.397
[8] 10-T	10	**5.12**	**2.34**	5.95	13.923	82.84
[3] FA-3	14	6.32	3.053	**0.344**	**1.05**	**0.361**

Performed in **ULV of 0.2V** for 45nm technology

V. COMPARISON

An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined

TABLE VII
THE INPUTS AND SIGNALS OF THE FUNCTION TABLE OF FA-3

A B C_{in}	M1	M2	M3	M4	$A \oplus B$	M5	M6	$A \odot B$	M7	M8	M9	M10	M11	M12	M13	M14
1: 0 0 0	ON	OFF	ON	OFF	V_T(M3)	ON	OFF	1	ON	OFF	OFF	ON	ON	ON	OFF	ON
2: 0 0 1	ON	OFF	ON	OFF	V_T-V_T(M3)	ON	OFF	1	OFF	ON	OFF	ON	ON	ON	OFF	ON
3: 0 1 0	OFF	ON	ON	OFF	1	OFF	ON	0	ON	OFF	ON	OFF	OFF	OFF	ON	OFF
4: 0 1 1	OFF	ON	ON	OFF	1	OFF	ON	0	OFF	ON	ON	OFF	OFF	OFF	ON	OFF
5: 1 0 0	ON	OFF	OFF	ON	V_{DD}-V_T(M4)	OFF	ON	0	OFF	ON	ON	OFF	OFF	OFF	ON	OFF
6: 1 0 1	ON	OFF	OFF	ON	V_{DD}-V_T(M4)	OFF	ON	0	OFF	ON	ON	OFF	OFF	OFF	ON	OFF
7: 1 1 0	OFF	ON	OFF	ON	0	ON	OFF	1	ON	ON	OFF	ON	ON	ON	OFF	ON
8: 1 1 1	OFF	ON	OFF	ON	0	ON	OFF	1	OFF	ON	OFF	ON	ON	ON	OFF	ON

with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.

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VI. CONCLUSION

An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.

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