Report 1

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***Abstract*—The abstract goes here.**
***Index Terms*—1-bit Adder, Hybird Adder, CMOS,**

I. Introduction

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An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.

in section 2, xxx will be discussed...

II. FA-1: XOR-XNOR-based Hybrid Full Adder

A. Design

The FA-1[1] design, which was proposed in 2021, contains three modules to perform a 1-bit full adder operation. Firstly, an XOR-XNOR circuit will take original inputs A and B as its input and produce two signals, one is from the XNOR gate marked as S_{xnor_out} and the other is from the XOR gate marked as S_{xor_out}. Then, a TG-based circuit as the second module will take both signal and the input carry C_{in} to calculate the Sum while a third module will then use the C_{in} along with A, B and signals S_{xnor_out}, S_{xor_out} to generate the carry C_{out}.

Fig. 1 presents the block diagram of the design.

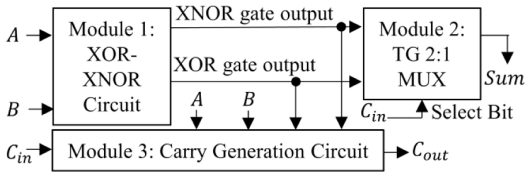

Fig. 1. Block Diagram Of FA-1

1) Module 1: XOR-XNOR Circuit Design

The circuit consists of 10 transistors as is shown in Fig. 2.

For all the possible A, B inputs, table I presents all the output patterns also the responsible transistors within the circuit. As the table presented, it is clear that at least one transistor path can provide full swing output to prevent threshold voltage loss.

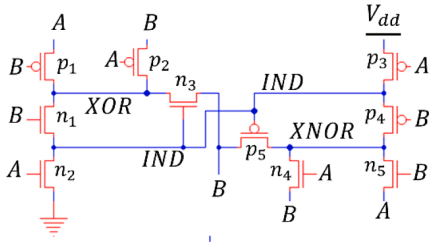

Fig. 2. XOR-XNOR Circuit

2) Module 2: Sum Generation Circuit

From the Table II, two paths for the Sum generation can be concluded:

when C_{in} = 0:

$$Sum = A \oplus B$$

when C_{in} = 1:

$$Sum = A \odot B$$

For input selection, a 2:1 Multiplexer(2:1 MUX) based on Transmission Gate(TG) has been used for the Sum generation.

As is given in Fig. 3, two TGs are used for implementing 2:1 MUX logic and with this manner, the Sum generation circuit can also provide full swing output.

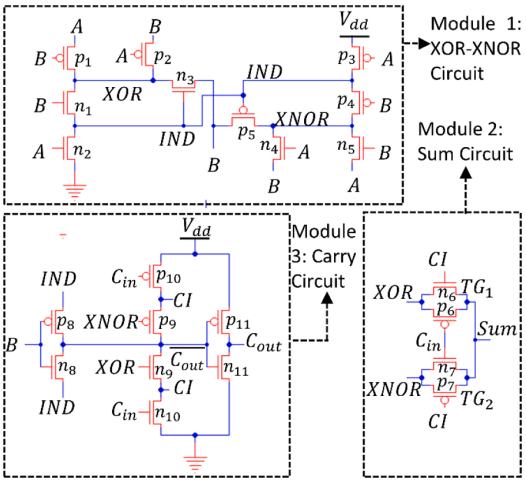

Fig. 3. FA-1 Circuit

3) Module 3: Carry Generation Circuit

As per Fig. 3, the $Carry$ generation circuit uses a CCMOS logic-based inverter at the output. With this logic, the output

TABLE I
OPERATION TABLE OF THE XOR-XNOR CIRCUIT

XOR Circuit					
	Input		**Output Transistor Path**		**Output**
Pattern no.	A	B	Full Swing Transistor Path	Non-Full Swing Transistor Path	Output Signal/logic
1.	0	0	n_3	p_1/p_2	$B/0$
2.	0	1	p_2	n_1/n_3	$B/1$
3.	1	0	p_1	None	$A/1$
4.	1	0	n_1 and n_2	None	0
XNOR Circuit					
	Input		**Output Transistor Path**		**Output**
Pattern no.	A	B	Full Swing Transistor Path	Non-Full Swing Transistor Path	Output Signal/logic
1.	0	0	p_3 and p_4	None	1
2.	0	1	n_5	None	$A/0$
3.	1	0	n_4	p_4/p_5	$B/0$
4.	1	0	p_5	n_4/n_5	$B/1$

TABLE II
TRUE-FALSE TABLE OF FA

	Inputs		**Outputs**	
C_{in}	A	B	C_{out}	Sum
0	0	0	0	0
	0	1	0	1
	1	0	0	1
	1	1	1	0
1	0	0	0	1
	0	1	1	0
	1	0	1	0
	1	1	1	1

voltage level of this circuit is either V_{dd} or G_{nd} level. It is a good design for the extensibility of the circuit since the design of the carry generation logic is the most important factor of the scalability of the wide word length adders.

B. Discussion

FA-1 shows impressive improvements compared to many other FAs. The presenters are intended to solve the voltage degradation issue with the hybrid logic-based design, hence they design the XOR-XNOR-based circuit to produce full swing output for its next stage and choose TG for implementing the sum generation circuit.

Finally, for the purpose of high-speed calculations and good scalabilities, they apply the CCMOS technique at the output terminial. The designed carry generation circuit can be extended to multiple bits adder structures with no additional voltage level restoring buffers. Furthermore, this logic can reduce the carry chain delay with involving just one pull-up and pull-down transistors.

As for the area overhead, a total of 22 transistors are used to produce this FA, namely, 10 on module one, 4 on module 2, and 8 on module 3.

According to the presenters' simulation using 45nm technique and 1 voltage supply on 1-bit FA, compare with the conventional CMOS FA[2] and other recent FA designs[3], [4], this design achieves many improvements which can be shown in the Table III.

Again, based on the presenters' simulation of the word-length adder architecture[1], the FA-1 continues to rank first in these performance comparisons with its scalability advantages.

III. DESIGN B

An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.

IV. DESIGN C

An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.

V. COMPARISON

An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined

TABLE III
PART OF THE 1-BIT FA PERFORMANCE INVESTIGATION PERFORMED BY THE DESIGNERS OF FA-1

FA Cell	**TC**	**Performance**					**Improvements with Respect to CCMOS FA**				
		Area(μm^2)	AP(μW)	PD(ps)	ADP(μm^2.ps)	PDP(αJ)	Area(٪)	AP(٪)	PD(٪)	ADP(٪)	PDP(٪)
CCMOS[2]	28	10.13	1.28	60.3	610.84	77.18	0.00	0.00	0.00	0.00	0.00
Kandpal's[3]	20	9.18	0.92	54.06	496.27	49.74	9.38	28.13	10.35	18.76	35.55
Sanapala's[4]	14	**7.38**	0.75	56.7	415.45	42.53	**27.15**	**41.41**	5.97	31.99	44.90
FA-1[1]	22	8.17	0.85	**38.5**	**267.40**	**32.73**	19.35	33.59	**36.15**	**56.22**	**57.59**

with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.

VI. CONCLUSION

An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.

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