Survey Of Several Recent Full Adder Designs

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***Abstract*—**
***Index Terms*—Full Adder, 1-bit Adder, Hybrid Adder, CMOS,**

I. Introduction

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A 22T XOR-XNOR-based hybrid full adder design [1] has been proposed in 2021 which uses an XOR-XNOR module combined with the sum-generation module which uses TG technique and the carry-generation module which use CCMOS technique.

A 18T hybrid full adder design [2] has been proposed in 2020. This design is also a three modules cell based on a XOR-XNOR circuit. With this fundamental circuit, two 4T circuits, which use the GDI technique and TG technique respectively, are driven to generate sum and carry.

In section II, the 22T XOR-XNOR-based hybrid FA is discussed as FA-1; Then in section III, the 18T hybrid FA is discussed as FA-2;

II. FA-1: XOR-XNOR-based Hybrid FA

A. Design

The FA-1 [1] design contains three modules to perform a 1-bit full adder operation. Firstly, an XOR-XNOR circuit will take original inputs A and B as its input and produce two signals, one is from the XNOR gate marked as S_{xnor_out} and the other is from the XOR gate marked as S_{xor_out}. Then, a TG-based circuit as the second module will take both signal and the input carry C_{in} to calculate the Sum while a third module will then use the C_{in} along with A, B and signals S_{xnor_out}, S_{xor_out} to generate the carry C_{out}.

Fig. 1 presents the block diagram of the design.

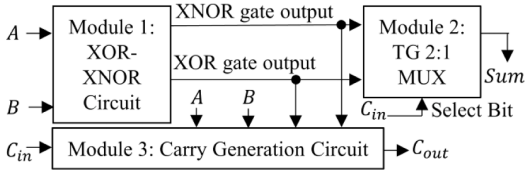

Fig. 1. Block Diagram of FA-1

1) Module 1: XOR-XNOR Circuit

The circuit consists of 10 transistors as is shown in Fig. 2.

For all the possible A, B inputs, table I presents all the output patterns also the responsible transistors within the circuit. As the table presented, it is clear that at least one transistor path can provide full swing output to prevent threshold voltage loss.

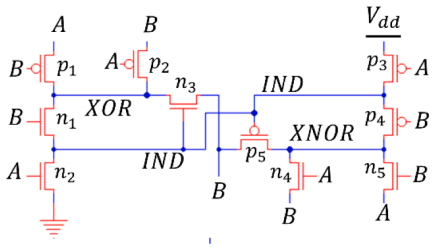

Fig. 2. XOR-XNOR Circuit of FA-1

2) Module 2: Sum Generation Circuit

From the Table II, two paths for the Sum generation can be concluded:

when C_{in} = 0:

$$Sum = A \oplus B$$

when C_{in} = 1:

$$Sum = A \odot B$$

For input selection, a 2:1 Multiplexer(2:1 MUX) based on Transmission Gate(TG) has been used for figuring the Sum.

As is given in Fig. 3, two TGs are used for implementing 2:1 MUX logic and with this manner, the Sum generation circuit can also provide full swing output.

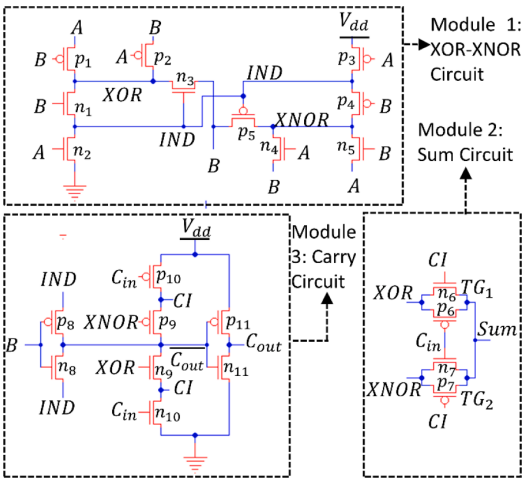

Fig. 3. FA-1 Circuit

TABLE I
OPERATION TABLE OF THE XOR-XNOR CIRCUIT OF FA-1

XOR Circuit					
	Input		**Output Transistor Path**		**Output**
Pattern no.	A	B	Full Swing Transistor Path	Non-Full Swing Transistor Path	Output Signal/logic
1.	0	0	n_3	p_1/p_2	$B/0$
2.	0	1	p_2	n_1/n_3	$B/1$
3.	1	0	p_1	None	$A/1$
4.	1	0	n_1 and n_2	None	0
XNOR Circuit					
	Input		**Output Transistor Path**		**Output**
Pattern no.	A	B	Full Swing Transistor Path	Non-Full Swing Transistor Path	Output Signal/logic
1.	0	0	p_3 and p_4	None	1
2.	0	1	n_5	None	$A/0$
3.	1	0	n_4	p_4/p_5	$B/0$
4.	1	0	p_5	n_4/n_5	$B/1$

TABLE II
TRUE-FALSE TABLE OF FA

Inputs			**Outputs**	
C_{in}	A	B	C_{out}	Sum
0	0	0	0	0
	0	1	0	1
	1	0	0	1
	1	1	1	0
1	0	0	0	1
	0	1	1	0
	1	0	1	0
	1	1	1	1

3) Module 3: Carry Generation Circuit

As per Fig. 3, the Carry generation circuit uses a CCMOS logic-based inverter at the output. With this logic, the output voltage level of this circuit is either V_{dd} or G_{nd} level. It is a good design for the extensibility of the circuit since the design of the carry generation logic is the most important factor of the scalability of the wide word length adders.

B. Discussion

FA-1 shows impressive improvements compared to many other FAs. The presenters are intended to solve the voltage degradation issue with the hybrid logic-based design, hence they design the XOR-XNOR-based circuit to produce full swing output for its next stage and choose TG for implementing the sum generation circuit.

Finally, for the purpose of high-speed calculations and good scalabilities, they apply the CCMOS technique at the output terminial. The designed carry generation circuit can be extended to multiple bits adder structures with no additional voltage level restoring buffers. Furthermore, this logic can reduce the carry chain delay with involving just one pull-up and pull-down transistors.

As for the area overhead, a total of 22 transistors are used to produce this FA, namely, 10 on module one, 4 on module 2, and 8 on module 3.

According to the presenters' simulation on 1-bit FA, compare with the conventional CMOS FA [3] and other recent FA designs [4], [5], [6], this design achieves many improvements which can be shown in the Table III.

Again, based on the presenters' simulations of the word-length adder architecture [1], the FA-1 continues to rank first in these performance comparisons with its scalability advantages, , especially on 16-bit and 32-bit.

III. FA-2: 18T HYBRID FA

A. Design

The FA-2 [2] design contains three module. Same as FA-1 [1], the module 1 of the FA-2 is an XOR-XNOR circuit that sending out two signals to drive Module 2 and Module 3 for the calculation of Sum and $Carry$.

Module 1 from FA-2 first take A and B and produce signal H (result of $A \oplus B$) and signal $\overline{H}$ (result of $A \odot B$). Module 2 then take H and C_{in} to calculate the Sun ($C_{in} \oplus H$). Module 3 finally figure the C_{out} out from the input A and C_{in} also count in the selection between H and $\overline{H}$.

The expressions of those outcomes can be:

$$Sum = H\overline{C_{in}} + \overline{H}C_{in} = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = HC_{in} + \overline{H}A \quad (2)$$

1) Module 1: XOR-XNOR Circuit

The structure of module 1 is presented in Fig. 4. To avoid the lack of voltage level, a feedback loop is attached to the XOR output and XNOR output for reaching the power required to drive the next two modules. So it use a pMOS transistor as Mpf, a nMOS transistor as Mnf. Any weak logic signal produced by the XOR gate or the XNOR gate (when $A = B$) will be handle by the feedback loop and obtains perfect logic signal at the H or $\overline{H}$ output. For example, if $A = B = 0$, weak logic 0 will be produce at the XOR gate as H, but it still turns

TABLE III
SIMULATIONS PERFORMED BY THE DESIGNERS OF FA-1

FA Cell	TC	Performance					Improvements with Respect to CCMOS FA				
		Area (μm^2)	AP (μW)	PD (ps)	ADP (μm^2.ps)	PDP (αJ)	Area(٪)	AP(٪)	PD(٪)	ADP(٪)	PDP(٪)
[3] CCMOS	28	10.13	1.28	60.3	610.84	77.18	0.00	0.00	0.00	0.00	0.00
[4] Bhattacharyya's	16	7.58	**0.62**	98.7	748.15	61.19	25.17	**51.56**	-63.68	-22.48	20.72
[5] Kandpal's	20	9.18	0.92	54.06	496.27	49.74	9.38	28.13	10.35	18.76	35.55
[6] Sanapala's	14	**7.38**	0.75	56.7	415.45	42.53	**27.15**	41.41	5.97	31.99	44.90
[1] FA-1	22	8.17	0.85	**38.5**	**267.40**	**32.73**	19.35	33.59	**36.15**	**56.22**	**57.59**

Performed in 1V for 45nm technology

ON the Mpf and then logic 1 passes to the Mnf, thus a perfect logic 0 is taken at the H.

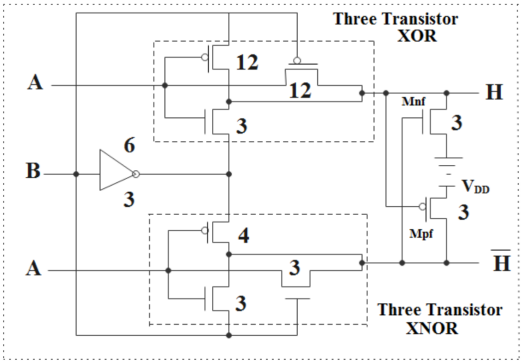

Fig. 4. Module 1 of FA-2

2) Module 2: Sum Generation Circuit

The structure of module 2 is presented in Fig. 5. Sum generate implementation of FA-2 is an XOR gate with Gate Diffusion Input technique. So it can generate the full swing output. When using GDI on the XOR gate, it is required that an inverter provide a perfect signal to the inputs. But since it retrieves such signal from module 1, the implementation of this module will only need 4 transistors to finish the task.

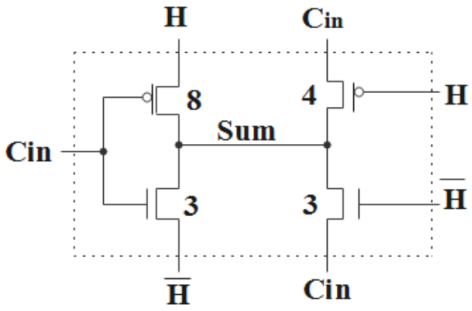

Fig. 5. Module 2 of FA-2

3) Module 2: Carry Generation Circuit

The structure of module 3 is presented in Fig. 6. The circuit is a 4 pass transistors(PT) 2-to-1 MUX, and it will provide a full swing output by a pMOS and an nMOS conducted in each of the input patterns. For instance, when H = A = 0, Mp1 and Mn2 turn on, a logic 0 goes through these transistors, C_{out} obtains perfect 0.

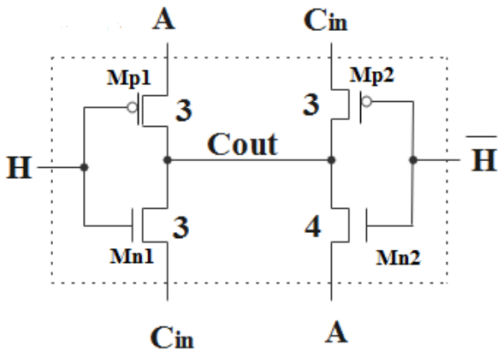

Fig. 6. Module 3 of FA-2

B. Discussion

FA-2 design is a lean logic cell for the addition operation. The designers were well aware of the problems such as bad performance happens at low supply voltages and the stability of the produced output at different loading conditions. The design combined feedback loop design, GDI design, and PT technique all together to solve these problems.

With respect of area overhead, 18 transistors are used to bulid this cell. 10 on module 1, 4 on module 2, and 4 on module 3.

As simulations performed by the designers which presented in Table IV, FA-2 shows its advantages on speed and PDP aspects compared with one old hybrid CMOS FA cell and one hybrid FA.

TABLE IV
SIMULATIONS PERFORMED BY THE DESIGNERS OF FA-2

FA Cell	TC	Performance		
		AP(μW)	PD(ps)	PDP(fJ)
[7] Hybrid CCMOS	24	6.21	143	0.888
[4] Bhattacharyya's	16	1.1766	91.3	0.107
[2] FA-2	18	**1.104**	**85.22**	**0.0941**

Performed in 1.2V for 90nm technology

IV. FA-3: GDI-BASED HYBRID FA

An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.

V. COMPARISON

An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.

VI. CONCLUSION

An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.An XOR-XNOR-based hybrid full adder design has been proposed[1] which uses an XOR-XNOR module combined with the carry-generation module and the sum-generation module. As the designers discussed, it is a scalable and full-swing FA with some performance improvements compared with several existing state-of-the-art FAs.

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