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Name: Dallon MEClair

Grade:

2) [20] The following truth table represents a Full Binary Adder. The two binary inputs are A and B and the carry from previous stage is Cin. The sum bit is S and the carry for the next stage is Cout.

A	В	Cln	Sum	Cout
0	0	0	0	0
0	0	1	02	0
0	1	0	1).	0
0	1	1	0	(1)
1	0	0	(1)	0
1	0	1	0	1
1	1	0	0	1
1	1	1		•

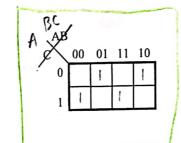
2.a) [2] Write the Boolean expression as a sum of Minterms:

Sum = f (A, B, Cin) = $M_1 + M_2 + M_4 + M_5 = \overline{ABC} + \overline{ABC} + \overline{ABC} + \overline{ABC}$ Cout = f (A, B, Cin) = $M_2 + M_5 + M_6 + M_5 = \overline{ABC} + \overline{ABC} + \overline{ABC} + \overline{ABC}$

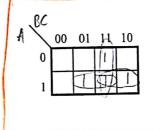
2.b) [2] Optimize the above functions using K-maps: Sum = f (A, B, Cin) = ABC + ABC + ABC

Cout = f (A, B, Cin) = _





Cannot be Optimized!

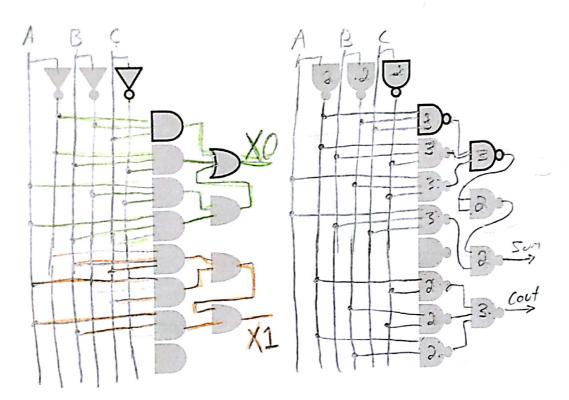


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- 2.c) [2] Implement the above two optimized functions as a 3-input 2-output NOT-AND-OR network:
- 2.d) [2] Convert the above network to all NAND gates:



- 2.e) [4] Build the above all-NAND circuit using the 7400 and 7410 logic chips (maximum 4 chips) on your breadboard and then connect it to your test platform to test it. Use 3 logic switches as inputs and 2 LEDs as outputs. You need to test all 8 different input combinations of the inputs.
 - Hint: Leave room on your breadboard for the 16-pin 74283.
- 2.f) [6] Connect your all-NAND 1-bit full adder to the standard 4-bit full adder (Chip 74283) making your adder the LSB of the 5-bit resulting adder. Use the following diagram to plan your wiring. To simplify the testing procedure, tie the two MSB bits to low level. Then, use 7 logic switches as inputs and 4 LEDs as outputs. To test your circuit, try as many input combinations as possible.
- 2.g) [2] You can verify the circuit design/behavior (the 5-bit adder) by implementing the circuit using Quartus. You may wish to do this before you actually build the circuit on the breadboard.

