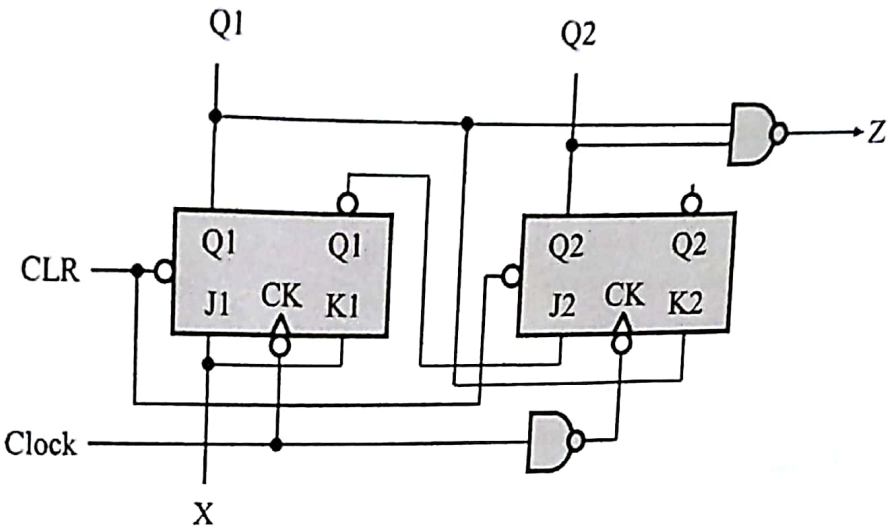
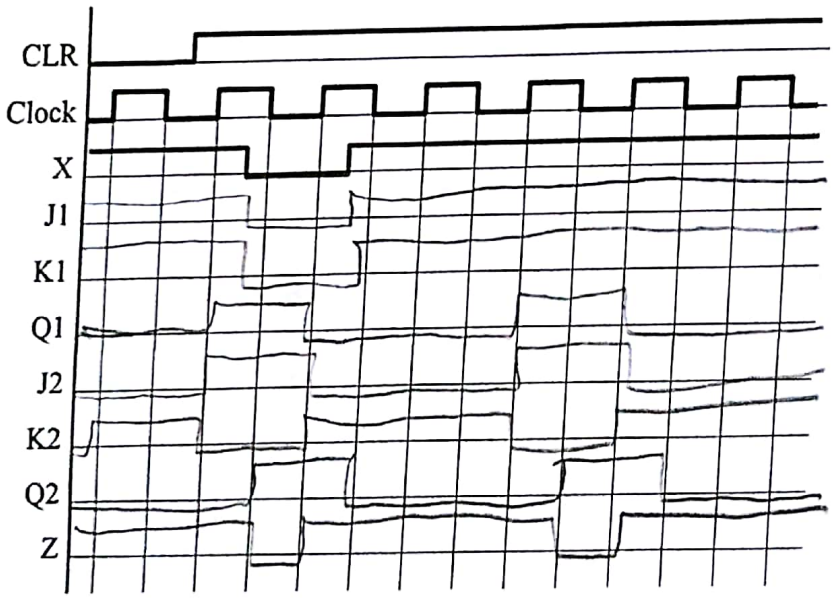
4) [20] Consider the following sequential circuit with two negative-edge-triggered JK flip-flops.



4.a) [2] Complete the timing diagram for the above circuit.



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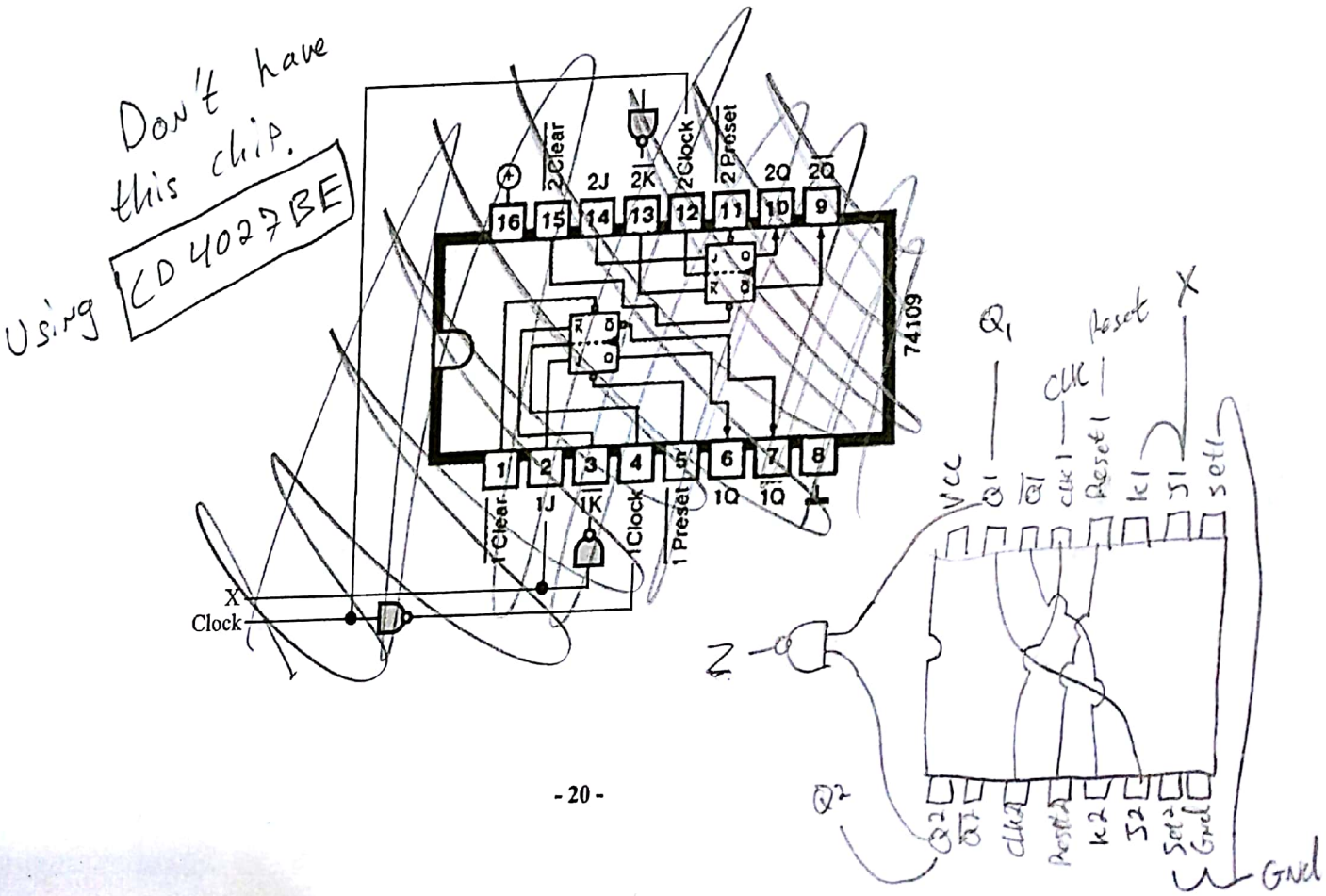
4.b) [8] Build the above circuit using the 74109 dual JK flip-flop logic chip on your breadboard and then connect it to your test platform to test it. Use the chip block diagram below to plan for your wiring. Use 2 logic switches for inputs X and CLR, and one pulse switch for the Clock. Use 4 LEDs to observe X=J1= K1, Q1=J2*=K2, Q2, and Z=Q1*+Q2*. Tie the PRE inputs to high as they are active low.

Observation: If X is kept high, Q1 will toggle at every Negative Clock transition because J1=K1=X=1 (toggle mode).

Warning 1: Note that for 74109 JK package, the K input of the flip-flops is internally inverted so you need to invert it outside the chip by using external inverters. Or simply, in case of 1K, connect it to X*, and in case of 2K, connect it to Q1* (just like 2J).

Warning 2: Note that for 74109 JK package, the Clock input of the flip-flops is actually positive-edge triggered, not negative as we have in the schematics. Therefor for the implementation, use the inverter to invert your Clock input going to 1Clock instead of 2Clock.



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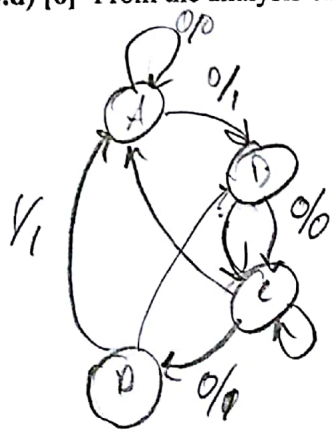
4.c) [4] You can verify the circuit design/behavior by implementing the circuit using Quartus. You may wish to do this before you actually build the circuit on the breadboard.

4.d) [6] From the analysis of the circuit above, draw the state table and the state graph.



	Q	I	Z	Q+	J_2 K_2	J_1 K_1
A	00	1	1	00	0 X	0 X
		0		01	0 X	1 X
B	01	1	1	11	1 X	X 0
		0		10	1 X	X 1
C	10	1	1	11	X 1	0 X
		0		10	X 1	1 X
D	11	1	0	00	X 0	X 0
		0		01	X 0	X 1