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CS382-B

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SleepyU Manual

Naming Conventions:

- BOOST: ADD
- FALL: SUB
- FETCH: LDR
- TUCK: STR
- Rd: destination register
- Rs: source register
- Rt: target register
- Rm: operand register 1
- Rn: operand register 2

Instructions (8-bit):

- [aa bb cc dd]:
 - 2-bit opcode: aa
 - 2-bit destination register: bb
 - 2-bit source/operand register: cc
 - 2-bit target/operand register: dd
- BOOST (BOOST Rd, Rm, Rn):
 - 2-bit opcode: {00}

- 2-bit destination register: {00, 01, 10, 11}
 - 2-bit operand register 1: {00, 01, 10, 11}
 - 2-bit operand register 2: {00, 01, 10, 11}
- FALL (FALL Rd, Rm, Rn):
 - 2-bit opcode: {01}
 - 2-bit destination register: {00, 01, 10, 11}
 - 2-bit operand register 1: {00, 01, 10, 11}
 - 2-bit operand register 2: {00, 01, 10, 11}
 - FETCH (FETCH Rd, [Rs, Rt]):
 - 2-bit opcode: {10}
 - 2-bit destination register: {00, 01, 10, 11}
 - 2-bit source register: {00, 01, 10, 11}
 - 2-bit target register: {00, 01, 10, 11}
 - TUCK (TUCK Rd, [Rs, Rt]):
 - 2-bit opcode: {11}
 - 2-bit destination register: {00, 01, 10, 11}
 - 2-bit source register: {00, 01, 10, 11}
 - 2-bit target register: {00, 01, 10, 11}