DC Lab Guide part2

Object:

After complete this lab student should be able to:

- Read timing constraints and fill the blanks in tcl file.
- Apply the constraints to a design.

Three files contained in this tutorial:

Name	Description
Design.v	An example code gate level circuit
dc.tcl	Tcl file which need to be used in DC
osu05_stdcell.db	Tech library file used in DC

Timing constrains:

Clock definition:	1.Set clock frequency to 333.33Mhz 2. Maximum external clock latency is 700ps 3. Maximum insertion delay from clock port to all register clock pin is 300ps. 4. Apply 150ps setup margin to the clock period. 5. The worst case rise/fall transition time of any clock is 120ps.
Input delays:	1. The maximum input delay of ports data1 and data2 are 450ps 2. The maximum input delay of ports Cin1 and Cin2 are 300ps
Output delays:	1. The maximum output delay of out1 is 500ps 2. The maximum output delay of out2 is 2.04ns 3. The maximum output delay of out3 is 400ps 4. The maximum output delay of out2 is 300ps