Project 1

Problem 1: (This question is not related to SystemVerilog)

Design a sequential circuit S1 with the following requirements
a) The combinational logic part for the next state function should contain at least 3 NOR gates, one XOR gate and 2 AND gates.
b) The number of the flip-flops should be at least 4.
c) The sequential circuit should have at least an output.
d) Make sure that your design be different from those used by other students. If your design is identical to a design used by other students, you will be asked to revise your design and redo the work.
Instructions:
1) Draw your sequential circuit S1.
2) Create the next state function table for S1.
3) Draw the state transition graph of S1 including all the POSSIBLE states.
4) Figures should be plotted by using a professional software tool. Scanned or cut/paste hand drawn figures and writing are not acceptable.

Problem 2: Given an input of a 9-bit Boolean vector M, write a SystemVerilog (SV) model for the detector specified as follows. If the number of the logic high bits of M equals the first digital of the PSU ID number of one member of your group, the detector will give logic high, otherwise low.
2.1) Write an SV algorithmic model (always_comb) of the detector having a delay of 10ns.
2.2) Write an SV dataflow model (continuous assignments) of the detector having a delay of 10ns.

Using the same testbench to simulate both designs. Your testbench should cover 512 combinations of the 9-bit vector, list all matched result in a log file with "#RUN_TIME, VECTOR STRING, MATCHED"

Problem 3: Write an SV behavioral model of a 2^n to n priority encoder.

Problem 4: Write an SV behavioral model for a 16-bit carry look ahead adder.

Problem 5: Write an SV model for an 8-bit Wallace tree multiplier.

Problem 6: 1) Write an SV model of a circuit whose 32-bit output is formed by shifting its 32-bit input three positions to the right and filling the vacant positions with the bit that was in the MSB before the shift occurred (shift arithmetic right). 2) Write an SV model of a circuit whose 32-bit output is formed by shifting its 32-bit input three positions to the left and filling the vacant positions with 0 (shift logical left).

Project Instructions:

1. Write a SystemVerilog (SV) model for the above problem I (I>1). Verify the correctness of your design with your testbench using a SystemVerilog simulator.
2. You should use the new SV statements whenever possible. For instance, when modeling combinational circuits with **always** statements, use **always_comb**.
3. Turn in your report and code to the D2L by the deadline.
4. Your report must contain at least:
   - The SV code with Legible result from your testbench
   - Your code should be packaged and organized with the related task name.
5. Only one report is needed for each group. Indicate your name and email on the first page of your report.