5.1.10 Error Detection and Recovery Methods for SDR

The error detection and recovery methods specified in this Section are provided in order to avoid fatal conditions when errors occur. A set of required methods is specified for I3C Target Devices, and a separate set of required methods is specified for I3C Controller Devices. Origins for all of these SDR Error Types are shown in ***Figure 164*** through ***Figure 167***.

5.1.10.1 SDR Error Detection and Recovery Methods for I3C Target Devices

The Error Types summarized in ***Table 59*** shall be supported for all I3C Target Devices. Each Error Type is further explained in a sub-section below the table.

Note:

In previous versions of the I3C Specification, these Error Types for I3C Target Devices were named "S0", "S1", etc. The purpose, detection methods, and recovery methods for these Error Types are unchanged.

Table 59 SDR Target Error Types

Error Type	Description	Error Detection Method	Error Recovery Method
TE0	**Invalid Broadcast Address/W** (7'h7E/W) or **Dynamic Address/RnW after DA assignment**	Detect any of the following: 7'h3E / W 7'h5E / W 7'h6E / W 7'h76 / W 7'h7A / W 7'h7C / W 7'h7F / W 7'h7E / R[1]	a. Enable HDR Exit Detector and ignore all other patterns b. (Optional) If both SCL and SDA stay at High level for a period greater than 60 µs, then enable STOP or START detector to exit from the TE0/TE1 error situation.
TE1	**CCC Code**	Parity Check, using T-Bit	a. Enable HDR Exit Detector and neglect other patterns. b. (Optional) If both SCL/SDA stay at High level for a period greater than 60 µs, then enable STOP or START detector to exit from the TE0/TE1 error situation.
TE2	**Write Data**	Parity Check, using T-Bit	Enable STOP or Repeated START detector and neglect other patterns.
TE3	**Assigned Address during Dynamic Address Arbitration**	Parity Check, using PAR Bit	Generate NACK (after PAR), then wait for another Repeated START and 7E/R to re-transmit the Provisioned ID.
TE4	**7'h7E/R missing after Sr during Dynamic Address Arbitration**	Detect 7'h7E/R missing after Sr during Dynamic Address Arbitration	Generate NACK (after 7'h7E/R), then enable STOP or Repeated START Detector and ignore all other patterns
TE5	**Transaction after detecting CCC**	Detect illegally formatted CCC	Generate NACK (after Target Address), then enable STOP or Repeated START Detector and ignore all other patterns
TE6 (optional)	**Monitoring Error**	Target detects (through monitoring) that transmitted Data differs from what it intended to transmit (Does not apply during Dynamic Address Arbitration)	Stop the transmission, then enable STOP or Repeated START Detector (per Read type) and ignore all other patterns
DBR (optional)	**Dead Bus Recovery**	Controller acting as Target detects that the I3C Bus is no longer being driven by a Controller	Controller acting as Target retakes control of the I3C Bus, becoming Active Controller

Note:

1. *In the ENTDAA mode, "7'h7E / R" is excluded from the TE0 error definition.*

5.1.10.1.1 Error Type TE0

If an error occurs during Broadcast Address/W or Dynamic Address/RnW after a Dynamic Address is assigned, then the Target will be unable to distinguish whether the transfer is a CCC transfer or a Private RnW transfer. For example, in the case of an ENTHDR CCC transfer the Target is not able to know that the I3C Bus has changed to HDR Mode. A potentially fatal situation could ensue if this case is not detected and handled, because the Target might become confused by seeing many STARTs and STOPs as illustrated in ***Figure 88***, and might attempt to interpret the HDR transfer as though the I3C Bus were still in SDR Mode.

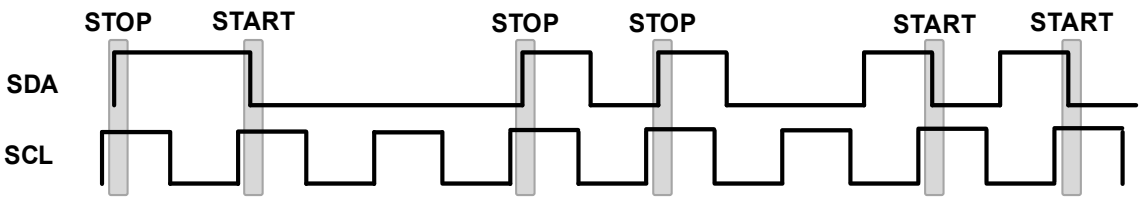

Figure 88 Example Waveform for Error Type TE0

In order to avoid this situation, the Controller shall not use any of the possible error case Addresses: 7'h7F, 7'h7C, 7'h7A, 7'h76, 7'h6E, 7'h5E and 7'h3E.

- The Controller shall not assign any of these Addresses to any Target as a Dynamic Address (or a Group Address, if supported) per the I3C Target Address restrictions in ***Table 8*** (see ***Section 5.1.2.2.5***).
- The Controller shall not use any of these Addresses in an I3C Address Header with the RnW bit of 1'b0, because the Target cannot distinguish such an I3C Address Header from a write to the Broadcast Address (i.e., 7'h7E/W) that has a single bit error.

Except during a Dynamic Address Arbitration procedure, the Target shall consider receipt of any of these restricted Addresses (i.e., 7'h7F/W, 7'h7C/W, 7'h7A/W, 7'h76/W, 7'h6E/W, 7'h5E/W and 7'h3E/W), or the receipt of 7'h7E/R, as an error per the following conditions:

- The Target shall always use its Error Type TE0 detector after a Dynamic Address has been assigned, to monitor the I3C Address Header for SDR Mode transfers.
  - This generally applies to any I3C Address Header that follows either a START or a Repeated START (see ***Figure 164***, ***Figure 165***, and ***Figure 166***).
  - However, this shall not apply during the Dynamic Address Assignment procedure if the Controller uses the ENTDAA CCC (per ***Section 5.1.4.2***). If this occurs, then the Target shall use its Error Type TE4 detector instead (per ***Section 5.1.10.1.5***) until the end of the Dynamic Address Assignment procedure (see ***Figure 167***).

If the Target's Error Type TE0 detector detects such a single bit error in an I3C Address Header, then the Target shall ignore the rest of the signal until either:

- The Target detects the HDR Exit Pattern; or
- Optional: The Target detects that both SCL and SDA stay High for a period greater than 60 µs (see ***Section 5.1.10.1.9***).

  Note:

  The second method is optional, i.e., Target Devices are not required to support it. If this method is supported, then the Target shall enable its STOP or START detector to exit from the Error Type TE0 state. If supported, then this method may also be used for Error Type TE1.

5.1.10.1.2 Error Type TE1

If the Target detects a parity error during a CCC code, then the Target will not be able to know that the I3C Bus has changed to HDR Mode if the CCC is ENTHDR. This is similar to the situation in Error Type TE0. In order to avoid this situation, if the Target detects a parity error during a CCC code, then the Target shall ignore the rest of the signal, until:

Either:

- The Target detects the HDR Exit Pattern,

Or:

- Optional: The Target detects that both SCL and SDA stay High for a period greater than 60 µs (see ***Section 5.1.10.1.9***).

  Note:

  The second method is optional, i.e., Target Devices are not required to support it. If this method is supported, then the Target shall enable its STOP or START detector to exit from the Error Type TE1 state. If supported, then this method may also be used for Error Type TE0.

5.1.10.1.3 Error Type TE2

If the Target detects a parity error during Write Data, then the Target shall wait for STOP or Repeated START.

If the Target detects this error after receiving a CCC, then the Target shall:

Either:

1. Retain the CCC state until the Target detects the end of CCC command (i.e., when the Target is recovered by the Repeated START),

Or:

2. Disregard everything until the STOP.

5.1.10.1.4 Error Type TE3

If the Target detects a parity error in the PAR Bit of the Assigned Address during a Dynamic Address Arbitration procedure, then the Target shall generate NACK (after PAR) and then wait for another Repeated START and 7E/R to re-transmit the Provisioned ID.

5.1.10.1.5 Error Type TE4

During a Dynamic Address Arbitration procedure, if the Target detects any value other than 7'h7E/R following Repeated START, then the Target shall generate NACK (after 7'h7E/R) and then wait for STOP to exit the ENTDAA mode.

5.1.10.1.6 Error Type TE5

If the Target detects an illegally formatted CCC, then the Target shall generate NACK (after the Dynamic Address) and then wait for STOP or Repeated START.

Examples of an illegally formatted CCC include:

- If the Target receives a matching Dynamic Address with Write during a Direct CCC that only has a Direct Read or Direct GET form (e.g., the GETBCR CCC)
- If the Target receives a matching Dynamic Address with Read during a Direct CCC that only has a Direct Write or Direct SET form (e.g., the SETGRPA CCC)

If the Target detects this error after receiving a CCC, then the Target shall either:

1. Retain the CCC state until the Target detects the end of CCC command (i.e., when the Target is recovered by the Repeated START), or else
2. Stop the CCC when the Target is recovered by the STOP.

Note:

This section does not provide all examples of illegally formatted CCCs.

Note:

If the Target detects a Direct CCC that is formatted correctly, but that is not supported, then the Target shall handle such CCCs, or unsupported Defining Bytes, as described in ***Section 5.1.9.2.2****.*

In an HDR Mode CCC, the Target would wait for the CCC to end as described in ***Section 5.2.1.2.1****,* ***Figure 98****.*

5.1.10.1.7 Error Type TE6 (Optional)

If an error occurs in the RnW Bit of the Address Header, then the Target might believe that it is responding to a Read, when what the Controller actually intends to initiate is a Write. If this happens, then the Write Data from the Controller might conflict with the Read Data from the Target.

The Target should always monitor the Data it transmits for Read transactions. If the Target does so, then if the monitored Data differs from the Data the Target intended to transmit, the Target shall consider this condition to be an error.

Note:

The Controller should also monitor the Data it transmits. If this condition happens due to a Target's misinterpretation of the RnW bit during an intended Write transfer, then the Controller should also detect this condition as Error Type CE1 (see ***Section 5.1.10.2.2****).*

The Target shall not consider this condition to be an example of Error Type TE6 during the Arbitration round of a Dynamic Address Assignment procedure (i.e., when the Controller has sent the ENTDAA CCC) while the Target is attempting to drive its Provisioned ID, BCR and DCR (see ***Section 5.1.4.2****).*

If the Target detects such an error during an intended Private Write transfer (i.e., when the Target believes it is responding to a Private Read transfer), then it shall stop the transmission, allow the Controller to finish, and then wait for STOP or Repeated START.

If the Target detects such an error during an intended Direct SET or Direct Write CCC (i.e., when the Target believes that it is responding to a Direct GET or Direct Read CCC), then the Target shall stop the transmission, allow the Controller to finish, and then either:

1. Retain the CCC state until the Target detects the end of CCC command (i.e., when the Target is recovered by the Repeated START), or else
2. Stop the CCC when the Target is recovered by the STOP.

5.1.10.1.8 Error Type DBR (Optional)

This error allows a Controller-capable Device that is acting as a Target (i.e., a Secondary Controller) to regain control of a dead Bus (i.e., where the Active Controller has stopped working for whatever reason). This works both for a Primary Controller acting as Target (i.e., while a Device that initialized as a Secondary Controller is acting as Active Controller), and for a Secondary Controller acting as a Target.

The general model is that when the Controller acting as Target pulls SDA Low to request an IBI or CRR, it may measure the time before SCL goes Low (i.e., in response to this START Request). If SCL does not go Low in 50 ms (t_{CAS} maximum for Activity State 3), then the Controller acting as a Target may take action to take over control of the Bus and become the new Active Controller.

The steps are as follows:

1. The Controller acting as Target pulls SDA Low to initiate an IBI or CRR.
   a. It starts a timer.
2. If 50 ms has elapsed without SCL going Low, then the Controller acting as a Target assumes that the former Active Controller is not operational.
   a. If SCL is pulled Low before 50 ms, then all is well and Error Type DBR shall not apply.
   b. Otherwise, Error Type DBR applies and as a result the Target acting as Controller may start a transition to Controller mode.
3. Once in Controller mode, the Device shall verify that SCL is still High, and if so, pull SCL Low to complete a START.
   a. If SCL is not High by the time the Device is a Controller, then the Device must switch back to Target mode, as Error Type DBR no longer applies. This might occur due to another Controller-capable Device (i.e., a Secondary Controller) having taken control of the Bus first.
4. After the START, the Controller may wish to check the status of the Targets.
   a. It may also initiate an ENTDAA sequence to see whether any Devices need a Dynamic Address to be assigned (see ***Section 5.1.4.2***).
   b. If available, the last DEFTGTS information that might have been sent by a previous Active Controller (i.e., as a Broadcast CCC) should be used for proper Dynamic Address assignment.

Note:

A Controller-capable Device acting as Target may choose to monitor the Bus at all times. In the event that SDA is pulled Low by any Target, the Device may then measure the time waiting for SCL to be pulled Low. If 50 ms elapses without SCL being pulled Low, then it may start the Dead Bus Recovery process above at step 3.

If the former Active Controller eventually resumes operation and senses activity on SCL and/or SDA, then it must assume that it has lost the Controller Role to the new Active Controller.

Per **Section 5.1.11.4.1***, the Primary Controller shall use a similar procedure after a Full/Chip reset, to determine whether it should be the Active Controller of the Bus.*

5.1.10.1.9 Optional Recovery Method for Error Types TE0 and TE1

An I3C Target can recover from an Error Type TE0 or Error Type TE1 situation not only by detecting the HDR Exit Pattern, but also by monitoring the SCL and SDA lines. If the Target detects that both lines stay at High level for a period exceeding 60 µs, then the I3C Target can regard the Bus as operating in non-HDR mode. The I3C Target can then recover from the TE0 or TE1 situation, and wait for a STOP or a START to resume normal operation.

Note:

Regarding timing, HDR's slowest clock rate is 10 kHz (100 µs total cycle). The period 60 µs is derived by assuming that HDR (i.e., HDR-DDR Mode) will always keep an approximately even duty cycle, especially at very slow clock rates (since the only reason to go so slow is for long lines and/or large capacitive load on Bus lines). 60 µs represents 60% of the duty cycle, and therefore is a safe duration to wait when seeing both lines High.

The Target can start measuring the period whenever it detects that both SCL and SDA are at High level. There is no need to start timing this period at any particular signal pattern (for example, at the STOP).