ECE 310-001

Project #2 Report

Your Name Here

1. Snapshot of the RTL synthesized in Quartus.

|  |
| --- |
|  |

*Part 1: Fill in the synthesis results*

|  |
| --- |
| **Synthesis Results** |
| Number of logic elements  6,271 / 36,100 ( 17 % ) |
| Number of registers: 196 |
|  |
| Number of memory bits:  0 / 2,939,904 ( 0 % ) |
| Frequency the design can run at: |
| Do you see any synthesis errors? Why? ( One line explanation is fine )  Info: \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  Info: Running Quartus II 64-Bit Analysis & Synthesis  Info: Version 13.1.0 Build 162 10/23/2013 SJ Web Edition  Info: Processing started: Mon Nov 28 21:49:19 2022  Info: Version 13.1.0 Build 162 10/23/2013 SJ Web Edition  Info: Processing started: Mon Nov 28 21:49:19 2022  Info: Command: quartus\_map --read\_settings\_files=on --write\_settings\_files=off proj2 -c proj2  Info (20030): Parallel compilation is enabled and will use 16 of the 16 processors detected  Info (12021): Found 1 design units, including 1 entities, in source file reg.v  Info (12023): Found entity 1: registers  Info (12023): Found entity 1: registers  Info (12021): Found 1 design units, including 1 entities, in source file ram.v  Info (12023): Found entity 1: ram  Info (12023): Found entity 1: ram  Info (12021): Found 1 design units, including 1 entities, in source file proj2.v  Info (12023): Found entity 1: proj2  Info (12023): Found entity 1: proj2  Info (12021): Found 1 design units, including 1 entities, in source file path.v  Info (12023): Found entity 1: datapath  Info (12023): Found entity 1: datapath  Info (12021): Found 1 design units, including 1 entities, in source file ctr.v  Info (12023): Found entity 1: ctr  Info (12023): Found entity 1: ctr  Info (12021): Found 19 design units, including 19 entities, in source file alu.v  Info (12023): Found entity 1: my1bitmux  Info (12023): Found entity 2: muxand  Info (12023): Found entity 3: muxxor  Info (12023): Found entity 4: my16bitsmuxxor  Info (12023): Found entity 5: muxor  Info (12023): Found entity 6: muxnot  Info (12023): Found entity 7: my16bitmuxnot  Info (12023): Found entity 8: my1bithalfadder  Info (12023): Found entity 9: my1bitfulladder  Info (12023): Found entity 10: my4bitfulladder  Info (12023): Found entity 11: my4bitmux  Info (12023): Found entity 12: my4bitaddsub\_gate  Info (12023): Found entity 13: my16bitfulladder  Info (12023): Found entity 14: my16bitmux  Info (12023): Found entity 15: my16bitaddsub\_gate  Info (12023): Found entity 16: my16bitdivider  Info (12023): Found entity 17: multiplier  Info (12023): Found entity 18: myexp  Info (12023): Found entity 19: alu  Info (12023): Found entity 1: my1bitmux  Info (12023): Found entity 2: muxand  Info (12023): Found entity 3: muxxor  Info (12023): Found entity 4: my16bitsmuxxor  Info (12023): Found entity 5: muxor  Info (12023): Found entity 6: muxnot  Info (12023): Found entity 7: my16bitmuxnot  Info (12023): Found entity 8: my1bithalfadder  Info (12023): Found entity 9: my1bitfulladder  Info (12023): Found entity 10: my4bitfulladder  Info (12023): Found entity 11: my4bitmux  Info (12023): Found entity 12: my4bitaddsub\_gate  Info (12023): Found entity 13: my16bitfulladder  Info (12023): Found entity 14: my16bitmux  Info (12023): Found entity 15: my16bitaddsub\_gate  Info (12023): Found entity 16: my16bitdivider  Info (12023): Found entity 17: multiplier  Info (12023): Found entity 18: myexp  Info (12023): Found entity 19: alu  Info (12127): Elaborating entity "proj2" for the top level hierarchy  Info (12128): Elaborating entity "ram" for hierarchy "ram:ram\_ins"  Warning (10240): Verilog HDL Always Construct warning at ram.v(15): inferring latch(es) for variable "q", which holds its previous value in one or more paths through the always construct  Info (10041): Inferred latch for "q[0]" at ram.v(19)  Info (10041): Inferred latch for "q[1]" at ram.v(19)  Info (10041): Inferred latch for "q[2]" at ram.v(19)  Info (10041): Inferred latch for "q[3]" at ram.v(19)  Info (10041): Inferred latch for "q[4]" at ram.v(19)  Info (10041): Inferred latch for "q[5]" at ram.v(19)  Info (10041): Inferred latch for "q[6]" at ram.v(19)  Info (10041): Inferred latch for "q[7]" at ram.v(19)  Info (10041): Inferred latch for "q[8]" at ram.v(19)  Info (10041): Inferred latch for "q[9]" at ram.v(19)  Info (10041): Inferred latch for "q[10]" at ram.v(19)  Info (10041): Inferred latch for "q[11]" at ram.v(19)  Info (10041): Inferred latch for "q[12]" at ram.v(19)  Info (10041): Inferred latch for "q[13]" at ram.v(19)  Info (10041): Inferred latch for "q[14]" at ram.v(19)  Info (10041): Inferred latch for "q[15]" at ram.v(19)  Info (12128): Elaborating entity "datapath" for hierarchy "datapath:datapathproj"  Warning (10230): Verilog HDL assignment warning at path.v(107): truncated value with size 32 to match size of target (8)  Info (12128): Elaborating entity "alu" for hierarchy "datapath:datapathproj|alu:myalu"  Warning (10230): Verilog HDL assignment warning at alu.v(469): truncated value with size 32 to match size of target (16)  Warning (10240): Verilog HDL Always Construct warning at alu.v(456): inferring latch(es) for variable "Rout", which holds its previous value in one or more paths through the always construct  Info (10041): Inferred latch for "Rout[0]" at alu.v(459)  Info (10041): Inferred latch for "Rout[1]" at alu.v(459)  Info (10041): Inferred latch for "Rout[2]" at alu.v(459)  Info (10041): Inferred latch for "Rout[3]" at alu.v(459)  Info (10041): Inferred latch for "Rout[4]" at alu.v(459)  Info (10041): Inferred latch for "Rout[5]" at alu.v(459)  Info (10041): Inferred latch for "Rout[6]" at alu.v(459)  Info (10041): Inferred latch for "Rout[7]" at alu.v(459)  Info (10041): Inferred latch for "Rout[8]" at alu.v(459)  Info (10041): Inferred latch for "Rout[9]" at alu.v(459)  Info (10041): Inferred latch for "Rout[10]" at alu.v(459)  Info (10041): Inferred latch for "Rout[11]" at alu.v(459)  Info (10041): Inferred latch for "Rout[12]" at alu.v(459)  Info (10041): Inferred latch for "Rout[13]" at alu.v(459)  Info (10041): Inferred latch for "Rout[14]" at alu.v(459)  Info (10041): Inferred latch for "Rout[15]" at alu.v(459)  Info (12128): Elaborating entity "my16bitsmuxxor" for hierarchy "datapath:datapathproj|alu:myalu|my16bitsmuxxor:my16muxxor"  Info (12128): Elaborating entity "muxxor" for hierarchy "datapath:datapathproj|alu:myalu|my16bitsmuxxor:my16muxxor|muxxor:xor11"  Info (12128): Elaborating entity "my1bitmux" for hierarchy "datapath:datapathproj|alu:myalu|my16bitsmuxxor:my16muxxor|muxxor:xor11|my1bitmux:mux2"  Info (12128): Elaborating entity "my16bitaddsub\_gate" for hierarchy "datapath:datapathproj|alu:myalu|my16bitaddsub\_gate:my16add"  Info (12128): Elaborating entity "muxnot" for hierarchy "datapath:datapathproj|alu:myalu|my16bitaddsub\_gate:my16add|muxnot:nb0"  Info (12128): Elaborating entity "my16bitmux" for hierarchy "datapath:datapathproj|alu:myalu|my16bitaddsub\_gate:my16add|my16bitmux:mm"  Info (12128): Elaborating entity "my16bitfulladder" for hierarchy "datapath:datapathproj|alu:myalu|my16bitaddsub\_gate:my16add|my16bitfulladder:mf"  Info (12128): Elaborating entity "my1bitfulladder" for hierarchy "datapath:datapathproj|alu:myalu|my16bitaddsub\_gate:my16add|my16bitfulladder:mf|my1bitfulladder:my0"  Info (12128): Elaborating entity "my1bithalfadder" for hierarchy "datapath:datapathproj|alu:myalu|my16bitaddsub\_gate:my16add|my16bitfulladder:mf|my1bitfulladder:my0|my1bithalfadder:m0"  Info (12128): Elaborating entity "muxand" for hierarchy "datapath:datapathproj|alu:myalu|my16bitaddsub\_gate:my16add|my16bitfulladder:mf|my1bitfulladder:my0|my1bithalfadder:m0|muxand:a1"  Info (12128): Elaborating entity "muxor" for hierarchy "datapath:datapathproj|alu:myalu|my16bitaddsub\_gate:my16add|my16bitfulladder:mf|my1bitfulladder:my0|muxor:O1"  Info (12128): Elaborating entity "my16bitmuxnot" for hierarchy "datapath:datapathproj|alu:myalu|my16bitmuxnot:my16muxnot"  Info (12128): Elaborating entity "multiplier" for hierarchy "datapath:datapathproj|alu:myalu|multiplier:my16mul"  Info (12128): Elaborating entity "my16bitdivider" for hierarchy "datapath:datapathproj|alu:myalu|my16bitdivider:my16div"  Warning (10036): Verilog HDL or VHDL warning at alu.v(200): object "A\_reg" assigned a value but never read  Warning (10036): Verilog HDL or VHDL warning at alu.v(202): object "C\_out" assigned a value but never read  Warning (10240): Verilog HDL Always Construct warning at alu.v(214): inferring latch(es) for variable "next\_state", which holds its previous value in one or more paths through the always construct  Info (10041): Inferred latch for "next\_state.S101" at alu.v(214)  Info (10041): Inferred latch for "next\_state.S100" at alu.v(214)  Info (10041): Inferred latch for "next\_state.S011" at alu.v(214)  Info (10041): Inferred latch for "next\_state.S010" at alu.v(214)  Info (10041): Inferred latch for "next\_state.S001" at alu.v(214)  Info (10041): Inferred latch for "next\_state.S000" at alu.v(214)  Info (12128): Elaborating entity "myexp" for hierarchy "datapath:datapathproj|alu:myalu|myexp:mye"  Warning (10230): Verilog HDL assignment warning at alu.v(380): truncated value with size 32 to match size of target (16)  Info (12128): Elaborating entity "registers" for hierarchy "datapath:datapathproj|registers:myreg"  Info (12128): Elaborating entity "ctr" for hierarchy "ctr:ctrproj"  Warning (10240): Verilog HDL Always Construct warning at ctr.v(98): inferring latch(es) for variable "mod", which holds its previous value in one or more paths through the always construct  Warning (10240): Verilog HDL Always Construct warning at ctr.v(189): inferring latch(es) for variable "opALU", which holds its previous value in one or more paths through the always construct  Info (10041): Inferred latch for "opALU[0]" at ctr.v(193)  Info (10041): Inferred latch for "opALU[1]" at ctr.v(193)  Info (10041): Inferred latch for "opALU[2]" at ctr.v(193)  Info (10041): Inferred latch for "mod" at ctr.v(98)  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[0]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[1]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[2]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[3]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[4]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[5]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[6]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[7]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[8]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[9]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[10]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[11]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[12]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[13]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[14]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|Rout[15]" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|my16bitdivider:my16div|next\_state.S000\_874" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|my16bitdivider:my16div|next\_state.S001\_863" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|my16bitdivider:my16div|next\_state.S011\_844" is permanently enabled  Warning (14026): LATCH primitive "datapath:datapathproj|alu:myalu|my16bitdivider:my16div|next\_state.S100\_833" is permanently enabled  Warning (12241): 1 hierarchies have connectivity warnings - see the Connectivity Checks report folder  Warning (13012): Latch ctr:ctrproj|opALU[1] has unsafe behavior  Warning (13013): Ports D and ENA on the latch are fed by the same signal ctr:ctrproj|current\_state.ExecDIV\_3  Warning (13013): Ports D and ENA on the latch are fed by the same signal ctr:ctrproj|current\_state.ExecDIV\_3  Warning (13012): Latch ctr:ctrproj|opALU[0] has unsafe behavior  Warning (13013): Ports D and ENA on the latch are fed by the same signal ctr:ctrproj|current\_state.ExecDIV\_3  Warning (13013): Ports D and ENA on the latch are fed by the same signal ctr:ctrproj|current\_state.ExecDIV\_3  Warning (13012): Latch ctr:ctrproj|mod has unsafe behavior  Warning (13013): Ports D and ENA on the latch are fed by the same signal datapath:datapathproj|registers:myreg|IR\_reg[5]  Warning (13013): Ports D and ENA on the latch are fed by the same signal datapath:datapathproj|registers:myreg|IR\_reg[5]  Info (286030): Timing-Driven Synthesis is running  Info (17049): 11 registers lost all their fanouts during netlist optimizations.  Info (144001): Generated suppressed messages file C:/Users/huo00/Desktop/ECE310/syn/project2/output\_files/proj2.map.smsg  Info (16010): Generating hard\_block partition "hard\_block:auto\_generated\_inst"  Info (16011): Adding 0 node(s), including 0 DDIO, 0 PLL, 0 transceiver and 0 LCELL  Info (16011): Adding 0 node(s), including 0 DDIO, 0 PLL, 0 transceiver and 0 LCELL  Info (21057): Implemented 6399 device resources after synthesis - the final resource count might be different  Info (21058): Implemented 2 input pins  Info (21059): Implemented 25 output pins  Info (21061): Implemented 6372 logic cells  Info (21058): Implemented 2 input pins  Info (21059): Implemented 25 output pins  Info (21061): Implemented 6372 logic cells  Info: Quartus II 64-Bit Analysis & Synthesis was successful. 0 errors, 37 warnings  Info: Peak virtual memory: 4752 megabytes  Info: Processing ended: Mon Nov 28 21:49:25 2022  Info: Elapsed time: 00:00:06  Info: Total CPU time (on all processors): 00:00:05  Info: Peak virtual memory: 4752 megabytes  Info: Processing ended: Mon Nov 28 21:49:25 2022  Info: Elapsed time: 00:00:06  Info: Total CPU time (on all processors): 00:00:05  Info: \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  Info: Running Quartus II 64-Bit Fitter  Info: Version 13.1.0 Build 162 10/23/2013 SJ Web Edition  Info: Processing started: Mon Nov 28 21:49:26 2022  Info: Version 13.1.0 Build 162 10/23/2013 SJ Web Edition  Info: Processing started: Mon Nov 28 21:49:26 2022  Info: Command: quartus\_fit --read\_settings\_files=off --write\_settings\_files=off proj2 -c proj2  Info: qfit2\_default\_script.tcl version: #1  Info: Project = proj2  Info: Revision = proj2  Info (20030): Parallel compilation is enabled and will use 16 of the 16 processors detected  Info (119004): Automatically selected device EP2AGX45CU17I3 for design proj2  Info (21076): High junction temperature operating condition is not set. Assuming a default value of '100'.  Info (21076): Low junction temperature operating condition is not set. Assuming a default value of '-40'.  Info (171003): Fitter is performing an Auto Fit compilation, which may decrease Fitter effort to reduce compilation time  Warning (292013): Feature LogicLock is only available with a valid subscription license. You can purchase a software subscription to gain full access to this feature.  Info (176444): Device migration not selected. If you intend to use device migration later, you may need to change the pin assignments as they may be incompatible with other devices  Info (176445): Device EP2AGX65CU17I3 is compatible  Info (176445): Device EP2AGX65CU17I3 is compatible  Info (169124): Fitter converted 1 user pins into dedicated programming pins  Info (169125): Pin ~ALTERA\_nCEO~ is reserved at location W12  Info (169125): Pin ~ALTERA\_nCEO~ is reserved at location W12  Warning (15714): Some pins have incomplete I/O assignments. Refer to the I/O Assignment Warnings report for details  Critical Warning (169085): No exact pin location assignment(s) for 27 pins of 27 total pins  Info (169086): Pin MemRW\_IO not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[0] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[1] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[2] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[3] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[4] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[5] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[6] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[7] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[0] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[1] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[2] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[3] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[4] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[5] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[6] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[7] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[8] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[9] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[10] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[11] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[12] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[13] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[14] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[15] not assigned to an exact location on the device  Info (169086): Pin rst not assigned to an exact location on the device  Info (169086): Pin clk not assigned to an exact location on the device  Info (169086): Pin MemRW\_IO not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[0] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[1] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[2] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[3] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[4] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[5] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[6] not assigned to an exact location on the device  Info (169086): Pin MemAddr\_IO[7] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[0] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[1] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[2] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[3] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[4] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[5] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[6] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[7] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[8] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[9] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[10] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[11] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[12] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[13] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[14] not assigned to an exact location on the device  Info (169086): Pin MemD\_IO[15] not assigned to an exact location on the device  Info (169086): Pin rst not assigned to an exact location on the device  Info (169086): Pin clk not assigned to an exact location on the device  Warning (335093): TimeQuest Timing Analyzer is analyzing 4116 combinational loops as latches.  Critical Warning (332012): Synopsys Design Constraints File file not found: 'proj2.sdc'. A Synopsys Design Constraints File is required by the TimeQuest Timing Analyzer to get proper timing constraints. Without it, the Compiler will not properly optimize the design.  Info (332144): No user constrained base clocks found in the design  Info (332143): No user constrained clock uncertainty found in the design. Calling "derive\_clock\_uncertainty"  Info (332123): Deriving Clock Uncertainty. Please refer to report\_sdc in TimeQuest to see clock uncertainties.  Info (332130): Timing requirements not specified -- quality metrics such as performance may be sacrificed to reduce compilation time.  Info (176353): Automatically promoted node clk~input (placed in PIN T10 (CLK6, DIFFCLK\_0p))  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G6  Info (176356): Following destination nodes may be non-global or may not use global or regional clocks  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[5]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[6]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[4]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[3]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[2]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[1]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[0]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[7]  Info (176357): Destination node datapath:datapathproj|registers:myreg|MAR\_reg[7]  Info (176357): Destination node datapath:datapathproj|registers:myreg|MAR\_reg[4]  Info (176358): Non-global destination nodes limited to 10 nodes  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G6  Info (176356): Following destination nodes may be non-global or may not use global or regional clocks  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[5]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[6]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[4]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[3]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[2]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[1]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[0]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[7]  Info (176357): Destination node datapath:datapathproj|registers:myreg|MAR\_reg[7]  Info (176357): Destination node datapath:datapathproj|registers:myreg|MAR\_reg[4]  Info (176358): Non-global destination nodes limited to 10 nodes  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[5]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[6]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[4]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[3]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[2]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[1]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[0]  Info (176357): Destination node datapath:datapathproj|registers:myreg|IR\_reg[7]  Info (176357): Destination node datapath:datapathproj|registers:myreg|MAR\_reg[7]  Info (176357): Destination node datapath:datapathproj|registers:myreg|MAR\_reg[4]  Info (176358): Non-global destination nodes limited to 10 nodes  Info (176353): Automatically promoted node ctr:ctrproj|current\_state.ExecStore\_1  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G0  Info (176356): Following destination nodes may be non-global or may not use global or regional clocks  Info (176357): Destination node ctr:ctrproj|next\_state~0  Info (176357): Destination node rtl~256  Info (176357): Destination node rtl~257  Info (176357): Destination node rtl~258  Info (176357): Destination node rtl~259  Info (176357): Destination node MemRW\_IO~output  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G0  Info (176356): Following destination nodes may be non-global or may not use global or regional clocks  Info (176357): Destination node ctr:ctrproj|next\_state~0  Info (176357): Destination node rtl~256  Info (176357): Destination node rtl~257  Info (176357): Destination node rtl~258  Info (176357): Destination node rtl~259  Info (176357): Destination node MemRW\_IO~output  Info (176357): Destination node ctr:ctrproj|next\_state~0  Info (176357): Destination node rtl~256  Info (176357): Destination node rtl~257  Info (176357): Destination node rtl~258  Info (176357): Destination node rtl~259  Info (176357): Destination node MemRW\_IO~output  Info (176353): Automatically promoted node rtl~0  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G9  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G9  Info (176353): Automatically promoted node rtl~1  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G3  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G3  Info (176353): Automatically promoted node rtl~10  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G14  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G14  Info (176353): Automatically promoted node rtl~100  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G15  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G15  Info (176353): Automatically promoted node rtl~101  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G10  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G10  Info (176353): Automatically promoted node rtl~102  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G12  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G12  Info (176353): Automatically promoted node rtl~103  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G13  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G13  Info (176353): Automatically promoted node rtl~104  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G8  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G8  Info (176353): Automatically promoted node rtl~105  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G7  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G7  Info (176353): Automatically promoted node rtl~106  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G11  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G11  Info (176353): Automatically promoted node rtl~107  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G1  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G1  Info (176353): Automatically promoted node rtl~108  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G5  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G5  Info (176353): Automatically promoted node rtl~109  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G2  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G2  Info (176353): Automatically promoted node rtl~11  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G4  Info (176355): Automatically promoted destinations to use location or clock signal Global Clock CLKCTRL\_G4  Info (176233): Starting register packing  Info (176235): Finished register packing  Extra Info (176219): No registers were packed into other blocks  Extra Info (176219): No registers were packed into other blocks  Info (176214): Statistics of I/O pins that need to be placed that use the same VCCIO and VREF, before I/O pin placement  Info (176211): Number of I/O pins in group: 26 (unused VREF, 2.5V VCCIO, 1 input, 25 output, 0 bidirectional)  Info (176212): I/O standards used: 2.5 V.  Info (176211): Number of I/O pins in group: 26 (unused VREF, 2.5V VCCIO, 1 input, 25 output, 0 bidirectional)  Info (176212): I/O standards used: 2.5 V.  Info (176212): I/O standards used: 2.5 V.  Info (176215): I/O bank details before I/O pin placement  Info (176214): Statistics of I/O banks  Info (176213): I/O bank number QL1 does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 0 pins available  Info (176213): I/O bank number QL0 does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 0 pins available  Info (176213): I/O bank number 3C does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 0 pins available  Info (176213): I/O bank number 3A does not use VREF pins and has undetermined VCCIO pins. 2 total pin(s) used -- 19 pins available  Info (176213): I/O bank number 4A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 36 pins available  Info (176213): I/O bank number 5A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 16 pins available  Info (176213): I/O bank number 6A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 16 pins available  Info (176213): I/O bank number 7A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 36 pins available  Info (176213): I/O bank number 8A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 20 pins available  Info (176213): I/O bank number 8C does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 0 pins available  Info (176214): Statistics of I/O banks  Info (176213): I/O bank number QL1 does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 0 pins available  Info (176213): I/O bank number QL0 does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 0 pins available  Info (176213): I/O bank number 3C does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 0 pins available  Info (176213): I/O bank number 3A does not use VREF pins and has undetermined VCCIO pins. 2 total pin(s) used -- 19 pins available  Info (176213): I/O bank number 4A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 36 pins available  Info (176213): I/O bank number 5A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 16 pins available  Info (176213): I/O bank number 6A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 16 pins available  Info (176213): I/O bank number 7A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 36 pins available  Info (176213): I/O bank number 8A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 20 pins available  Info (176213): I/O bank number 8C does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 0 pins available  Info (176213): I/O bank number QL1 does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 0 pins available  Info (176213): I/O bank number QL0 does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 0 pins available  Info (176213): I/O bank number 3C does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 0 pins available  Info (176213): I/O bank number 3A does not use VREF pins and has undetermined VCCIO pins. 2 total pin(s) used -- 19 pins available  Info (176213): I/O bank number 4A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 36 pins available  Info (176213): I/O bank number 5A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 16 pins available  Info (176213): I/O bank number 6A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 16 pins available  Info (176213): I/O bank number 7A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 36 pins available  Info (176213): I/O bank number 8A does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 20 pins available  Info (176213): I/O bank number 8C does not use VREF pins and has undetermined VCCIO pins. 0 total pin(s) used -- 0 pins available  Info (171121): Fitter preparation operations ending: elapsed time is 00:00:03  Info (170189): Fitter placement preparation operations beginning  Info (170190): Fitter placement preparation operations ending: elapsed time is 00:00:02  Info (170191): Fitter placement operations beginning  Info (170137): Fitter placement was successful  Info (170192): Fitter placement operations ending: elapsed time is 00:00:09  Info (170193): Fitter routing operations beginning  Info (170195): Router estimated average interconnect usage is 4% of the available device resources  Info (170196): Router estimated peak interconnect usage is 28% of the available device resources in the region that extends from location X24\_Y22 to location X35\_Y33  Info (170196): Router estimated peak interconnect usage is 28% of the available device resources in the region that extends from location X24\_Y22 to location X35\_Y33  Info (170194): Fitter routing operations ending: elapsed time is 00:00:44  Info (170199): The Fitter performed an Auto Fit compilation. Optimizations were skipped to reduce compilation time.  Info (170201): Optimizations that may affect the design's routability were skipped  Info (170201): Optimizations that may affect the design's routability were skipped  Info (11888): Total time spent on timing analysis during the Fitter is 3.00 seconds.  Info (334003): Started post-fitting delay annotation  Info (334004): Delay annotation completed successfully  Info (334003): Started post-fitting delay annotation  Info (334004): Delay annotation completed successfully  Info (11218): Fitter post-fit operations ending: elapsed time is 00:00:03  Info (144001): Generated suppressed messages file C:/Users/huo00/Desktop/ECE310/syn/project2/output\_files/proj2.fit.smsg  Info: Quartus II 64-Bit Fitter was successful. 0 errors, 5 warnings  Info: Peak virtual memory: 6399 megabytes  Info: Processing ended: Mon Nov 28 21:50:36 2022  Info: Elapsed time: 00:01:10  Info: Total CPU time (on all processors): 00:01:08  Info: Peak virtual memory: 6399 megabytes  Info: Processing ended: Mon Nov 28 21:50:36 2022  Info: Elapsed time: 00:01:10  Info: Total CPU time (on all processors): 00:01:08  Info: \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  Info: Running Quartus II 64-Bit Assembler  Info: Version 13.1.0 Build 162 10/23/2013 SJ Web Edition  Info: Processing started: Mon Nov 28 21:50:38 2022  Info: Version 13.1.0 Build 162 10/23/2013 SJ Web Edition  Info: Processing started: Mon Nov 28 21:50:38 2022  Info: Command: quartus\_asm --read\_settings\_files=off --write\_settings\_files=off proj2 -c proj2  Info (115031): Writing out detailed assembly data for power analysis  Info (115030): Assembler is generating device programming files  Info: Quartus II 64-Bit Assembler was successful. 0 errors, 0 warnings  Info: Peak virtual memory: 4730 megabytes  Info: Processing ended: Mon Nov 28 21:50:41 2022  Info: Elapsed time: 00:00:03  Info: Total CPU time (on all processors): 00:00:03  Info: Peak virtual memory: 4730 megabytes  Info: Processing ended: Mon Nov 28 21:50:41 2022  Info: Elapsed time: 00:00:03  Info: Total CPU time (on all processors): 00:00:03  Info (293026): Skipped module PowerPlay Power Analyzer due to the assignment FLOW\_ENABLE\_POWER\_ANALYZER  Info: \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  Info: Running Quartus II 64-Bit TimeQuest Timing Analyzer  Info: Version 13.1.0 Build 162 10/23/2013 SJ Web Edition  Info: Processing started: Mon Nov 28 21:50:43 2022  Info: Version 13.1.0 Build 162 10/23/2013 SJ Web Edition  Info: Processing started: Mon Nov 28 21:50:43 2022  Info: Command: quartus\_sta proj2 -c proj2  Info: qsta\_default\_script.tcl version: #1  Info (20030): Parallel compilation is enabled and will use 16 of the 16 processors detected  Info (21076): High junction temperature operating condition is not set. Assuming a default value of '100'.  Info (21076): Low junction temperature operating condition is not set. Assuming a default value of '-40'.  Warning (335093): TimeQuest Timing Analyzer is analyzing 4116 combinational loops as latches.  Critical Warning (332012): Synopsys Design Constraints File file not found: 'proj2.sdc'. A Synopsys Design Constraints File is required by the TimeQuest Timing Analyzer to get proper timing constraints. Without it, the Compiler will not properly optimize the design.  Info (332142): No user constrained base clocks found in the design. Calling "derive\_clocks -period 1.0"  Info (332105): Deriving Clocks  Info (332105): create\_clock -period 1.000 -name clk clk  Info (332105): create\_clock -period 1.000 -name ctr:ctrproj|current\_state.ExecStore\_1 ctr:ctrproj|current\_state.ExecStore\_1  Info (332105): create\_clock -period 1.000 -name ctr:ctrproj|current\_state.ExecDIV\_3 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332105): create\_clock -period 1.000 -name ctr:ctrproj|current\_state.Decode ctr:ctrproj|current\_state.Decode  Info (332105): create\_clock -period 1.000 -name clk clk  Info (332105): create\_clock -period 1.000 -name ctr:ctrproj|current\_state.ExecStore\_1 ctr:ctrproj|current\_state.ExecStore\_1  Info (332105): create\_clock -period 1.000 -name ctr:ctrproj|current\_state.ExecDIV\_3 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332105): create\_clock -period 1.000 -name ctr:ctrproj|current\_state.Decode ctr:ctrproj|current\_state.Decode  Info (332143): No user constrained clock uncertainty found in the design. Calling "derive\_clock\_uncertainty"  Info (332123): Deriving Clock Uncertainty. Please refer to report\_sdc in TimeQuest to see clock uncertainties.  Info: Found TIMEQUEST\_REPORT\_SCRIPT\_INCLUDE\_DEFAULT\_ANALYSIS = ON  Info: Analyzing Slow 900mV 100C Model  Critical Warning (332148): Timing requirements not met  Info (11105): For recommendations on closing timing, run Report Timing Closure Recommendations in the TimeQuest Timing Analyzer.  Info (11105): For recommendations on closing timing, run Report Timing Closure Recommendations in the TimeQuest Timing Analyzer.  Info (332146): Worst-case setup slack is -5.745  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -5.745 -6565.661 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): -4.237 -388.738 clk  Info (332119): -2.726 -2.726 ctr:ctrproj|current\_state.Decode  Info (332119): -1.165 -2.299 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -5.745 -6565.661 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): -4.237 -388.738 clk  Info (332119): -2.726 -2.726 ctr:ctrproj|current\_state.Decode  Info (332119): -1.165 -2.299 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332146): Worst-case hold slack is -0.917  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -0.917 -13.974 clk  Info (332119): -0.253 -1.866 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): 0.022 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): 2.467 0.000 ctr:ctrproj|current\_state.Decode  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -0.917 -13.974 clk  Info (332119): -0.253 -1.866 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): 0.022 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): 2.467 0.000 ctr:ctrproj|current\_state.Decode  Info (332146): Worst-case recovery slack is -3.435  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -3.435 -6.417 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -3.435 -6.417 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332146): Worst-case removal slack is 2.737  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): 2.737 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): 2.737 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332146): Worst-case minimum pulse width slack is -2.846  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -2.846 -316.795 clk  Info (332119): 0.363 0.000 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): 0.481 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): 0.482 0.000 ctr:ctrproj|current\_state.Decode  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -2.846 -316.795 clk  Info (332119): 0.363 0.000 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): 0.481 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): 0.482 0.000 ctr:ctrproj|current\_state.Decode  Info: Analyzing Slow 900mV -40C Model  Info (334003): Started post-fitting delay annotation  Info (334004): Delay annotation completed successfully  Info (332123): Deriving Clock Uncertainty. Please refer to report\_sdc in TimeQuest to see clock uncertainties.  Critical Warning (332148): Timing requirements not met  Info (11105): For recommendations on closing timing, run Report Timing Closure Recommendations in the TimeQuest Timing Analyzer.  Info (11105): For recommendations on closing timing, run Report Timing Closure Recommendations in the TimeQuest Timing Analyzer.  Info (332146): Worst-case setup slack is -5.204  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -5.204 -6519.201 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): -4.012 -356.267 clk  Info (332119): -2.567 -2.567 ctr:ctrproj|current\_state.Decode  Info (332119): -1.106 -2.169 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -5.204 -6519.201 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): -4.012 -356.267 clk  Info (332119): -2.567 -2.567 ctr:ctrproj|current\_state.Decode  Info (332119): -1.106 -2.169 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332146): Worst-case hold slack is -0.907  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -0.907 -14.521 clk  Info (332119): -0.107 -0.269 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): 0.032 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): 2.377 0.000 ctr:ctrproj|current\_state.Decode  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -0.907 -14.521 clk  Info (332119): -0.107 -0.269 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): 0.032 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): 2.377 0.000 ctr:ctrproj|current\_state.Decode  Info (332146): Worst-case recovery slack is -3.266  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -3.266 -6.126 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -3.266 -6.126 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332146): Worst-case removal slack is 2.662  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): 2.662 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): 2.662 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332146): Worst-case minimum pulse width slack is -2.846  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -2.846 -317.179 clk  Info (332119): 0.334 0.000 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): 0.466 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): 0.481 0.000 ctr:ctrproj|current\_state.Decode  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -2.846 -317.179 clk  Info (332119): 0.334 0.000 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): 0.466 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): 0.481 0.000 ctr:ctrproj|current\_state.Decode  Info: Analyzing Fast 900mV -40C Model  Info (332123): Deriving Clock Uncertainty. Please refer to report\_sdc in TimeQuest to see clock uncertainties.  Critical Warning (332148): Timing requirements not met  Info (11105): For recommendations on closing timing, run Report Timing Closure Recommendations in the TimeQuest Timing Analyzer.  Info (11105): For recommendations on closing timing, run Report Timing Closure Recommendations in the TimeQuest Timing Analyzer.  Info (332146): Worst-case setup slack is -2.813  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -2.813 -2162.784 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): -1.719 -108.362 clk  Info (332119): -1.086 -1.086 ctr:ctrproj|current\_state.Decode  Info (332119): -0.073 -0.116 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -2.813 -2162.784 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): -1.719 -108.362 clk  Info (332119): -1.086 -1.086 ctr:ctrproj|current\_state.Decode  Info (332119): -0.073 -0.116 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332146): Worst-case hold slack is -0.492  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -0.492 -7.298 clk  Info (332119): -0.046 -0.058 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): 0.014 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): 1.457 0.000 ctr:ctrproj|current\_state.Decode  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -0.492 -7.298 clk  Info (332119): -0.046 -0.058 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): 0.014 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): 1.457 0.000 ctr:ctrproj|current\_state.Decode  Info (332146): Worst-case recovery slack is -1.489  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -1.489 -2.726 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -1.489 -2.726 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332146): Worst-case removal slack is 1.609  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): 1.609 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): 1.609 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332146): Worst-case minimum pulse width slack is -2.846  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -2.846 -133.873 clk  Info (332119): 0.397 0.000 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): 0.490 0.000 ctr:ctrproj|current\_state.Decode  Info (332119): 0.494 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (332119): Slack End Point TNS Clock  Info (332119): ========= =================== =====================  Info (332119): -2.846 -133.873 clk  Info (332119): 0.397 0.000 ctr:ctrproj|current\_state.ExecStore\_1  Info (332119): 0.490 0.000 ctr:ctrproj|current\_state.Decode  Info (332119): 0.494 0.000 ctr:ctrproj|current\_state.ExecDIV\_3  Info (21076): High junction temperature operating condition is not set. Assuming a default value of '100'.  Info (21076): Low junction temperature operating condition is not set. Assuming a default value of '-40'.  Info (332123): Deriving Clock Uncertainty. Please refer to report\_sdc in TimeQuest to see clock uncertainties.  Info (332102): Design is not fully constrained for setup requirements  Info (332102): Design is not fully constrained for hold requirements  Info: Quartus II 64-Bit TimeQuest Timing Analyzer was successful. 0 errors, 5 warnings  Info: Peak virtual memory: 5004 megabytes  Info: Processing ended: Mon Nov 28 21:50:47 2022  Info: Elapsed time: 00:00:04  Info: Total CPU time (on all processors): 00:00:04  Info: Peak virtual memory: 5004 megabytes  Info: Processing ended: Mon Nov 28 21:50:47 2022  Info: Elapsed time: 00:00:04  Info: Total CPU time (on all processors): 00:00:04  Info: \*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*  Info: Running Quartus II 64-Bit EDA Netlist Writer  Info: Version 13.1.0 Build 162 10/23/2013 SJ Web Edition  Info: Processing started: Mon Nov 28 21:50:48 2022  Info: Version 13.1.0 Build 162 10/23/2013 SJ Web Edition  Info: Processing started: Mon Nov 28 21:50:48 2022  Info: Command: quartus\_eda --read\_settings\_files=off --write\_settings\_files=off proj2 -c proj2  Info (204019): Generated file proj2\_3\_900mv\_100c\_slow.vho in folder "C:/Users/huo00/Desktop/ECE310/syn/project2/simulation/modelsim/" for EDA simulation tool  Info (204019): Generated file proj2\_3\_900mv\_-40c\_slow.vho in folder "C:/Users/huo00/Desktop/ECE310/syn/project2/simulation/modelsim/" for EDA simulation tool  Info (204019): Generated file proj2\_min\_900mv\_-40c\_fast.vho in folder "C:/Users/huo00/Desktop/ECE310/syn/project2/simulation/modelsim/" for EDA simulation tool  Info (204019): Generated file proj2.vho in folder "C:/Users/huo00/Desktop/ECE310/syn/project2/simulation/modelsim/" for EDA simulation tool  Info (204019): Generated file proj2\_3\_900mv\_100c\_vhd\_slow.sdo in folder "C:/Users/huo00/Desktop/ECE310/syn/project2/simulation/modelsim/" for EDA simulation tool  Info (204019): Generated file proj2\_3\_900mv\_-40c\_vhd\_slow.sdo in folder "C:/Users/huo00/Desktop/ECE310/syn/project2/simulation/modelsim/" for EDA simulation tool  Info (204019): Generated file proj2\_min\_900mv\_-40c\_vhd\_fast.sdo in folder "C:/Users/huo00/Desktop/ECE310/syn/project2/simulation/modelsim/" for EDA simulation tool  Info (204019): Generated file proj2\_vhd.sdo in folder "C:/Users/huo00/Desktop/ECE310/syn/project2/simulation/modelsim/" for EDA simulation tool  Info: Quartus II 64-Bit EDA Netlist Writer was successful. 0 errors, 0 warnings  Info: Peak virtual memory: 4699 megabytes  Info: Processing ended: Mon Nov 28 21:50:53 2022  Info: Elapsed time: 00:00:05  Info: Total CPU time (on all processors): 00:00:04  Info: Peak virtual memory: 4699 megabytes  Info: Processing ended: Mon Nov 28 21:50:53 2022  Info: Elapsed time: 00:00:05  Info: Total CPU time (on all processors): 00:00:04  Info (293000): Quartus II Full Compilation was successful. 0 errors, 47 warnings |

**Name: Ye Qin Student ID:200281549**

I certify that I did not copy the answers to this homework and did not let

anyone copy my answers (sign):

\_\_\_\_\_\_\_\_Ye Qin\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_