Yuanqiu(Zoe) Tan

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Education

Purdue University *(Prof. Zhihong Chen), West Lafayette, IN* — Aug 2020 - present
Ph.D. in Electrical Engineering — GPA: 4.0/4.0
Master of Science in Electrical Engineering — Dec 2024
Purdue University, *West Lafayette, IN* — Aug 2016 - 2020
Bachelor of Science in Electrical Engineering - Graduate with Highest Distinction — GPA: 3.97/4.0
Minor in Economics

Skills

Fabrication and Characterization: e-Beam Lithography, Photolithography, Plasma-Enhanced Chemical Vapor Deposition, ALD, RIE, Ion Milling, MPMS, PPMS, AFM, SEM, XRD, Optical Spectrum.
Software: Cadence, HSpice, LTspice, TCAD, Python, C, MATLAB, Verilog, ABEL, Embedded C, Eagle, Klayout, Solidworks, 3ds Max

Research and Internship

Graduate Research Assistant — **Birck Nanotechnology Center**, IN
Research Assistant — August 2020 - present

Probabilistic- bit based on Stochastic Low-Barrier-Nanomagnets (LBM) with spin transport on 2D diffusion channel (Funded by US NAVY)

- Developed the stochastic low-barrier nanomagnet stack for both In-plane Magnetic Anisotropy (IMA) and Perpendicular Magnetic Anisotropy (PMA) magnets fluctuating in kHz.
- Designing and fabricating probabilistic logic array with stochastic LBM and 2D spin diffusion channel to achieve low energy without charge-spin conversion.
- Simulating the spin transport for designed logic array with HSpice.

High-performance monolayer TMD devices through defect engineering and doping (Funded by Intel and Semiconductor Research Corporation)

- Developing robust spacer doping strategy for monolayer WSe_2, with record high threshold voltage control for ultra-scaled p-type FETs, while showing thermal robustness compatible with BEOL integration.
- Developed robust passivation and doping strategy for monolayer WSe_2, resulting in substantial improvements in device performance in both the on-state and off-state performance of monolayer WSe_2, with SS_{min}-values reaching 70mV/dec, on-currents of 110 μA/μm and Imax/Imin $> 10^9$, while maintaining promising stability under various conditions.
- Revealed the correlation between off-state electrical performance and Raman spectra.
- Performed the reliability study of p-type FETs to illustrate the potential defect differences between defect engineering and doping.
- Surface analysis through XPS and EELS with TEM showing the binding mechanism of the doping strategy.

Ultra-thin material searching for liner and diffusion barrier in advanced interconnect (Funded by NSF FuSe2)

- Developing and implementing a machine learning-enhanced algorithm to efficiently identify and evaluate candidate materials for thin liner applications.
- Synthesizing the liner and diffusion barrier utilizing Plasma-Enhanced Chemical Vapor Deposition (PECVD), and conducting comprehensive evaluations of their electrical, optical, and thermal properties.

Surface analysis of defect and interface study in monolayer 2D TMD materials (Funded by Intel)

- Depositing the contamination-free monolayer TMD materials on TEM grids and introducing various defect engineering and doping techniques.
- Establishing the capability of low-energy STEM imaging with atomic resolution and eliminating the damage to the sample surface.

Innovation for Front-End-Of-Line application with sub-nanometer 2D TMD materials for next technology node (Funded by Semiconductor Research Corporation)

- Designed and Fabricated advanced n-type and p-type FETs with TMD materials and high-k dielectric, reaching channel length of tenth nanometer.
- Investigating the contact engineering, doping strategies, and dielectric growth to improve the on-state current to 1 mA/µm and low contact resistance.
- Studied the impact of e-Beam lithography and photolithography on monolayer 2D TMD materials.

Large area 2D diffusion barrier for Ultra-Scaled Interconnect Technology (Funded by Semiconductor Research Corporation, Samsung, and EMD)

- Conducted in-depth studies on BOEL-compatible growth of nanometer-thin TMD and graphene layers, resulting in a 50% enhancement in electrical resistivity. This improvement was closely linked to advancements in crystallinity and surface scattering properties, demonstrating the significant impact of material quality on device performance.
- Enhanced Cu interconnect lifetime and performance by integrating TMD materials in the fabrication process, with comprehensive study in the BEOL compatible growth for diffusion barrier and liner barrier in trench structure, achieving a 30% improvement in lifetime compared to that with TaN and Ta.

Experimental demonstration of an integrated on-chip p-bit core utilizing stochastic Magnetic Tunnel Junctions and 2D-MoS2 FETs (Funded by NSF)

- Designed a PCB circuit and measurement setup to characterize high-frequency stochastic MTJs in the GHz range with low noise.
- Worked on electrically characterizing and studying the response of stochastic MTJ to temperature and input voltage in the time domain.

Graduate Research Mentor Undergrad VIP team in Semiconductor Jan 2023 - 2024

- Supervising the class of 50 undergraduate students in MOS fabrication, NV center sensing, and heterostructure design.
- Mentoring undergraduate students in semiconductor-related research topics and career paths, and helping connect them through technical seminars with engineers and scientists from national labs and Industries.

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New Limits group led by Dr. Zhihong Chen Purdue University, IN

Undergraduate Research Assistant May 2019 - May 2020

- Conducted C-V measurement in SiC MOS with the ring capacitor model on the probe station to extract the intrinsic properties from the device.
- Conducted 4-probe I-V measurement and 4-point probe conductance measurement SiC device and MoS2 device for determining if it is appropriate for device fabrication and analyzing its performance
- Analyzed the performance of MOS devices with different annealing conditions to offer recommendations in annealing for TMD transistor fabrication.

CAPSL group led by Dr. Joerg Appenzeller Purdue University, IN

Undergraduate Research Assistant Internship May 2019 - May 2020

- Analyzed the design related to oscillator based Ising model with SPICE circuit simulation.
- Implemented the circuits on the breadboard and analyzed them with the oscilloscope and differential amplifier.
- Explored the potential design of spintronics for the next generation of probabilistic computing.

Human Body Communication project led by Dr. Shreyas Sen Purdue University, IN

Research Assistant January 2018 - January 2019

- Optimized the analog circuit design for HBC wake-up receiver to improve the accuracy of the main receiver and lower overall power.
- Analyzed the performance of our design when frequency beyond 10MHz to minimize the potential hazards.
- Performed literature review and developed the control techniques to achieve 200MHz to 1GHz to support the testbench for the overall HBC chip.

Undergraduate Teaching Assistant Purdue University, IN

ECE 207, ECE 362, ECE 337 January 2018- May 2020

- Instructed students on the concepts of digital circuits, ASIC, and assembly language.
- Supervised and planned undergraduate laboratory for class of 60 students in CMOS circuit analysis, ASIC design and application in STM32 and ESP32.

Shandong Shenchuan Drive Technology Co., Ltd Shandong, China

Technology support and development Intern May 2017

- Tested and analyzed the new product with our team to minimize potential problems and provide understandable instructions to customers.
- Tracked and communicated the entire process of production between each department to optimize the standard operation principle minimizing the potential problems.

Project Experience

Probabilistic computing based on 3T-1sMTJ for reversible logic (*Cadence*) May 2024

- Explored the development and application of stochastic magnetic tunnel junctions (sMTJs) in the realm of probabilistic computing, focusing on invertible logic gates and multipliers.

- Developed robust p-bit configurations that capitalize on the inherent stochasticity of low-energy barrier nanomagnets, utilizing a three-transistor, one sMTJ (3T-1sMTJ) design.
- Detailed the operational principles of these p-bits, emphasizing their ability to fluctuate between binary states under voltage control and how this capability can be harnessed for implementing complex forward and invertible logic operations and arithmetic functions.

Verilog USB Module on AHB Bus Interfac (*System Verilog*) April 2019

- Designed and implemented a complete USB transmitter and receiver module using Verilog/System Verilog, facilitating data communication between the AHB Bus and USB interface through an integrated data buffer..

Condiments Express & Six-degree Free Robotic Arms (*CAD, PCB, and Embedded system*) 2019

- Designed and built an automated condiment dispenser with full CAD/PCB design, motorized x-y table, sensors, and BLE-based OLED user interface.
- Engineered robotic arms with six degrees of freedom capable of rotating and grasping objects in multiple directions, integrating user controls via an STM32 microcontroller.

Publications

- **Y. Tan**, S. Yang, C. Lin, F. Vega, J. Cai, H. Lan, R. Tripathi, S. Sharma, Z. Shang, T. Hou, T. Beechem, J. Appenzeller, Z.Chen. "Monolayer WSe_2 Field Effect Transistor Performance Enhancement by Atomic Defect Engineering and Passivation". *ACS Nano* (2025). Impact Factor:15.8
- **Y. Tan**‡, R. Tripathi‡, S. Bunaiyan, R. Wagner, N. Dilley, S. Datta, K. Camsari, J. Appenzeller, Z. Chen. "Probing Magnitude and Directionality of Spin Vector in real space for Probabilistic Computing". *Nature Nano* (under review)
- J. Cai, H. Lan, **Y. Tan**, Z. Chen, J.Appenzeller. "First demonstration of DG monolayer MoS_2 FETs with 0.3nm-thin contact extensions achieving near immunity to SCEs at L_{CH} = 20nm and g_m = 206 μs/μm". *IEDM* 2025
- J. Daniel, Z. Sun, X. Zhang, **Y. Tan**, N. Dilley, Z. Chen, J. Appenzeller. "Experimental demonstration of an on-chip p-bit core based on stochastic magnetic tunnel junctions and 2D MoS_2 transistors". *Nature Communication* (2024). Impact Factor:17.7
- H. Lan, **Y. Tan**, S. Yang, X. Liu, Z. Shang,J. Appenzeller, Z. Chen. "Improved Hysteresis of High-Performance p-Type WSe_2 transistors with native oxide WO_x interfacial layer". *ACS Nano* (2025) Impact Factor:15.8
- J. Cai, H. Zhang, **Y. Tan**, Z. Sun, P. Wu, R. Tripathi, S. Krylyuk, C. Suhy, J. Kong, A. Davydov, Z. Chen, J. Appenzeller. "On-Chip Synthesis of Quasi-2D Semimetals from Multi-Layer Chalcogenides". *Adv. Mater.* (2024).Impact Factor:29.4
- P. Deng, Y. Wang, R. Yang, Z. He, **Y. Tan**, Z. Chen, J. Liu, T. Li. "Self-Powered Smart Textile Based on Dynamic Schottky Diode for Human-Machine Interactions". *Adv. Sci.* (2023). Impact Factor:15.1
- H. Lan, C. Lin, L. Liu, J.Cai, Z. Sun, P.Wu, **Y. Tan**, S. Yang, T. Hou, J. Appenzeller, Z. Chen, Uncovering the doping mechanism of nitric oxide in high-performance P-type WSe_2 transistors. *Nature Communication* (2025) Impact Factor:17.7
- Z. Sun, S. Kim, Jun Cai, J. Shen, H. Lan, **Y. Tan**, X. Wang, C. Shen, H. Wang, Z. Chen, R. Wallace, J. Appenzeller. "Low Contact Resistance on Monolayer MoS_2 Field-Effect Transistors Achieved by CMOS-Compatible Metal Contacts". *ACS Nano* (2024). Impact Factor:15.8

Oral Presentations and Presentation Proceedings

- **Y. Tan**, R. Tripathi, J. Appenzeller and Z. Chen. "Nonlocal Detection of Vector Spin Accumulation in Graphene for Probabilistic Computing". In 2024 Materials Research Society Fall Conference (MRS), Boston, Massachusetts.
- T. Ngo, **Y. Tan**, A. Zacatzi, D. Lee, A. Wankis, N. Vu, R. Kanjolia, M. Moinpour, Z.Chen. "300mm Wafer-Scale ALD-Grown MoS_2 for Cu Diffusion Barrier". In 2024 IEEE International Interconnect Technology Conference (IITC), San Jose, California.
- **Y. Tan**, and Z. Chen. "High performance monolayer WSe_2 devices through defect engineering and doping". In 2023 Device Research Conference (DRC), Santa Barbara, California.
- **Y. Tan**, and Z. Chen. "BEOL Compatible TaSx Barrier/Liner Growth and Interaction with Metal Thin Films". In 2021 Semiconductor Research Corporation (SRC), virtual.

Leadership Experience

Conference Committee Chairs Birck Annual Research Conference 2023 - 2025

- Leading and planning the research conference in nanotechnology-related topics for more than 200 people in Midwest universities, including Purdue, UIUC, Notre Dame and etc.
- Coordinating all aspects of the conference, including venue selection, budget management, keynote speaker invitations, and program scheduling.

Team leader of Electric Team RoboMaster August 2019 – May 2020

- Led the Electric team in designing the electric system of the five robots with microcontrollers and PCB design.
- Designed and analyzed the supercapacitor used to improve the stability of the standard robots.
- Held workshop for people who are interested in circuit design and embedded system.

Secretary of Event Planning Purdue Chinese Student and Scholar Association 2016 – 2019

- Conducted several events on campus for Chinese students with local communities, with 80 members in the department of Event Planning.
- Cooperated with other organizations and local restaurants to maximize the welfare of Purdue students.

Achievement, and Affiliations

- **Membership** Phi Kappa Phi; IEEE; MRS
- **Reviewer** for Nanoscale, Advanced Electronic Material, American Chemical Society
- **Ambassador** for Birck Nanotechnology Center (2022 -present)
- **Mentor** in Women of Engineering (2017)
- **Scholarship**, RCA Zworykin Scholarship (2019) Charles W. Brown ECE Scholarship (2019) Eli Shay Scholarship (2018)