

# Yuanqiu(Zoe) Tan

✉ tan213@purdue.edu | 📞 765-337-0010 | 🌐 /in/yuanqiu-tan-zoe | 🐙 yqzoetan.github.io | 🌐 Birck Nanotechnology Center, IN

## EDUCATION

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<b>Purdue University</b> , West Lafayette, IN	Aug 2020 - present
<i>Ph.D. in Electrical Engineering</i> (Advisor: Prof. Zhihong Chen)	GPA: 4.0/4.0
<i>Master of Science in Electrical Engineering</i>	Dec 2024
<b>Purdue University</b> , West Lafayette, IN	Aug 2016 - 2020
<i>Bachelor of Science in Electrical Engineering</i> - Graduate with Highest Distinction	GPA: 3.97/4.0
Minor in Economics	

## RESEARCH SUMMARY

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### Research Focus:

Next-generation computing using 2D materials, ultra-scaled transistors, and probabilistic spin-based architectures. Developed record-performance monolayer 2D TMD FETs, stochastic nanomagnet-based probabilistic computing systems, and BEOL-compatible diffusion barriers. Published in ACS Nano, Nature Communications, Advanced Materials, and more.

### Impact:

Demonstrated innovations bridging materials, devices, and computing, with applications in energy-efficient electronics and emerging probabilistic computing frameworks.

## SKILLS

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**Fabrication:** EBL, Photolithography, PECVD, ALD, RIE, Ion Milling.

**Characterization:** MPMS, PPMS, AFM, SEM, XRD, Raman.

**Software:** Cadence, HSpice, LTspice, TCAD, Python, C, MATLAB, Verilog, Klayout, Solidworks, 3ds Max

## RESEARCH EXPERIENCE

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### Graduate Research Assistant

Birck Nanotechnology Center, IN

Research Assistant

August 2020 - present

### Probabilistic- bit based on Stochastic Low-Barrier-Nanomagnets (LBM) with spin transport on 2D diffusion channel (Funded by US NAVY)

- Developed the stochastic low-barrier nanomagnet stack for both In-plane Magnetic Anisotropy (IMA) and Perpendicular Magnetic Anisotropy (PMA), achieving stochastic operation in kHz.
- Fabricating probabilistic logic arrays combining LBM and 2D spin diffusion, enabling clockless low-energy computing.
- Simulated spin-logic performance using HSpice and validated with non-local spin transport measurements.

### High-performance monolayer TMD devices through defect engineering and doping (Funded by Intel and Semiconductor Research Corporation)

- Developed robust spacer doping strategy, achieving industry-leading p-type  $WSe_2$  FETs with:
  - $SS_{min} = 70$  mV/dec,  $I_{on} = 110 \mu A/\mu m$ ,  $I_{max}/I_{min} > 10^9$

- Stable operation at 50 nm channel length
- Revealed the correlation between off-state electrical performance and Raman spectra.
- Identified defect–performance mechanisms using DFT calculation, EELS, and XPS.
- Demonstrated thermal robustness compatible with BEOL integration

#### **Advanced 2D Material defects and reliability** (Funded by Intel)

- Deposited the contamination-free monolayer TMD materials on TEM grids and studied defect formation, doping chemistry, and interface stability of monolayer TMDs.
- Demonstrated low-energy STEM imaging of monolayers without beam damage.

#### **Large area Ultra-Thin Diffusion Barriers for Scaled Interconnects** (Funded by NSF FuSe2, Semiconductor Research Corporation, Samsung, and EMD)

- Synthesized nanometer-thin TMDs/graphene by BEOL-compatible PECVD.
- Achieved a 50% enhancement in electrical resistivity and revealed its improvement with crystallinity and surface scattering properties.
- Achieved 30% lifetime improvement vs. TaN/Ta in Cu interconnects.

#### **Integration of stochastic Magnetic Tunnel Junctions and 2D-MoS2 FETs for charge-based p-bit** (Funded by NSF)

- Designed a PCB circuit and measurement setup to characterize high-frequency stochastic MTJs in the GHz range with low noise.
- studied the response of stochastic MTJ to temperature and input voltage.

## **OTHER RESEARCH, TEACHING, AND INTERN EXPERIENCE**

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#### **Graduate Research Mentor** Undergrad VIP team in Semiconductor Jan 2023 - 2024

- Mentored 50 students in MOS fabrication, NV-center sensing, and device physics..
- Mentored undergraduate students in semiconductor-related research topics and career paths, connecting students with national labs and industry.

#### **Undergraduate Research Assistant** 2017 - 2020

- Implemented and characterized the invertible Boolean circuits with oscillator-based Ising model and verified with SPICE circuit simulation. (2019 - 2020)
- Conducted electrical characterization and analysis on SiC MOS and  $MoS_2$  device under different annealing conditions.(2019)
- Optimized the analog circuit design for HBC wake-up receiver to improve the accuracy of the main receiver and lower overall power, and minimize potential hazards; Developed the testing circuit for the HBC chip, achieving 200MHz to 1GHz. (2017 - 2018)

#### **Undergraduate Teaching Assistant** (ECE 207, ECE 362, ECE 337) 2018 - 2020

- Instructed students on the concepts of digital circuits, ASIC, and assembly language.
- Supervised and planned undergraduate laboratory for class of 60 students in CMOS circuit analysis, ASIC design and application in STM32 and ESP32.

#### **Technology support and development Intern** (Shandong, China) Summer 2017

- Tested and analyzed the new product with our team to minimize potential problems and provide understandable instructions to customers.

- Tracked and communicated the entire process of production between each department to optimize the standard operation principle minimizing the potential problems.

## PROJECT EXPERIENCE

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### Probabilistic computing based on 3T-1sMTJ for reversible logic (*Cadence*) May 2024

- Developed robust p-bit configurations that capitalize on the inherent stochasticity of low-energy barrier nanomagnets, utilizing a three-transistor and one sMTJ (3T-1sMTJ) design.
- Demonstrated on invertible logic gates and multipliers with stochastic magnetic tunnel junctions (sMTJs) in the realm of probabilistic computing.

### Verilog USB Module on AHB Bus Interfac (*System Verilog*) April 2019

- Designed and implemented a complete USB transmitter and receiver module using Verilog/System Verilog, facilitating data communication between the AHB Bus and USB interface through an integrated data buffer..

### Condiments Express & Six-degree Free Robotic Arms (*CAD, PCB, and Embedded system*) 2019

- Designed and built an automated condiment dispenser with full CAD/PCB design, motorized x-y table, sensors, and BLE-based OLED user interface.
- Engineered robotic arms with six degrees of freedom capable of rotating and grasping objects in multiple directions, integrating user controls via an STM32 microcontroller.

## PUBLICATIONS

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- **Y. Tan**<sup>‡</sup>, R. Tripathi<sup>‡</sup>, S. Bunaiyan, R. Wagner, N. Dilley, S. Datta, K. Camsari, J. Appenzeller, Z. Chen. "Spin Vector Control for Heisenberg-Inspired Probabilistic Computing". *Nature Nano* (under review)
- P. Deng, Y. Meng, Q. Cheng, **Y. Tan**, Z. Chen, T. Li. "Energy-efficient, high-accuracy sensing in loose-fitting textile sensor matrix for LLM-enabled human-robot collaboration". *Nano Energy* (2025) Impact Factor:16.8
- **Y. Tan**, S. Yang, C. Lin, F. Vega, J. Cai, H. Lan, R. Tripathi, S. Sharma, Z. Shang, T. Hou, T. Beechem, J. Appenzeller, Z. Chen. "Monolayer  $WSe_2$  Field Effect Transistor Performance Enhancement by Atomic Defect Engineering and Passivation". *ACS Nano* (2025). Impact Factor:15.8
- H. Lan, C. Lin, L. Liu, J. Cai, Z. Sun, P. Wu, **Y. Tan**, S. Yang, T. Hou, J. Appenzeller, Z. Chen, Uncovering the doping mechanism of nitric oxide in high-performance P-type  $WSe_2$  transistors. *Nature Communication* (2025) Impact Factor:17.7
- H. Lan, **Y. Tan**, S. Yang, X. Liu, Z. Shang, J. Appenzeller, Z. Chen. "Improved Hysteresis of High-Performance p-Type  $WSe_2$  transistors with native oxide  $WO_x$  interfacial layer". *Nanoletter* (2025) Impact Factor:15.8
- J. Daniel, Z. Sun, X. Zhang, **Y. Tan**, N. Dilley, Z. Chen, J. Appenzeller. "Experimental demonstration of an on-chip p-bit core based on stochastic magnetic tunnel junctions and 2D  $MoS_2$  transistors". *Nature Communication* (2024). Impact Factor:17.7
- J. Cai, H. Zhang, **Y. Tan**, Z. Sun, P. Wu, R. Tripathi, S. Krylyuk, C. Suhy, J. Kong, A. Davydov, Z. Chen, J. Appenzeller. "On-Chip Synthesis of Quasi-2D Semimetals from Multi-Layer Chalcogenides". *Advanced Material* (2024). Impact Factor:29.4
- Z. Sun, S. Kim, Jun Cai, J. Shen, H. Lan, **Y. Tan**, X. Wang, C. Shen, H. Wang, Z. Chen, R. Wallace, J. Appenzeller. "Low Contact Resistance on Monolayer  $MoS_2$  Field-Effect Transistors Achieved by CMOS-Compatible Metal Contacts". *ACS Nano* (2024). Impact Factor:15.8

- P. Deng, Y. Wang, R. Yang, Z. He, **Y. Tan**, Z. Chen, J. Liu, T. Li. "Self-Powered Smart Textile Based on Dynamic Schottky Diode for Human-Machine Interactions". *Advanced Science* (2023). Impact Factor:15.1

## ORAL PRESENTATIONS AND PRESENTATION PROCEEDINGS

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- J. Cai, H. Lan, **Y. Tan**, Z. Chen, J. Appenzeller. "First demonstration of DG monolayer  $MoS_2$  FETs with 0.3nm-thin contact extensions achieving near immunity to SCEs at  $L_{CH} = 20\text{nm}$  and  $g_m = 206 \mu\text{S}/\mu\text{m}$ ". *IEDM2025*
- **Y. Tan**, R. Tripathi, J. Appenzeller and Z. Chen. "Nonlocal Detection of Vector Spin Accumulation in Graphene for Probabilistic Computing". In the 2024 Materials Research Society (MRS) Fall Conference, Boston, Massachusetts.
- T. Ngo, **Y. Tan**, A. Zacatzi, D. Lee, A. Wankis, N. Vu, R. Kanjolia, M. Moinpour, Z. Chen. "300mm Wafer-Scale ALD-Grown  $MoS_2$  for Cu Diffusion Barrier". In 2024 IEEE International Interconnect Technology Conference (IITC), San Jose, California.
- **Y. Tan**, and Z. Chen. "High performance monolayer  $WSe_2$  devices through defect engineering and doping". In 2023 Device Research Conference (DRC), Santa Barbara, California.
- **Y. Tan**, and Z. Chen. "BEOL Compatible TaSx Barrier/Liner Growth and Interaction with Metal Thin Films". In 2021 Semiconductor Research Corporation (SRC), virtual.

## LEADERSHIP AND SERVICE

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**Graduate Ambassador** Birck Nanotechnology Center 2022– present

- Outreach, lab tours, mentorship for prospective students.

**President** PUCSSA Dance Club 2024– present

- Organized and led the dance performance in campus-wide events.

**Conference Committee Chairs** Birck Annual Research Conference 2023 - 2025

- Led planning for 200+ attendees across Midwest universities.
- Managed budget, speaker invitations, program design.

**Team leader of Electric Team** RoboMaster August 2019 – May 2020

- Led team building 5 robots, involving design in supercapacitor module, microcontrollers, and PCB design.
- Held workshops for people who are interested in circuit design and embedded systems.

**Secretary of Event Planning** Purdue Chinese Student and Scholar Association 2016 – 2019

- Organized campus-wide events serving 80+ members.
- Partnered with other organizations and local restaurants to maximize the welfare of Purdue students.

**Reviewer** Nanoscale, Advanced Electronic Material, ACS journals

## AWARDS AND HONORS

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- Phi Kappa Phi member; IEEE member; MRS member
- RCA Zworykin Scholarship (2019)
- Charles W. Brown ECE Scholarship (2019)
- Eli Shay Scholarship (2018)