

K. J. SOMAIYA COLLEGE OF ENGINEERING
DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
DC Biasing Circuits

Numerical 1:

Determine the DC bias voltage V_{CE} and the current I_C for the voltage divider configuration in Figure 1. Given $\beta = 140$

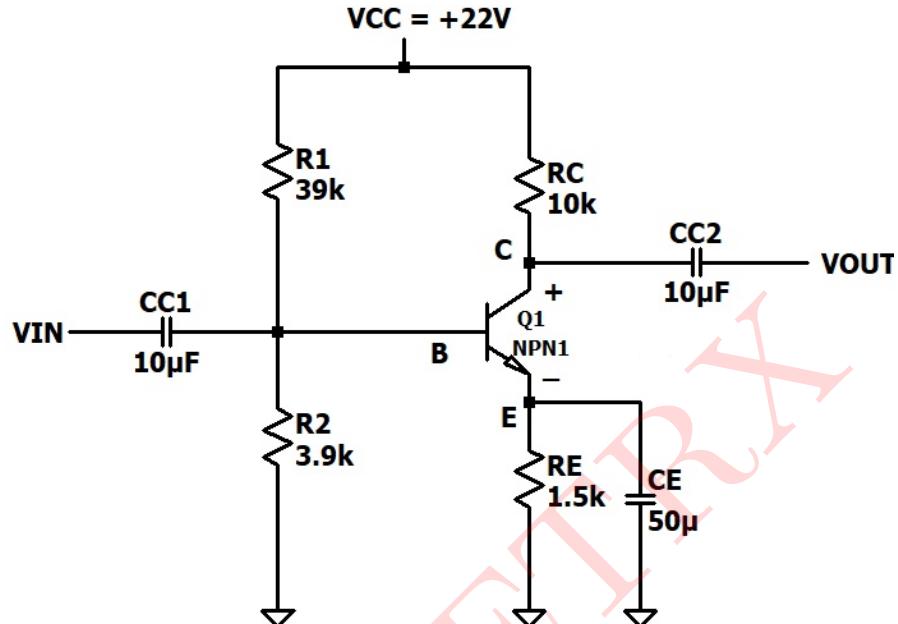


Figure 1: Circuit 1

Solution : The given circuit 1 is a BJT biased in the voltage divider bias configuration. For finding the DC bias voltages and currents we will remove the coupling capacitors C_{C_1} and C_{C_2} .

The input side is redrawn as a Thevenin's equivalent network

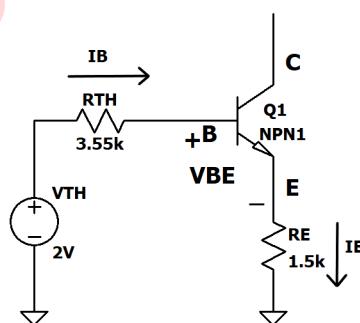


Figure 2: Thevenin's Equivalent Circuit

Now,

$$\begin{aligned}
 R_{th} &= R_1 \parallel R_2 \\
 &= \frac{(39k\Omega)(3.9k\Omega)}{39k\Omega + 3.9k\Omega} \\
 &= 3.55k\Omega
 \end{aligned}$$

$$\begin{aligned}
 V_{th} &= \frac{R_2 V_{CC}}{R_1 + R_2} \\
 &= \frac{(3.9k\Omega)(22V)}{39k\Omega + 3.9k\Omega} \\
 &= \mathbf{2V}
 \end{aligned}$$

Applying KVL to Base Emitter loop,

$$V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

$$\text{Since, } I_E = (\beta + 1)I_B$$

$$V_{th} - I_B R_{th} - V_{BE} - (\beta + 1)R_E = 0$$

$$\begin{aligned}
 I_B &= \frac{V_{th} - V_{BE}}{R_{th} + (\beta + 1)R_E} \\
 &= \frac{2 - 0.7}{3.55k\Omega + (141)(1.5k\Omega)} \\
 &= \mathbf{6.05\mu A}
 \end{aligned}$$

$$\begin{aligned}
 I_C &= \beta I_B \\
 &= 140 \times 6.05\mu A \\
 &= \mathbf{0.85mA}
 \end{aligned}$$

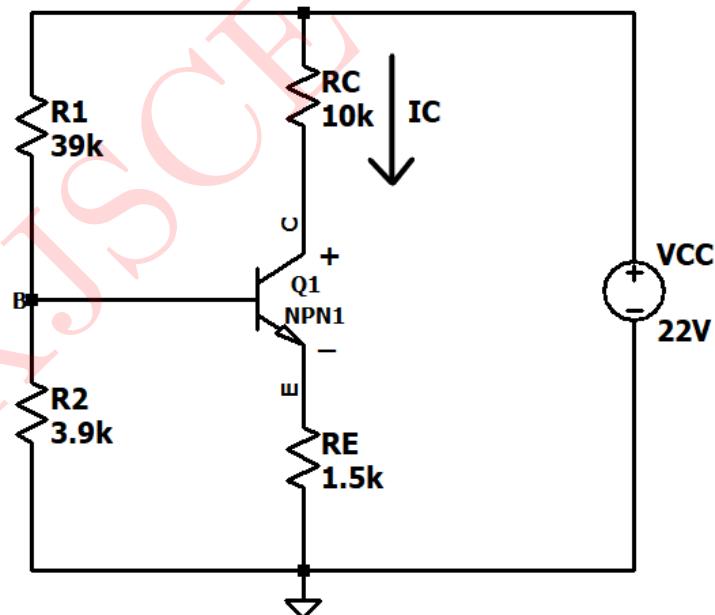


Figure 3: DC Equivalent Circuit

Applying KVL to collector emitter loop,

$$\begin{aligned}
 V_{CE} &= V_{CC} - I_C(R_C + R_E) && [\text{Assuming } I_C \cong I_E] \\
 &= 22V - (0.85mA)(10k\Omega + 1.5k\Omega) \\
 &= 22V - 9.78V \\
 &= \mathbf{12.22V}
 \end{aligned}$$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below

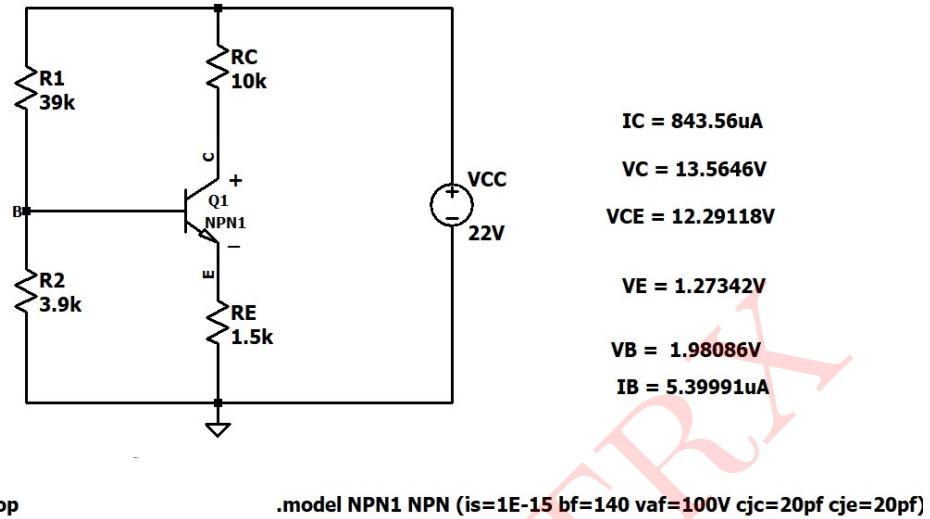


Figure 4: Circuit Schematic: Results

Comparison of Theoretical and Simulated results

Parameters	Theoretical	Simulated
V_{CE}	12.22V	12.29118V
I_C	0.85mA	0.84356mA

Table 1: Numerical 1

Numerical 2:

Determine the quiescent levels of I_{CQ} and V_{CE} for the network shown in Figure 5.

Given $\beta = 90$

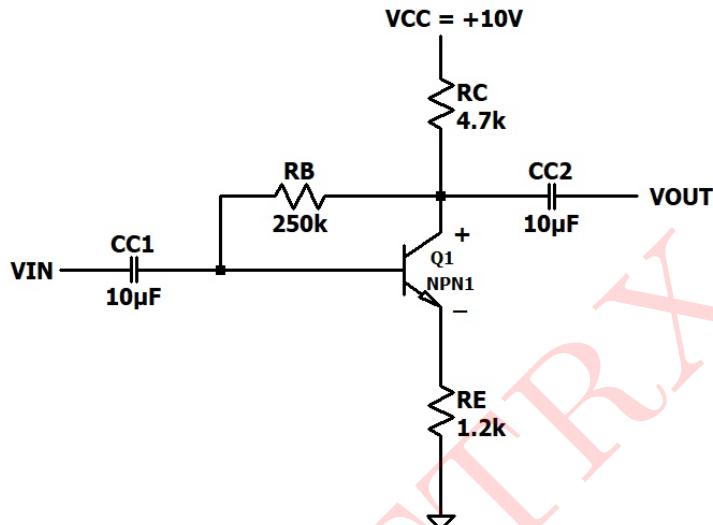


Figure 5: Circuit 2

Solution : The given circuit 2 is a collector to base bias configuration.

To find the quiescent levels, we perform DC analysis hence we remove the coupling capacitors C_{C_1} and C_{C_2}

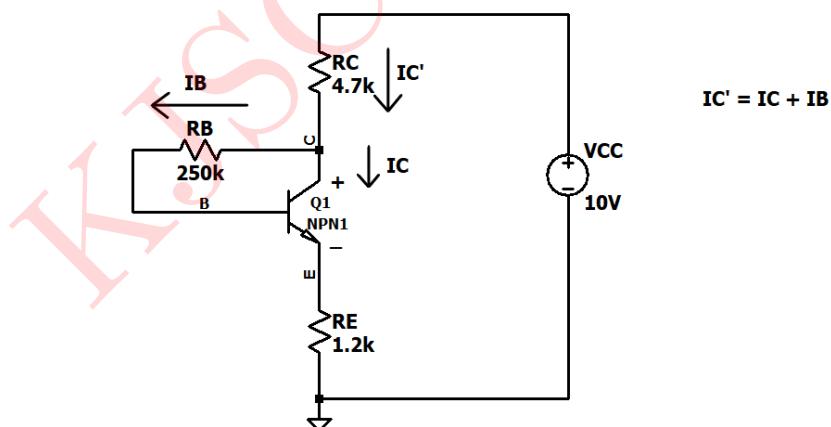


Figure 6: DC Equivalent Circuit

Assuming, $I_C \cong I_E$ and $I_{C'} \cong I_C$

We know, $I_C = \beta I_B$

Applying KVL to Base Emitter loop,

$$V_{CC} - I_C R_C - I_B R_B - V_{BE} - I_C R_E = 0$$

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_B = 0$$

$$\begin{aligned}
I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} \\
&= \frac{10V - 0.7V}{250k\Omega + (90)(4.7k\Omega + 1.2k\Omega)} \\
&= \frac{9.3V}{250k\Omega + 531k\Omega} \\
&= \mathbf{11.91\mu A}
\end{aligned}$$

$$I_{CQ} = \beta I_B = (90)(11.91\mu A) = \mathbf{1.07mA}$$

Applying KVL to Collector Emitter loop,

$$I_E R_E + V_{CE} + I_{C'} R_C - V_{CC} = 0$$

Since, $I_{C'} \cong I_C$ and $I_C \cong I_E$

$$I_C(R_C + R_E) + V_{CEQ} - V_{CC} = 0$$

$$\begin{aligned}
V_{CEQ} &= V_{CC} - I_C(R_C + R_E) \\
&= 10V - (1.07mA)(4.7k\Omega + 1.2k\Omega) \\
&= 10V - 6.31V \\
&= \mathbf{3.69V}
\end{aligned}$$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are as follows

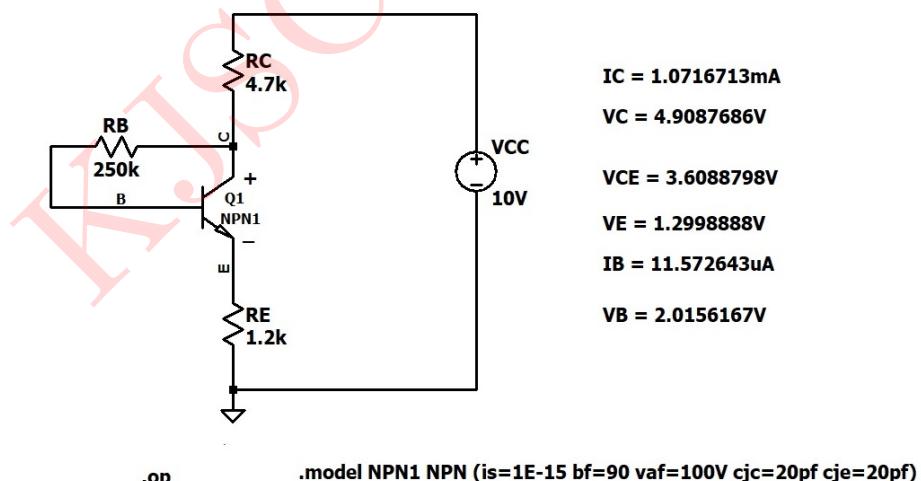


Figure 7: Circuit Schematic: Results

Comparison of Theoretical and Simulated results

Parameters	Theoretical	Simulated
V_{CEQ}	3.69V	3.6088798V
I_{CQ}	1.07mA	1.0716713mA

Table 2: Numerical 2

Numerical 3:

For circuit 3 shown in figure 8, find I_C , V_{CE} & Stability factor. Given $\beta = 100$

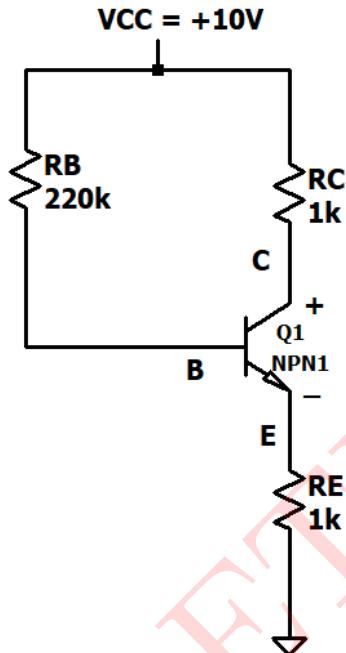


Figure 8: Circuit 3

Solution : The given circuit 3 is a fixed bias configuration

DC Analysis:

Applying KVL to the Base Emitter loop,

$$V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_{CC} - I_B R_B - V_{BE} - (\beta + 1) I_B R_E = 0 \quad [\text{Since, } I_E = (\beta + 1) I_B]$$

$$\begin{aligned} I_B &= \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1) R_E} \\ &= \frac{10V - 0.7V}{(200k\Omega) + (101)(1k\Omega)} \\ &= 28.9\mu\text{A} \end{aligned}$$

$$I_C = \beta I_B = (100)(28.9\mu\text{A}) = 2.89\text{mA}$$

Applying KVL to the Collector Emitter loop,

$$V_{CC} - I_C R_C - V_{CE} - (I_B + I_C) R_E = 0$$

$$V_{CE} = V_{CC} - I_C R_C - (I_B + I_C) R_E$$

$$= 10V - (2.89\text{mA})(1k\Omega) - ((28.9\mu\text{A}) + (2.89\text{mA}))(1k\Omega)$$

$$= 4.19\text{V}$$

Now finding the stability factor,

$$\begin{aligned} S &= \frac{\beta + 1}{1 + \beta \left(\frac{R_E}{R_B + R_E} \right)} \\ &= \frac{100 + 1}{1 + \frac{(100)(1k\Omega)}{220k\Omega + 1k\Omega}} \\ &= \mathbf{69.53} \end{aligned}$$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below

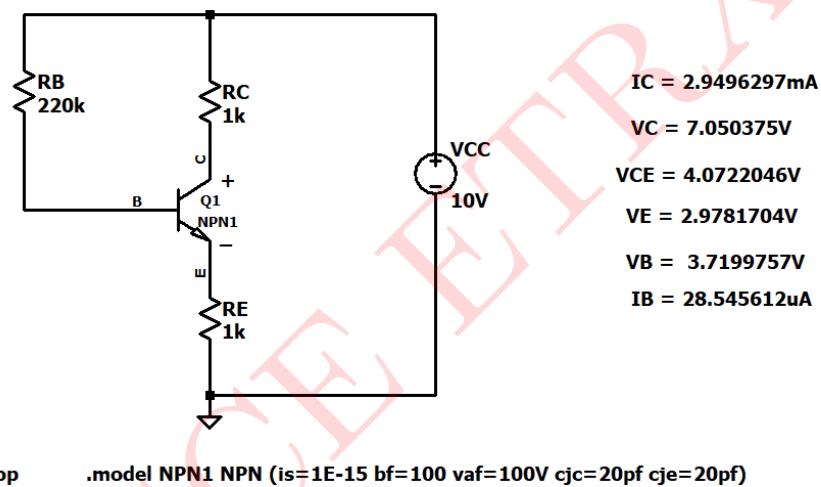


Figure 9: Circuit Schematic: Results

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
I_C	2.89mA	2.9496mA
V_{CE}	4.19V	4.0722V

Table 3: Numerical 3

Numerical 4:

For circuit 4 shown in figure 10, find I_B , I_C & V_{CE} . Given $\beta = 100$

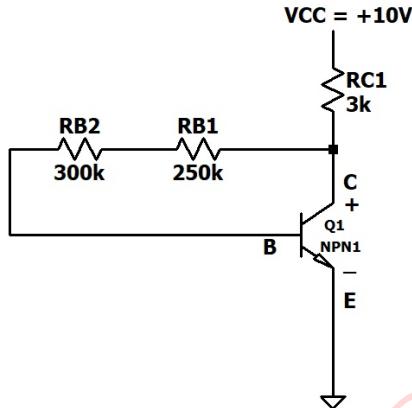


Figure 10: Circuit 4

Solution : The given circuit 4 is a collector to base bias employing npn-BJT.

From the circuit we observe,

$$I_{C'} = I_B + I_C \quad \dots\dots(1)$$

$$\begin{aligned} R_B &= R_{B_1} + R_{B_2} \\ &= 300\text{k}\Omega + 250\text{k}\Omega \\ &= 550\text{k}\Omega \end{aligned}$$

Applying KVL to the input Base Emitter loop,

$$\begin{aligned} V_{CC} - I_{C'} R_C - I_B R_B - V_{BE} &= 0 \\ V_{CC} - (I_B + I_C) R_C - I_B R_B - V_{BE} &= 0 \end{aligned} \quad [\text{Since, } I_C = \beta I_B]$$

$$\begin{aligned} I_B &= \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_C} \\ &= \frac{15V - 0.7V}{(550\text{k}\Omega) + (101)(3\text{k}\Omega)} \\ &= 16.76\mu\text{A} \end{aligned}$$

$$I_C = \beta I_B = (100)(16.76\mu\text{A}) = 1.676\text{mA}$$

Now applying KVL to the outer Collector Emitter loop,

$$V_{CC} - I_{C'} R_C - V_{CE} = 0$$

$$\begin{aligned} V_{CE} &= V_{CC} - (I_B + I_C) R_C \quad [\text{From eq (1)}] \\ &= 15V - ((16.76\mu\text{A}) + (1.676\text{mA}))(3\text{k}\Omega) \\ &= 9.92\text{V} \end{aligned}$$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below

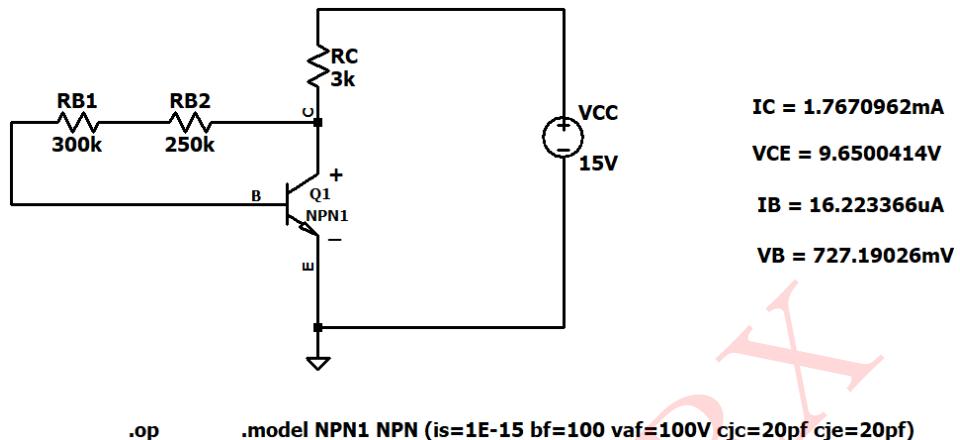


Figure 11: Circuit Schematic: Results

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
I_B	$16.76\mu A$	$16.2233\mu A$
I_C	$1.676mA$	$1.767mA$
V_{CE}	$9.92V$	$9.65V$

Table 4: Numerical 4

Numerical 5:

For the voltage-divider bias configuration in circuit 5, determine
 a. I_{BQ} b. I_{CQ} c. V_{CEQ} d. V_C e. V_E f. V_B [Given $\beta = 80$]

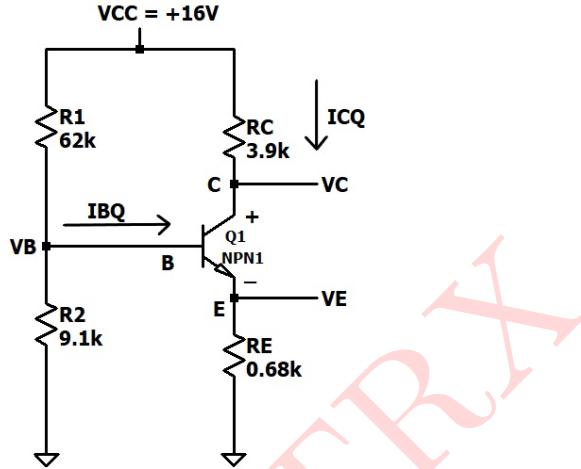


Figure 12: Circuit 5

Solution: The given circuit 5 is a npn BJT biased in voltage divider configuration. The input side is redrawn as a Thevenin's equivalent network:

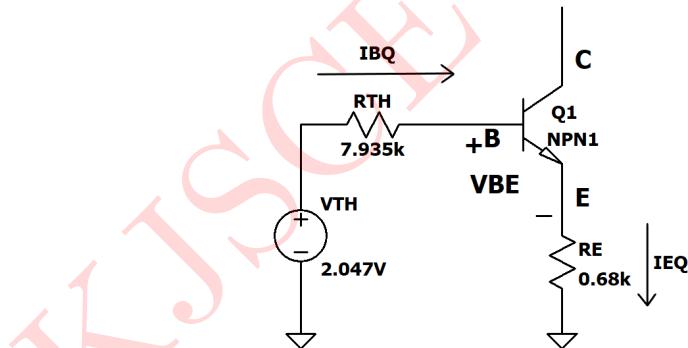


Figure 13: Thevenin's Equivalent Circuit

$$\begin{aligned} R_{TH} &= R_1 \parallel R_2 \\ &= \frac{(62k\Omega)(9.1k\Omega)}{62k\Omega + 9.1k\Omega} \\ &= 7.935k\Omega \end{aligned}$$

$$\begin{aligned} V_{TH} &= \frac{R_2 V_{CC}}{R_1 + R_2} \\ &= \frac{(9.1k\Omega)(16V)}{62k\Omega + 9.1k\Omega} \\ &= 2.047V \end{aligned}$$

Applying KVL to input Base Emitter loop,

$$V_{TH} - I_{BQ}R_{TH} - V_{BE} - I_{EQ}R_E = 0$$

$$V_{TH} - I_{BQ}R_{TH} - V_{BE} - (\beta + 1)I_{BQ}R_E = 0$$

[Since, $I_E = (\beta + 1)I_B$]

$$\begin{aligned}
I_{BQ} &= \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E} \\
&= \frac{2.047V - 0.7V}{(7.935k\Omega) + (81)(0.68k\Omega)} \\
&= \mathbf{21.375\mu A}
\end{aligned}$$

$$\begin{aligned}
I_{CQ} &= \beta I_{BQ} \\
&= (80)(21.375\mu A) \\
&= \mathbf{1.71mA}
\end{aligned}$$

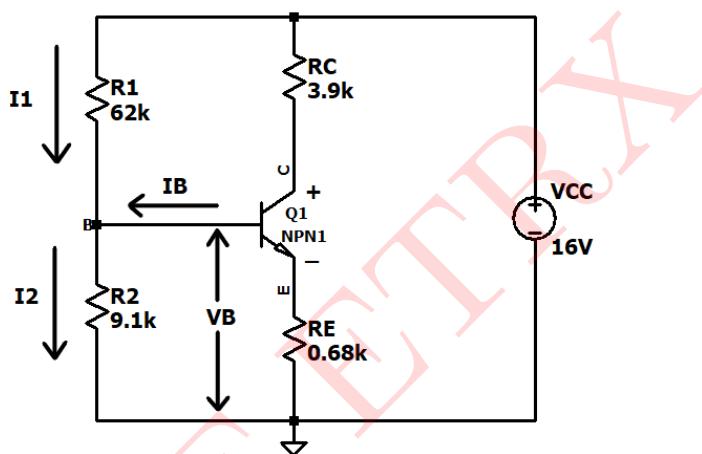


Figure 14: DC Equivalent Circuit

Applying KVL to Collector Emitter loop,

$$\begin{aligned}
V_{CEQ} &= V_{CC} - I_{CQ}(R_C + R_E) && [\text{Assuming } I_C \cong I_E] \\
&= 16V - (1.71mA)(3.9k\Omega + 0.68k\Omega) \\
&= \mathbf{8.1682V} && \dots\dots(1)
\end{aligned}$$

Applying KVL upto the collector terminal in output Collector Emitter loop,

$$\begin{aligned}
V_C &= V_{CC} - I_C R_C \\
&= 16V - (1.71mA)(3.9k\Omega) \\
&= \mathbf{9.331V}
\end{aligned}$$

$$V_{CE} = 8.1682V \quad [\text{From eq (1)}]$$

$$V_C - V_E = 8.1682V$$

$$9.331 - V_E = 8.1682V$$

$$V_E = \mathbf{1.1628V}$$

For the calculation of V_B , we use approximate analysis,

$$\beta R_E = 80 \times 0.68\text{k}\Omega$$

$$= 54.4\text{k}\Omega$$

$$10R_2 = 10 \times 3.9\text{k}\Omega$$

$$= 39\text{k}\Omega$$

$$\text{Thus, } \beta R_E \geq 10R_2$$

Hence, we can say that current I_B will be much smaller than I_2 , if we approximate that I_B is essentially 0A compared to I_1 and I_2 , and $I_1 \cong I_2$, then the base voltage is the voltage across R_2 .

$$\therefore V_B = \frac{R_2 V_{CC}}{R_1 + R_2} = 2.047\text{V}$$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below

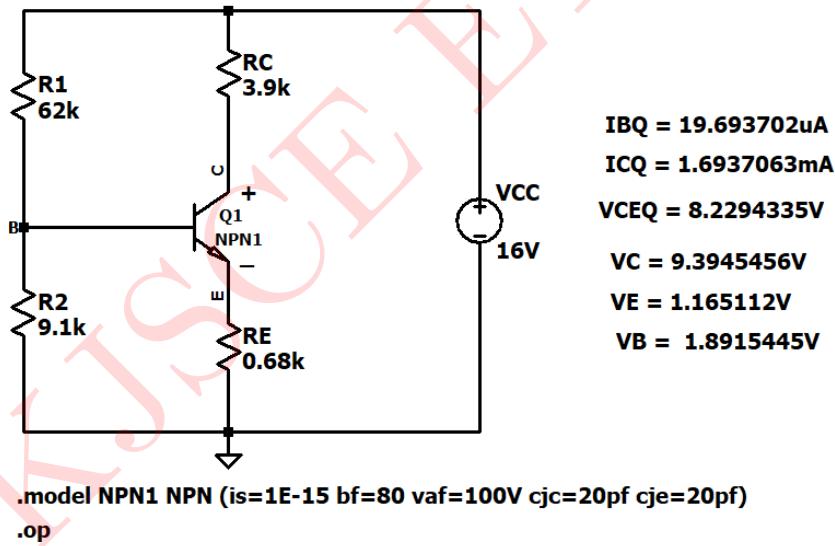


Figure 15: Circuit Schematic: Results

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
I_{BQ}	$21.375\mu\text{A}$	$19.693\mu\text{A}$
I_{CQ}	1.71mA	1.6937mA
V_{CEQ}	8.1682V	8.2294V
V_C	9.331V	9.3945V
V_E	1.1628V	1.1651V
V_B	2.047V	1.8915V

Table 5: Numerical 5

Numerical 6:

For the Collector to Base bias configuration in circuit 6, determine
 a. I_B b. I_C c. V_C [Given $\beta = 120$]

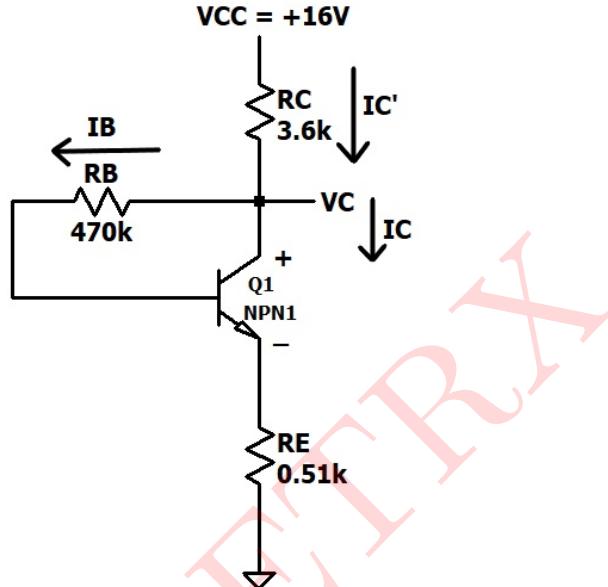


Figure 16: Circuit 6

Solution : The given circuit 6 is a Collector to Base bias employing a npn BJT.

DC Analysis:

Assuming $I_C \cong I_E$ and $I'_C \cong I_C$

Applying KVL to input Base Emitter loop,

$$V_{CC} - I_C R_C - I_B R_B - V_{BE} - I_C R_E = 0$$

$$V_{CC} - V_{BE} - \beta I_B (R_C + R_E) - I_B R_B = 0$$

$$\begin{aligned} I_B &= \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)} \\ &= \frac{16V - 0.7V}{(470k\Omega) + (120)(3.6k\Omega + 0.51k\Omega)} \\ &= 15.817\mu A \end{aligned}$$

$$\begin{aligned} I_C &= \beta I_B \\ &= (120)(15.817\mu A) \\ &= 1.898mA \end{aligned}$$

Applying KVL upto the collector terminal in output Collector Emitter loop,

$$V_C = V_{CC} - I_C R_C$$

$$= 9.1682V$$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below

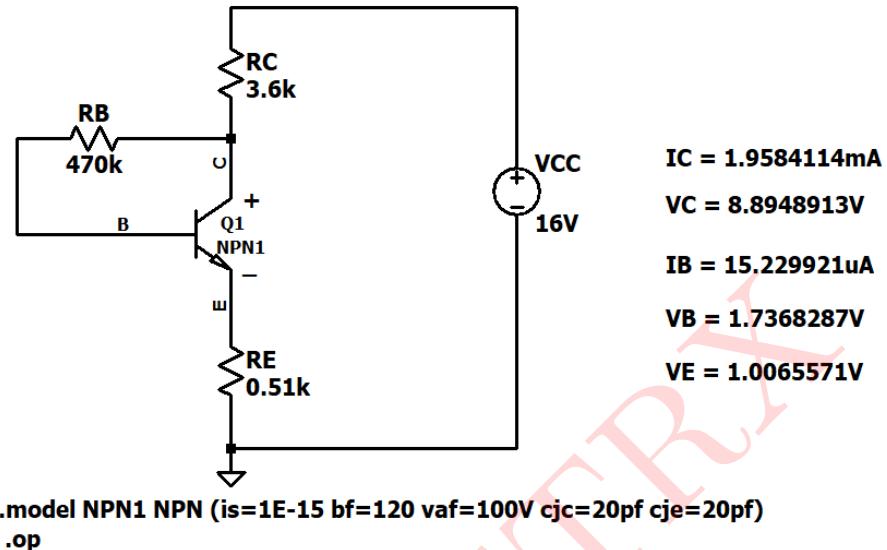


Figure 17: Circuit Schematic: Results

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
I_B	$15.817\mu A$	$15.2299\mu A$
I_C	$1.898mA$	$1.9584mA$
V_C	$9.1672V$	$8.8948V$

Table 6: Numerical 6

Numerical 7:

For the circuit given in figure 18, find

a. R_{TH} & V_{TH} for the base circuit. b. Determine I_{BQ} , I_{CQ} , V_E , V_C

Given $\beta = 60$

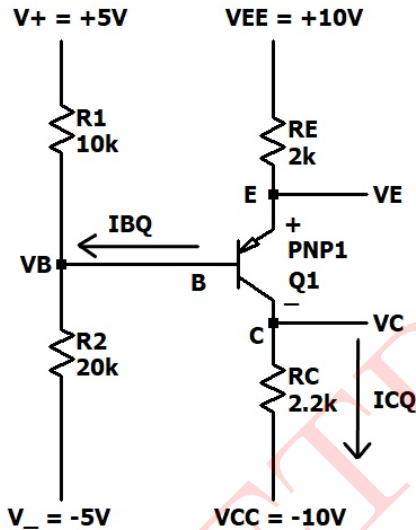


Figure 18: Circuit 7

Solution: The given circuit 7 employs a pnp BJT.

The input side is redrawn as a Thevenin's equivalent network:

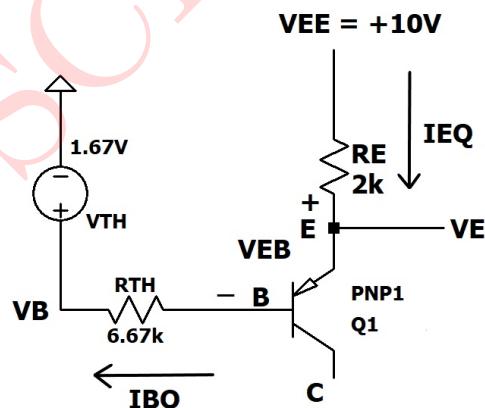


Figure 19: Thevenin's Equivalent Circuit

$$\begin{aligned} R_{TH} &= R_1 \parallel R_2 \\ &= \frac{(10k\Omega)(20k\Omega)}{10k\Omega + 20k\Omega} \\ &= 6.67k\Omega \end{aligned}$$

$$\begin{aligned} V_{TH} &= \left(\frac{R_2}{R_1 + R_2} \right) (V_+ - V_-) + V_- \\ &= \left(\frac{20k\Omega}{10k\Omega + 20k\Omega} \right) (5 - (-5)) - 5 \\ &= 1.67V \end{aligned}$$

Applying KVL to input Base Emitter loop,

$$V_{EE} - I_{EQ}R_E - V_{EB} - I_{BQ}R_{TH} - V_{TH} = 0$$

$$V_{EE} - (1 + \beta)I_{BQ}R_E - V_{EB} - I_{BQ}R_{TH} - V_{TH} = 0$$

[Since, $I_E = (1 + \beta)I_B$]

$$\begin{aligned} I_{BQ} &= \frac{V_{EE} - V_{EB} - V_{TH}}{R_{TH} + (1 + \beta)R_E} \\ &= \frac{10V - 0.7V - 1.67V}{(6.67k\Omega) + (61)(2k\Omega)} \\ &= \mathbf{59.3\mu A} \end{aligned}$$

$$I_{CQ} = \beta I_{BQ} = \mathbf{3.56mA}$$

$$I_{EQ} = (1 + \beta)I_{BQ} = \mathbf{3.62mA}$$

Applying KVL to output Collector Emitter loop,

$$V_E = V_{EE} - I_{EQ}R_E$$

$$= 10 - (3.62mA)(2k\Omega)$$

$$= \mathbf{2.76V}$$

$$V_C = I_{CQ}R_C - V_{CC}$$

$$= (3.56mA)(2.2k\Omega) - (-10)$$

$$= \mathbf{-2.168V}$$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below:

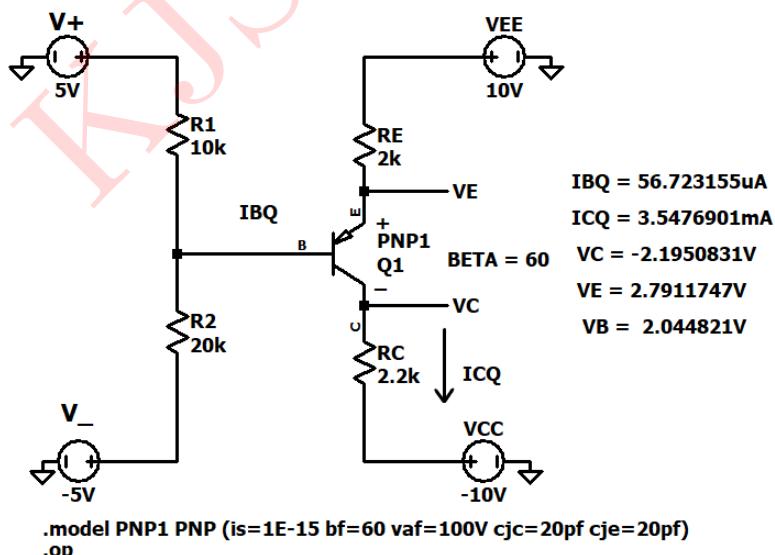


Figure 20: Circuit Schematic: Results

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
I_{BQ}	$59.3\mu A$	$56.723\mu A$
I_{CQ}	$3.56mA$	$3.5476mA$
V_E	$2.76V$	$2.7911V$
V_C	$-2.168V$	$-2.19508V$

Table 7: Numerical 7

Numerical 8:

For the circuit given in figure 21, find

a. V_{TH} & R_{TH} for the base circuit. b. Determine I_{CQ} & V_{CEQ}

Given $\beta = 100$

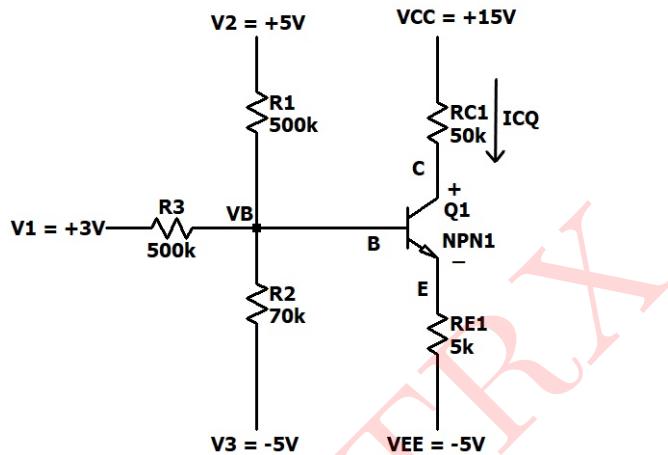


Figure 21: Circuit 8

Solution: The given circuit 8 employs a npn BJT.

The input side is redrawn as a Thevenin's equivalent network:

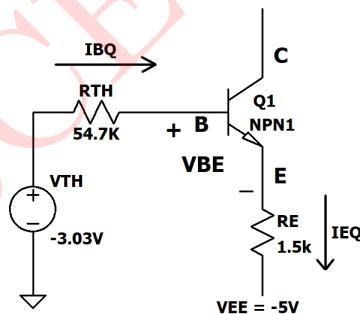


Figure 22: Thevenin's Equivalent Circuit

$$\begin{aligned}
 R_{TH} &= R_1 \parallel R_2 \parallel R_3 \\
 &= 500k \parallel 500k \parallel 70k \\
 &= 250k \parallel 70k \\
 &= \frac{(250k\Omega)(70k\Omega)}{250k\Omega + 70k\Omega} \\
 &= \mathbf{54.7k\Omega}
 \end{aligned}$$

Applying KCL at B node,

$$\begin{aligned}
 \frac{5V - V_{TH}}{500k\Omega} + \frac{3V - V_{TH}}{500k\Omega} &= \frac{V_{TH} - (-5V)}{70k\Omega} \\
 \frac{5V}{500k\Omega} + \frac{3V}{500k\Omega} - \frac{5}{70k\Omega} &= V_{TH} \left(\frac{1}{500k\Omega} + \frac{1}{500k\Omega} + \frac{1}{70k\Omega} \right) \\
 V_{TH} &= \mathbf{-3.03V}
 \end{aligned}$$

Applying KVL to input Base Emitter loop,

$$V_{TH} - I_{BQ}R_{TH} - V_{BE} - I_{EQ}R_E - V_{EE} = 0$$

$$-V_{EE} + V_{TH} - I_{BQ}R_{TH} - V_{BE} - (1+\beta)I_{BQ}R_E = 0$$

[Since, $I_E = (1+\beta)I_B$]

$$\begin{aligned} I_{BQ} &= \frac{V_{TH} - V_{BE} - V_{EE}}{R_{TH} + (1 + \beta)R_E} \\ &= \frac{-3.03 - 0.7 - (-5)}{(54.7k\Omega) + (101)(5k\Omega)} \\ &= 2.27\mu\text{A} \end{aligned}$$

$$I_{CQ} = \beta I_{BQ} = 0.227\text{mA}$$

$$I_{EQ} = (1 + \beta)I_{BQ} = 0.229\text{mA}$$

Applying KVL to output Collector Emitter loop,

$$\begin{aligned} V_{CEQ} &= V_{CC} - I_{CQ}R_C - I_{EQ}R_E - V_{EE} \\ &= 15V - (0.227\text{mA})(50k\Omega) - (0.229\text{mA})(5k\Omega) - (-5) \\ &= 7.505\text{V} \end{aligned}$$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below:

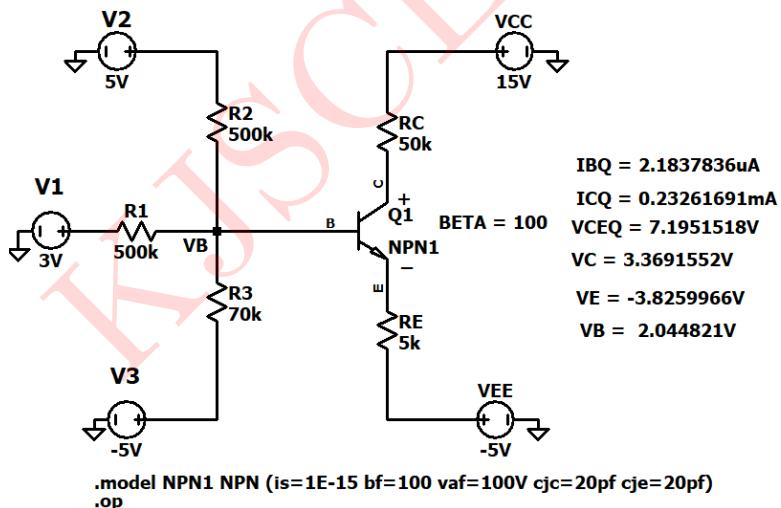


Figure 23: Circuit Schematic: Results

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
I_{CQ}	0.227mA	0.2326mA
V_{CEQ}	7.505V	7.19515V

Table 8: Numerical 8

Numerical 9:

The NMOS amplifier shown in circuit 9 has $V_{DD} = 15V$, $R_S = 500\Omega$, $R_L = 10k\Omega$, $R_{SR} = 3k\Omega$, $R_D = 5k\Omega$, $R_{G_1} = 700k\Omega$, $R_{G_2} = 300k\Omega$, $V_T = 2.4V$ and $k_n = 2.042mA/V^2$. Calculate V_{GS} , I_D and V_{DS}

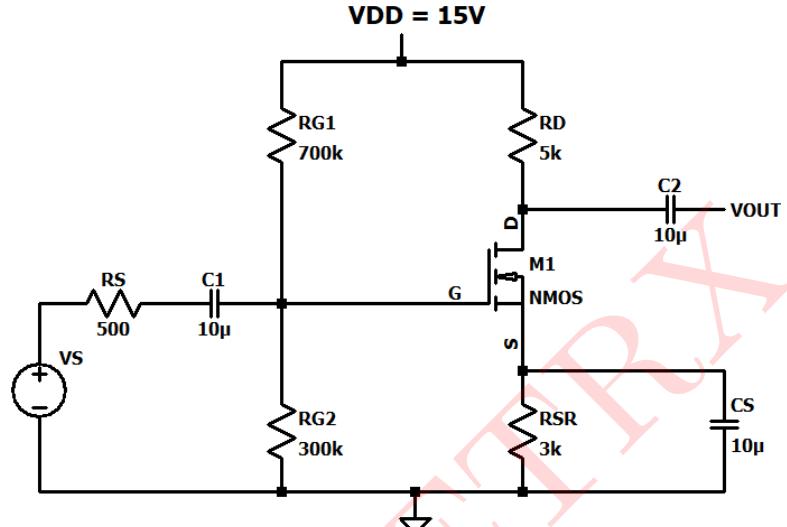


Figure 24: Circuit 9

Solution: The given circuit 8 is a voltage divider bias employing an enhancement mode n-channel MOSFET.

For the DC analysis we will remove the capacitors,

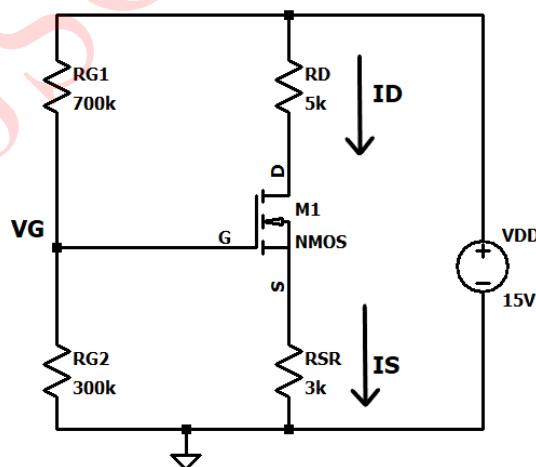


Figure 25: DC Equivalent Circuit

From the circuit we observe,

$$\begin{aligned}
 V_G &= \frac{R_{G_2}}{R_{G_1} + R_{G_2}} \times V_{DD} && [\text{Assuming } I_G \cong 0] \\
 &= \frac{300k\Omega}{700k\Omega + 300k\Omega} \times 15 \\
 &= 4.5V
 \end{aligned}$$

Applying KVL to Gate-Source loop,

$$V_G - V_{GS} - I_D R_{SR} = 0 \quad [\text{Assuming } I_D \cong I_S]$$

$$V_{GS} = 4.5 - (3k\Omega)I_D$$

$$I_D = \frac{4.5 - V_{GS}}{3k\Omega} \quad \dots\dots(1)$$

In Saturation region,

$$I_D = k_n [V_{GS} - V_T]^2$$

Substituting equation (1) in above equation,

$$\frac{4.5 - V_{GS}}{3k\Omega} = (2.042 \times 10^{-3}) (V_{GS} - 2.4)^2$$

$$4.5 - V_{GS} = 6.126 \times (V_{GS}^2 - 4.8V_{GS} + 5.76)$$

$$6.126V_{GS}^2 - 28.4048V_{GS} + 30.78576 = 0$$

$$\therefore V_{GS} = 2.9V \quad \text{or} \quad V_{GS} = 1.727V$$

For the transistor to be in saturation, $V_{GS} > V_T$

$$\therefore V_{GS} = \mathbf{2.9V}$$

Applying KVL to Drain Source loop,

$$V_{DS} = V_{DD} - I_D(R_D + R_{SR}) \quad [\text{Assuming } I_D \cong I_S]$$

$$= 15 - \left(\frac{4.5 - 2.9}{3k\Omega} \right) (5k\Omega + 3k\Omega) \quad \dots\dots[\text{From (1)}]$$

$$= \mathbf{10.733V}$$

From equation (1),

$$I_D = \frac{4.5 - V_{GS}}{3k\Omega}$$

$$= \frac{4.5 - 2.9}{3k\Omega}$$

$$= 5.333 \times 10^{-4} A = \mathbf{0.533mA}$$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below:

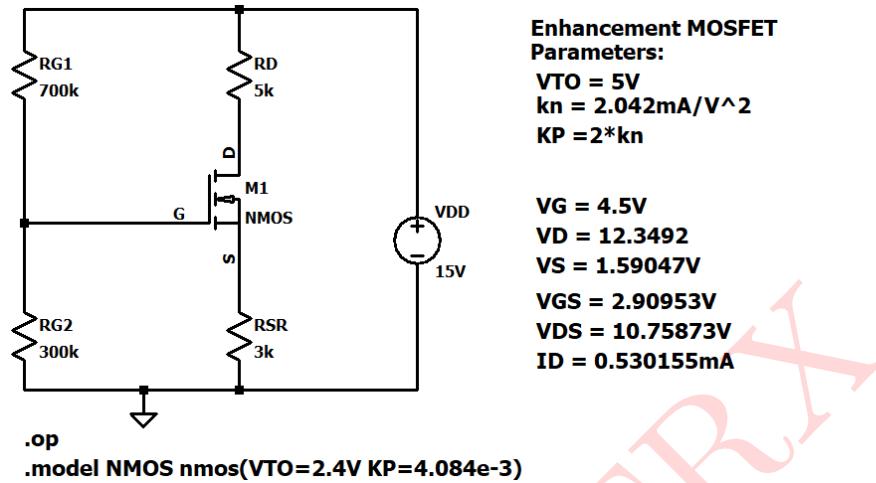


Figure 26: Circuit Schematic: Results

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
V_{GS}	2.9V	2.909V
I_D	0.533mA	0.5301mA
V_{DS}	10.733V	10.7587V

Table 9: Numerical 9

Numerical 10:

The MOSFET amplifier shown in circuit 10 has $R_S = 500\Omega$, $R_1 = 30k\Omega$, $R_2 = 50k\Omega$, $R_D = 10k\Omega$ and $R_L = 15k\Omega$. Assume $V_M = -200V$, $V_T = 2V$ and $k_n = 30mA/V^2$. Calculate V_{DS} , I_D and V_{GS}

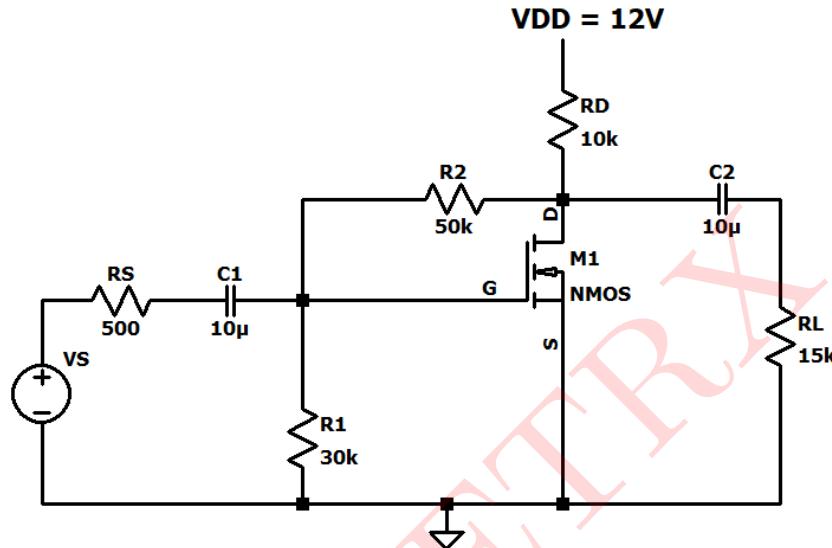


Figure 27: Circuit 10

Solution: The given circuit 10 employ a enhancement type n-channel MOSFET.

$$\lambda = \frac{1}{|V_M|} = 0.005V^{-1}$$

For the DC analysis we will remove all the coupling capacitors,

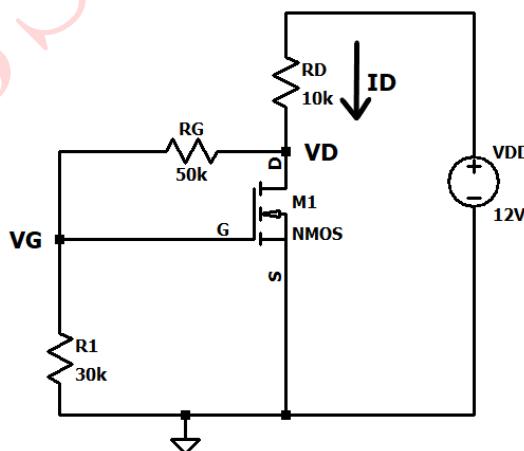


Figure 28: DC Equivalent Circuit

From the circuit we can observe that the source terminal is connected to the ground, hence $V_S = 0$

Also,

$$V_{DS} = V_D - V_S = V_D$$

$$V_{GS} = V_G - V_S$$

$$V_{GS} = V_G = \left(\frac{R_1}{R_1 + R_2} \right) V_{DS}$$

[Since, $V_{DS} = V_D$]

$$V_{DS} = \frac{V_{GS}(R_1 + R_2)}{R_1}$$

$$= \frac{V_{GS}(30k\Omega + 50k\Omega)}{30k\Omega}$$

$$= \frac{8}{3}V_{GS}$$

.....(1)

Applying KVL to Drain Source loop,

$$V_{DS} = V_{DD} - I_D R_D$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D}$$

$$= \frac{V_{DD} - \frac{8}{3}V_{GS}}{R_D}$$

.....[From (1)]

$$= \frac{12 - \frac{8}{3}V_{GS}}{10k\Omega}$$

.....(2)

In Saturation region,

$$I_D = k_n [V_{GS} - V_T]^2 (1 + \lambda V_{DS})$$

Substituting I_D from equation (2) and V_{DS} from equation (1),

$$\frac{V_{DD} - \frac{8}{3}V_{GS}}{10k\Omega} = (30 \times 10^{-3}) (V_{GS} - 2)^2 \left(1 + \frac{0.005 \times 8}{3}V_{GS} \right)$$

$$12 - \frac{8}{3}V_{GS} = 300(V_{GS}^2 - 4V_{GS} + 4) \left(1 + \frac{V_{GS}}{75} \right)$$

$$4V_{GS}^3 + 284V_{GS}^2 - 1181.33V_{GS} + 1185 = 0$$

$$\therefore V_{GS} = -74.99V \quad \text{or} \quad V_{GS} = 2.1726V \quad \text{or} \quad V_{GS} = 1.818V$$

For the transistor to be in saturation, $V_{GS} > V_T$

$$\therefore V_{GS} = \mathbf{2.1726V}$$

Substituting the value of V_{GS} in equation (1),

$$V_{DS} = \frac{8 \times 2.1726}{3}$$

$$= \mathbf{5.717V}$$

Substituting the value of V_{GS} & V_{DS} in equation (2),

$$I_D = \frac{12 - \frac{8}{3} \times 2.1726}{10k\Omega}$$

$$= \mathbf{0.620mA}$$

SIMULATED RESULTS

The above circuit is simulated in LTspice and results are presented below:

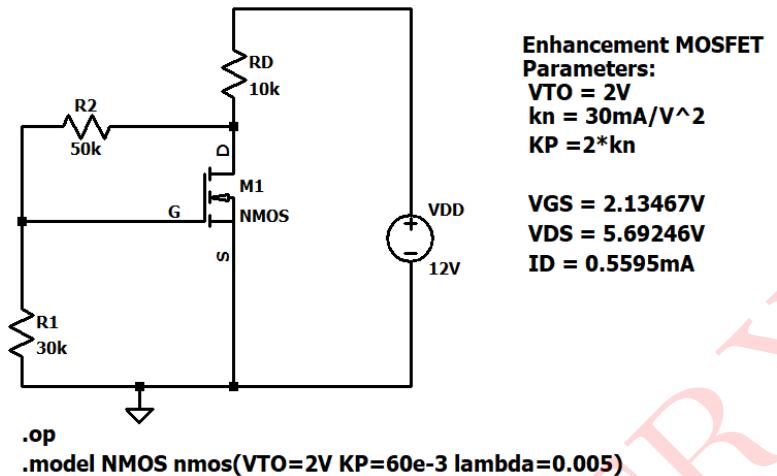


Figure 29: Circuit Schematic: Results

Comparison of Theoretical and Simulated results:

Parameters	Theoretical	Simulated
V_{GS}	2.1726V	2.13467V
I_D	0.620mA	0.5595mA
V_{DS}	5.717V	5.69246V

Table 10: Numerical 10
