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Lab 1 Report

ECEN 449-503

Due: 1 February 2016

Introduction
The purpose of this lab was to familiarize ourselves with the Xilinx ISE and FPGA. Most of the content in this lab was review.

Procedure
The first part of this lab involved compiling the source code provided and loading it onto the FPGA. The provided code would turn on certain LEDS when a corresponding switch was flipped.

The second part of the lab involved implementing an LED counter in Verilog. The LEDs would count up/down depending on if the corresponding up/down button was pressed. If the reset button was pressed, the LED counter would be reset back to zero. Since the built in clock on the FPGA was too fast, it was divided into a slower clock that ran at 1Hz.

The final part of this lab involved implementing a Jackpot game. One LED would turn on at a time. If the switch corresponding to that specific LED was turned on when the LED was lit, the user would win and all the lights would turn on. Different states were created for the different LEDs and winning conditions.

Results / Q&A
All three parts of the lab were working correctly. Debugging was necessary as some Verilog code would not map correctly to the FPGA. Some updates were made to the .ucf file to prevent some compile warnings and errors.

The push button signals are pulled up when the button is pressed. They're corresponding pin identifiers are:

- SW10 = N (GPIO North) = U8
- SW11 = S (GPIO South) = V8
- SW12 = E (GPIO East) = AK7
- SW13 = W (GPIO West) = AJ7
- SW14 = C (GPIO Center) = AJ6

The purpose of an edge detection circuit is to provide specific situations in which an always block is triggered. Without edge detection, an always block will be triggered whenever there is an event (or a change in the condition value). Edge detection allows the designer to control which types of events trigger the always block.

Conclusion
In conclusion, this lab provided a good "warm up" for future labs and Verilog coding. This lab highlighted how some aspects of Verilog would not work on the FPGA board (for example: time delays). The skills used in this lab will be vital to future work with Verilog and FPGA boards.