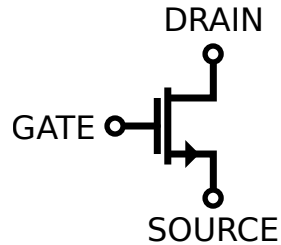# Zero to ASIC: Analogue Design

Thomas Parry

1 Fundamentals of the MOSFET

The MOSFET (Metal-Oxide Semiconductor Field Effect Transistor) is the fundamental building block of modern IC design.

The MOSFET is a *transconductance* device which translates a voltage between it's gate and source terminals to a current between the drain and source - assuming the device is biased correctly.

(a) The Saturation Region

Most devices in a circuit will be operating in saturation where the following description of the current is given for a square-law device:

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 \tag{1}$$

This can be simplified to:

$$I_D = K_n \frac{W}{L}V_{OD}^2 \tag{2}$$

$$given\ that: \quad V_{DS} > V_{OD} \tag{3}$$

The condition is very important, if you want your FET to work as expected you must ensure you have sufficient V_{DS} headroom. The value V_{OD} is also more commonly called $V_{D_{SAT}}$ and is defined as the minimum drain voltage required to keep the device in saturation. Note that in sub-micron processes (like Skywater 130 nm) the statement that $V_{D_{SAT}} = V_{OD}$ is not fully accurate due to second order effects from device scaling.

(b) The Triode Region

When there is insufficient drain-source voltage (by design or error) the device will work in the triode region where it approximates a voltage controlled resistor:

$$I_D = \mu_n C_{ox} \frac{W}{L}\left((V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right) \tag{4}$$

(c) The Cutoff Region

When there is insufficient voltage across the gate-source terminals the device is 'off':

$$I_D = 0 \quad given\ that: \quad V_{GS} << V_{TH} \tag{5}$$

> Always know the region you expect your FET to operate and check that you have it correctly biased or all other assumptions are broken.

2 Basics of Transconductance Efficiency

The transconductance is the amount of current in the drain per gate-source voltage.

$$i_d = g_m \cdot v_{gs} \tag{6}$$

This simple diagram shows the most important concept of the FET: a voltage at the input is converted to an output current. This output current will later be converted by an impedance to another voltage.
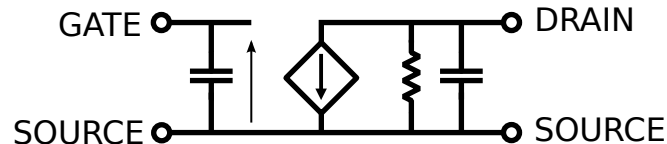
The transconductance can be expressed as a function of the bias current, giving the g_m/I_d value. This value is related to how inverted the channel of the FET is - a measure of how 'turned on' the FET is. The measure of channel inversion is how many minority charge carriers have been attracted to the conductive channel between the source and drain.

(a) Transconductance Efficiency and Overdrive Voltage

There is a relation to the overdrive voltage mentioned above, V_{OD}. The higher the V_{OD}, the more the FET is 'turned on', and therefore the more the FET channel is inverted, which leads to a *lower* g_m/I_d. Conversely, a lower V_{OD} turns on the FET less, and therefore the FET channel is less inverted, which leads to a *higher* g_m/I_d.

(b) Realistic Values of Transconductance Efficiency

There is a range of transconductance efficiencies that can be obtained in standard CMOS processes. It is reasonable to assume a maximum transconductance efficiency of 20 in design equations, although in some specific cases values of 25 can be reached. Typically a device will not be used below a transconductance efficiency of 4.

(c) Why Use Transconductance Efficiency?

While transconductance efficiency, g_m/I_d, feels very abstract at first, its use lies in two factors.

1. It gives a strong indication of the channel inversion.

2. It allows quick calculation of circuit currents and other conditions.

For example, if I have determined I will use a FET in weak inversion and I need $1\ mS$ of transconductance, then I very simply know the required current of $50\ \mu A$.

> But how do we know what transconductance we should use for a given FET? We'll discuss this in the next section where I will talk about the relation of matching and noise to transconductance.

Further Reading (clickable)
    gm/ID - Based Design
    An Introduction to the EKV Model and a comparison of EKV to BSIM

3 Noise, Offset and Transconducance

(a) Noise

Considering only thermal noise the drain noise in a MOSFET is given by:

$$\frac{i_{n,d}^2}{\Delta f} = 4KT\gamma g_{do} \tag{7}$$

Where the K is the Boltzmann's constant and T is absolute temperature. We will set the device specific parameter $\gamma = 1$ for simplicity. The zero bias drain conductance, g_{do}, can be approximated to g_m.

$$\frac{i_{n,d}^2}{\Delta f} \approx 4KTg_m \tag{8}$$

So now we can see that the current noise in the drain of a MOSFET **increases** with increasing transconductance. However, to complete the story we can also refer the noise to the gate. To do this we divide the noise power above by the power transfer function of the MOSFET, g_m^2, to give:

$$\frac{v_{n,d}^2}{\Delta f} \approx \frac{4KT}{g_m} \tag{9}$$

Now we see that expressed as a input referred noise source the noise **decreases** with increasing g_m. This is because the increasing gain of the MOSFET overpowers the increasing noise in the channel. The result also complies with the intuition formed by Friis' equation.

(b) Offset

All MOSFETs are fabricated with random variations which exhibit as mismatch offset between ideally identical devices. The largest contributor to offset is due to the gate-source threshold voltage offset. Pelgrom proposed the following model for offset which is widely adopted:

$$\sigma_{\Delta V_{TH}} = \frac{A_{VTH}}{\sqrt{WL}} \tag{10}$$

This states that the standard deviation of the mismatch between two devices is a process specific value divided by the square root of the area of the device (assuming both devices are identical). The SKY130 process does not have a published figure for A_{VTH} but using $10\ mV\,\mu m$ is reasonable.

Consider the small signal description of the FETs transfer:

$$i = g_m \cdot v_{GS} \tag{11}$$

Where we then add an offset:

$$i = g_m \cdot (v_{GS} + \Delta V_{TH}) \tag{12}$$

We can see that the offset voltage is transferred to the current as a function of g_m. So for small drain current offset we need a low g_m.

Considering a voltage amplilfier, the original threshold offset cannot be improved but any offset further down the system can be modelled as input referred but divided by g_m. Therefore, we want a high g_m, this tracks with Friis' equation.

4 The Current Mirror

The most important circuit in analogue design is the current mirror. This circuit is used as the building block for a huge amount of applications.
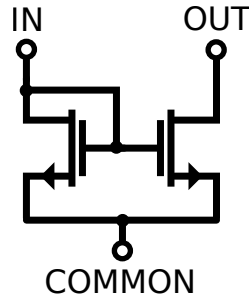
(a) Circuit Operation

The input current is fed into a diode-connected FET. This diode-connected FET generates a voltage on it's gate which is approximately equal to:

$$V_{GS} = \sqrt{I_{IN} \frac{1}{K_n} \frac{L}{W}} + V_{TH} \tag{13}$$

This voltage is then applied to the gate of the second FET. Assuming the sizes are the same, the output current will then match the input current. If the sizes are different then the output current is scaled by:

$$I_{OUT} = \left(\frac{W}{L}\right)_{OUT} \cdot \left(\frac{L}{W}\right)_{IN} \tag{14}$$

To have good matching performance usually $L_{IN} = L_{OUT}$ and $\frac{W_{OUT}}{W_{IN}}$ is a rational number so that unit FETs can be used.

(b) Selecting Sizes

How do we select the value of $\frac{W}{L}$? As we discussed previously the output is a current so to get the best performance for thermal noise and offset we need to use a low g_m. This means we need a low transconductance efficiency where the channel is heavily inverted and the overdrive voltage is high.
To achieve this, generally we want a low value of $\frac{W}{L}$. Although the absolute value depends on the device used, PMOS devices have a lower charge mobility than NMOS so will require a higher $\frac{W}{L}$ ratio. Aim for a g_m/I_d of 5-7 or a $V_{DS,sat}$ of 300 - 350 mV.

5 The Differential Pair

The differential pair is shown below. It is most commonly seen at the input of op-amp circuits but is also seen in many other places.
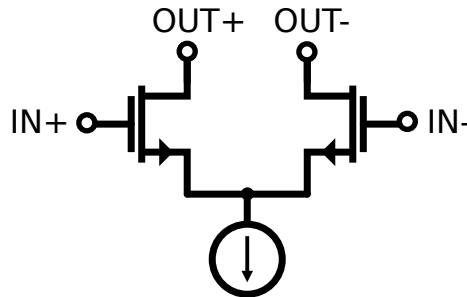
(a) Circuit Operation

The differential pair compares two voltages and splits the bias current depending on the difference between the input voltages.

If the two input voltages are equal then V_{GS} is equal for both devices and both devices get half of the bias voltage. If V_{IN+} is higher than V_{IN-} then more current flows into V_{OUT+} and less into V_{OUT-}, but the sum still remains the same bias current.

(b) Selecting Sizes

As already discussed in the section on noise and offset the differential pair devices should operate with a high g_m and therefore a high transconductance efficiency. Therefore the ratio of $\frac{W}{L}$ should be high. Aim for a g_m/I_d of 20-25 or a $V_{DS,sat}$ of 10 - 50 mV.

6 Useful Circuits

(a) Transmission Gate

A building block switch made of one or more FETs. The control signals are digital and the terminals A and B are analogue.
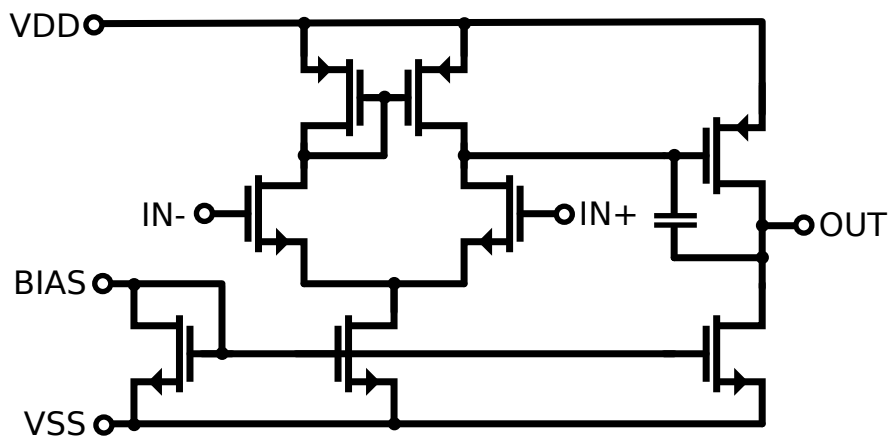
CTL+

A   B

CTL-
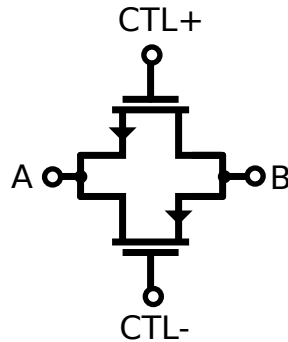
Important factors:

- On resistance of switch

- Charge injection

(b) 5T Op-Amp

A simple two stage op-amp circuit with differential inputs and current output. Stability can be improved with a Miller capacitor across the output stage.

VDD

IN-   IN+   OUT

BIAS

VSS

Important factors:

- Input/Output Voltage Ranges

- Gain

- Bandwidth

- Stability

- Noise

- Slew Rate

7 NGSpice Notes

(a) Saving Operating Parameters

To save the operating parameters in NGSpice outputs the following syntax needs to be used:

```
.save all @M.x1.XMcas_p.msky130_fd_pr__pfet_01v8[vdsat]
```

The addition of all is to prevent NGSpice *only* saving operating parameter and none of the voltages. Note that the string starts with an M for MOSFET then the dot delimited path to the transistor model. The exact transistor model needs to be used. Finally the operating parameter can be specified in square brackets. This is reqiured for every device and paramter you want to investigate.
Some common parameters:

```
gm vdsat vds id
```