Decimator in PSoC®

AN51352

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Associated Project: No
Associated Part Family: CY8C24x94, CY8C27x43, CY8C29x66, CY8C23x33, CY8C24x23A
Software Version: None
Associated Application Notes: AN2010, AN2041, AN2239

Application Note Abstract

This application note describes the decimator, which is a hardware block used in Delta-Sigma and incremental ADCs in PSoC®. It discusses density signals, decimation functions, and Sinc filters, and how they are related to the decimator in PSoC.

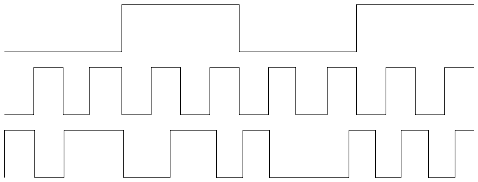
Introduction

The decimator is an important hardware function in the implementation of Delta-Sigma and incremental Analog-to-Digital Convertors (ADCs) in PSoC. A decimator is a digital Finite Impulse Response (FIR) filter that converts a density stream into parallel digital data. The decimator is chosen over other external FIR filters in PSoC because of its simplicity in implementation and cost effectiveness in silicon area. This application note assumes that you are familiar with user modules (UM) in PSoC. If you are new to PSoC, refer the application note AN2010, *Getting Started with PSoC.*

Density Domain

Density is the percentage of '1's in the digital signal stream of '1's and '0's. The percentage in the signal that is high is important and not the particular waveform. From the density perspective, all the signals shown in Figure 1 are equivalent.

Figure 1. 50% Density Waveforms



The density signal is a digital signal interpreted in density domain. The benefits of signal processing in the density domain are:

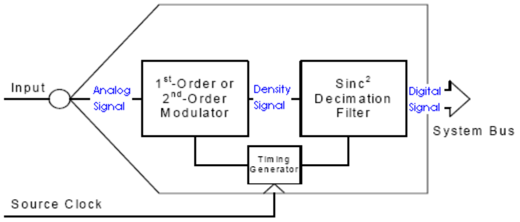
- Simple logic gates
- Higher immunity to noise
- Better resolution at lesser logic blocks, unlike digital signal processing

Density Signal in PSoC

A modulator converts either an analog or a digital value to a density signal. In this application note, the focus is on the analog modulators, because decimators are used in the ADCs in PSoC.

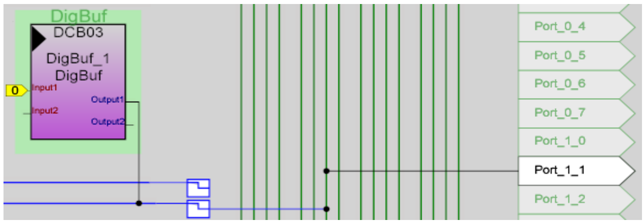
An example of an analog modulator is a Delta Sigma Modulator (DSM). The DSM is a combined integrator and comparator formed with a switched capacitor block. A DSM is a part of the DelSig ADC UM, where the analog signal is converted into a density signal by the modulator and fed into the decimator, as shown in Figure 2.

Figure 2. Block Diagram of DelSig ADC



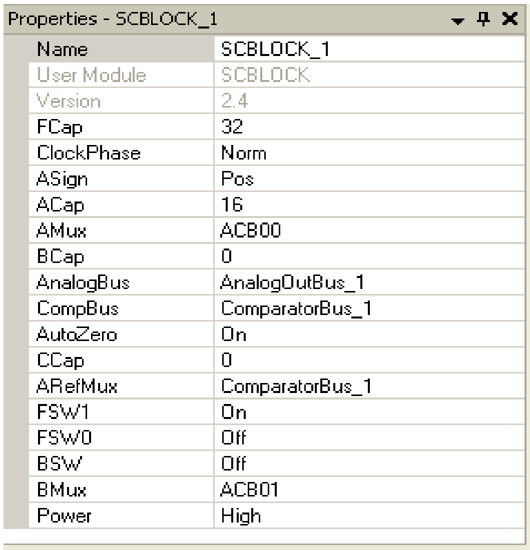
The density signal is observed in the ADCs by connecting the comparator bus output to a digital buffer (DigBuf) UM, and connecting it to an output port pin (Figure 3).

Figure 3. Routing the Comparator Bus to Output Port



A DSM is formed with the switched capacitor block (SCBlock) UM in PSoC with the parameter settings shown in Figure 4. The output density signal is observed by connecting to the output pin shown in Figure 3. Refer to AN2041 for more information about switched capacitor analog blocks.

Figure 4. SCBlock Settings that Implement a DSM

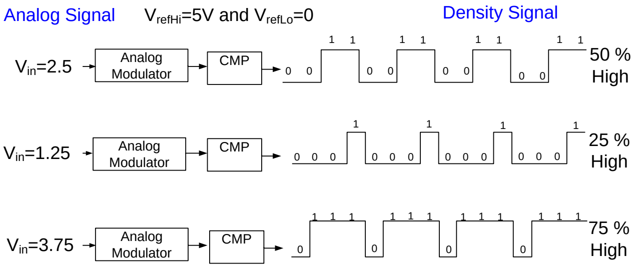


Properties - SCBLOCK_1

Name	SCBLOCK_1
User Module	SCBLOCK
Version	2.4
FCap	32
ClockPhase	Norm
ASign	Pos
ACap	16
AMux	ACB00
BCap	0
AnalogBus	AnalogOutBus_1
CompBus	ComparatorBus_1
AutoZero	On
CCap	0
ARefMux	ComparatorBus_1
FSW1	On
FSW0	Off
BSW	Off
BMux	ACB01
Power	High

Figure 5 shows an example of the density signal output from an analog modulator. The output signal for the reference from 0 to 5V is shown. It is not the shape of the waveform that matters in the density domain, but the percentage of '1's in the waveform.

Figure 5. Inputs and Outputs of Analog Modulator



The DSM is an oversampled converter. This implies that the output bit-stream of the modulator is at a higher rate than the required Nyquist frequency. Therefore, the quantization noise is lower in the bandwidth of interest and the noise increases rapidly beyond the bandwidth. Thus, we need a hardware function that accomplishes two goals:

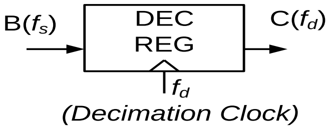
- Downsampling - To reduce the sample rate to the Nyquist rate
- Filtering - To eliminate the out of band noise

In the decimator, these functions are performed with decimation and a Sinc^2 filter. This is described in the following sections.

Decimation

Decimation is a function that downsamples the input signal. It has the benefits of higher signal to noise ratio and lower power consumption. It is an averaging function that accumulates N bits and averages them to give an output value. Decimation for digital signals is similar to sampling for analog signals. The most economical method of implementation of a decimation function is to pick one sample out of K samples. This is the method used in PSoC, by use of a hold register and clocking it at the decimation frequency. Considering an input signal B with frequency f_s, the output of the decimation register is a signal C, with frequency f_d, as shown in Figure 6.

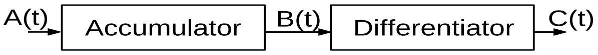
Figure 6. Decimation Function with Hold Register



Sinc Filter

A Sinc filter is a low pass digital filter that attenuates the quantization, interference, and anti-aliasing noise. The Sinc filter gets its name from the frequency response of the filter that is of the form sin(ω)/(ω). Filtering in the density domain does not need any digital multipliers. It can be implemented easily by cascading accumulators and differentiators. The block diagram for the Sinc filter is shown in Figure 7 and a description of each block follows.

Figure 7. Block Diagram for Decimator Sinc Filter



Accumulation

The accumulator is implemented using adders and delay blocks. For an input signal A(n) and accumulated signal B(n), accumulation in time domain is represented by Equation 1.

$$B(n) = B(n-1) + A(n) \qquad \text{Equation 1}$$

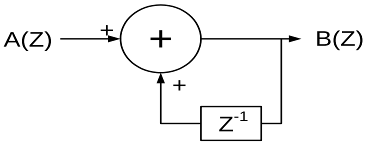
In Z domain it translates to:

$$B(z) = B(z)z^{-1} + A(z) \qquad \text{Equation 2}$$

$$H(z) = \left[\frac{1}{1-z^{-1}}\right] \qquad \text{Equation 3}$$

The Z domain representation for the transfer function obtained in Equation 3 is given in Figure 8.

Figure 8. Transfer Function for Accumulator



Differentiation

The differentiator is implemented using subtraction and delay blocks. In time domain, when the delay is K, differentiation is represented by Equation 4.

$$D(n) = C(n) - C(n-K) \qquad \text{Equation 4}$$

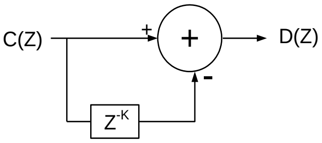
In Z domain it translates to

$$D(z) = C(z) - C(z)z^{-K} \qquad \text{Equation 5}$$

$$H(z) = 1 - z^{-K} \qquad \text{Equation 6}$$

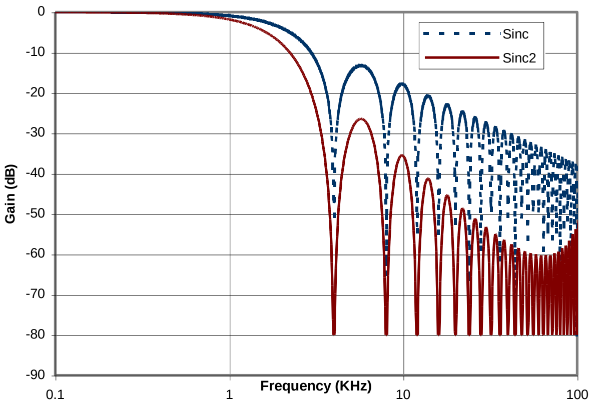
The Z domain representation for the transfer function obtained in Equation 6 is given in Figure 9.

Figure 9. Transfer Function for Differentiator



When the Sinc function is applied twice, we get a Sinc^2 filter that has lower cut off frequency and better noise elimination. The graph of a Sinc function and a Sinc^2 function for f_s=125 kHz is shown in Figure 10. The Sinc^2 response is for a decimation rate of K=32. The equation used to plot the Sinc^2 function is described in detail in the next section. The graph in Figure 10 explains why a Sinc^2 filter is chosen for PSoC, with more clarity.

Figure 10. Comparison of Sinc vs Sinc^2 Function

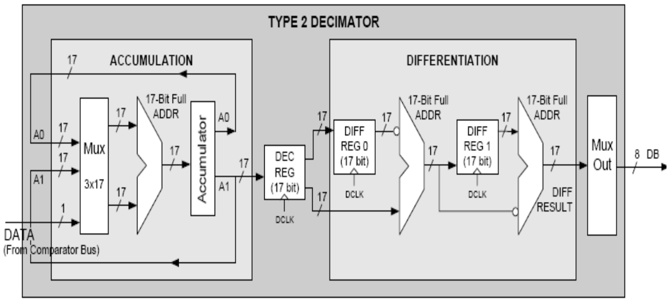


Decimator in PSoC

As mentioned earlier, the decimator is a digital filter that has the Sigma (accumulation) – Delta (differentiation) functionality. The decimator in PSoC has the Sinc^2 filter and decimation function incorporated in it, to form a Sinc^2 decimation filter. The decimation rate is also the rate at which differentiation is performed. A Sinc^2 filter is obtained by applying the Sinc function twice—by cascading two accumulators and two differentiators.

The complete block diagram of the decimator, formed with the blocks discussed in the previous section and a decimation rate of K is shown in Figure 11. This is the block diagram of a Type 2 decimator in PSoC, which has the complete decimation operation in hardware. There are other forms of decimators in PSoC and their differences from this base module are given in a later section.

Figure 11. Block Diagram for Decimator showing Accumulation, Decimation, and Differentiation



Considering the accumulator and differentiator equations (Equation 3 and Equation 6), and the decimation function, the normalized transfer function of the decimator for a Sinc^2 decimation filter is given by Equation 7.

$$H(z) = \left[\frac{1}{K}\,\frac{1-z^{-K}}{1-z^{-1}}\right]^2 \qquad \text{Equation 7}$$

The frequency response of this normalized transfer function is given in Equation 8. It is this equation that is plotted in Figure 10 and compared with the Sinc function that has the sin(ω)/(ω) format.

$$H(e^{j\omega}) = \left(\frac{1}{K}\,\frac{\sin\left(\frac{\pi f K}{f_s}\right)}{\sin\left(\frac{\pi f}{f_s}\right)}\right)^2 \qquad \text{Equation 8}$$

In the case of a DelSig UM, the accumulation is performed at the same frequency as the modulation (Equation 9). In one DataClk cycle, both the accumulations are completed, the first accumulation during ϕ1 and the second during ϕ2.

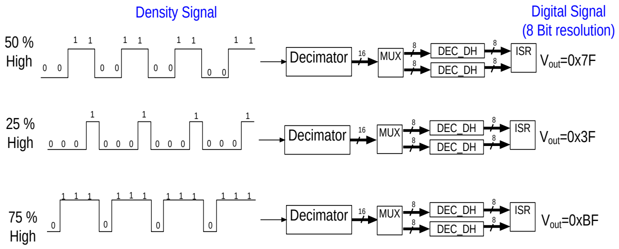
$$f_s = \frac{DataClk}{4} \quad \text{(Same as } \phi_1 \text{ and } \phi_2\text{)} \qquad \text{Equation 9}$$

The differentiators operate at a lower frequency, depending on the decimation rate. If the decimation rate is K, then the decimation register and differentiators are clocked at frequency f_d given by Equation 10.

$$f_d = \frac{DataClk}{4 * K} \qquad \text{Equation 10}$$

The output of the decimator is N bit data that comes out at frequency f_d. The output of the decimator is shown in Figure 12. To avoid overflow during internal calculations, the internal registers and the bus lines have a higher number of bits than the maximum resolution. The data is shifted based on the resolution bits parameter and the output is stored in registers DEC_DH and DEC_DL in PSoC. The data value is later processed in the interrupt service routine (ISR). The data processing can be a function such as conversion from unsigned to signed, because the hardware treats the data as unsigned.

Figure 12. Inputs and Outputs of Decimator



Types of Decimators in PSoC

In PSoC, there are both Type 1 and Type 2 decimators.

Type 1 Decimator Block

The Type 1 decimator has the accumulation performed in the hardware and requires the differentiation in firmware. Also, the density signal is represented as '1's and '-1's instead of '1's and '0's. In other words, when the input is a '0', 1 is subtracted from the accumulated value. The PSoC device families that have a Type 1 decimator block are:

- CY8C27x43
- CY8C24x23A

Type 2 or Super Decimator Block

The Type 2 decimator has a full version of the Sinc^2 filter. Both the accumulation and decimation are performed in hardware and thus it is much faster and uses less memory.

- CY8C29x66: Uses an external digital block timer
- CY8C24x94: Can choose either external digital block or an internal timer

The decimator in the Delta Sigma ADC is a low pass filter. It is more complex than a counter, which is the most basic form of filter. The decimator block is also used in the Incremental ADC (ADCINC) UM as a digital counter block, and thus saves a digital block. In this mode, the decimator block is used in place of a counter to count the number of times the output is high. Other incremental ADCs such as ADCINC14, ADCINC12, and ADCINCVR have the same sample rate as ADCINC but they use a digital block for the counter. The decimator is used in both ADCINC and DELSIG ADC modules, but in different configurations, that results in differences between the two. For detailed information on the differences in ADCs refer application note AN2239, *ADC Selection*.

Summary

The decimator is a low pass digital filter. It converts a density bit stream into parallel digital data and reduces the noise on the input signal. The decimator is more efficient than a counter, which is the simplest of the low pass digital filters. In PSoC, the Delta Sigma ADCs use the decimator as a low pass Sinc^2 decimation filter. The incremental ADCs use the decimator in place of a counter, because it saves a digital block. Using decimators for filtering makes the signal processing in PSoC easier to implement, and less expensive in terms of silicon area.

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Document History

Document Title: Decimator in PSoC®

Document Number: 001-51352

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2678596	YARA	03/25/09	New application note

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