## 13.3.5 DxBxxFN

### Digital Basic/Communications Type B Block Function Register

**Individual Register Names and Addresses:**

| | | | |
|---|---|---|---|
| DBB00FN : 1,20h | DBB01FN : 1,24h | DCB02FN : 1,28h | DCB03FN : 1,2Ch |
| DBB10FN : 1,30h | DBB11FN : 1,34h | DCB12FN : 1,38h | DCB13FN : 1,3Ch |
| DBB20FN : 1,40h | DBB21FN : 1,44h | DCB22FN : 1,48h | DCB23FN : 1,4Ch |
| DBB30FN : 1,50h | DBB31FN : 1,54h | DCB32FN : 1,58h | DCB33FN : 1,5Ch |

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| **Access : POR** | RW : 0 | RW : 0 | RW : 0 | RW : 0 | | RW : 0 | | |
| **Bit Name** | Data Invert | BCEN | End Single | Mode[1:0] | | Function[2:0] | | |

This register contains the primary Mode and Function bits that determine the function of the block.

Before changing any of the configuration registers (DxBxxFN, DxBxxIN, and DxBxxOU), disable the corresponding digital block by setting bit 0 in the CR0 or DxBxxCR0 register to '0'. The values in the DxBxxFN register should not be changed while the block is enabled. After all configuration changes are made, enable the block by setting bit 0 in the DxBxxCR0 register to '1'.

The naming convention for this register is as follows. The first 'x' in the digital register's name represents either "B" for basic or "C" for communication. For rows of digital PSoC blocks and their registers, the second 'x' set represents <Prefix>mn<Suffix>, where m=row index, n=column index. Therefore, DCB12FN is a digital communication register for a digital PSoC block in row 1 column 2. Depending on the digital row characteristics of your PSoC device, some addresses may not be available. For additional information, refer to the "Register Definitions" on page 335 in the Digital Blocks chapter.

| Bit | Name | Description |
|---|---|---|
| **7** | **Data Invert** | 0 Data input is non-inverted.<br>1 Data input is inverted. |
| **6** | **BCEN** | Enable Primary Function Output to drive the broadcast net.<br>0 Disable<br>1 Enable |
| **5** | **End Single** | 0 Block is not the end of a chained function or the function is not chainable.<br>1 Block is the end of a chained function or a standalone block in a chainable function. |
| **4:3** | **Mode[1:0]** | These bits are function dependent and are described by function as follows. |
| | Timer or Counter: | Mode[0] signifies the interrupt type.<br>0 Interrupt on Terminal Count<br>1 Interrupt on Compare True<br>Mode[1] signifies the compare type.<br>0 Compare on Less Than or Equal<br>1 Compare on Less Than |
| | CRCPRS: | Mode[1:0] are encoded as the Compare Type.<br>00b Compare on Equal<br>01b Compare on Less Than or Equal<br>10b Reserved<br>11b Compare on Less Than |

*(continued on next page)*

## 13.3.5 DxBxxFN *(continued)*

| | | |
|---|---|---|
| **4:3** *(cont.)* | Dead Band: | Mode[1:0] are encoded as the Kill Type.<br>00b Synchronous Restart KILL mode<br>01b Disable KILL mode<br>10b Asynchronous KILL mode<br>11b Reserved |
| | UART: | Mode[0] signifies the Direction.<br>0 Receiver<br>1 Transmitter<br>Mode[1] signifies the Interrupt Type.<br>0 Interrupt on TX Reg Empty<br>1 Interrupt on TX Complete |
| | SPI: | Mode[0] signifies the Type.<br>0 Master<br>1 Slave<br>Mode[1] signifies the Interrupt Type.<br>0 Interrupt on TX Reg Empty<br>1 Interrupt on SPI Complete |
| **2:0** | **Function[2:0]** | 000b Timer (chainable)<br>001b Counter (chainable)<br>010b CRCPRS (chainable)<br>011b Reserved<br>100b Dead Band<br>101b UART (DCBxx blocks only)<br>110b SPI (DCBxx blocks only)<br>111b Reserved |