A technique for measuring the signal frequency using PSoC programmable digital blocks to obtain maximum precision is described in application note AN2283.

A Hybrid method described on page 3 will be used which measures the width of as many cycles that can fit in a specified sample period shown in figure 3 of application note. A timer will function as an n bit down counter that decrements each clock cycle fclk. A terminal count is generated when the counter underflows. This signal fsample defines the sample period. It is a function of the clock frequency and counter size. The CPU uses this signal to synchronize the first and the last cycle capture. The input finput is connected to the timer capture input. A rising edge on the capture cause the counter value to be latched and be accessible to the CPU. The input signal is connected to the CPU. This enables it to be counted. This method requires measuring the time of as many input cycles that fit within the sample period.

Table 5 summarizes the hybrid method of measuring the frequency. It shows that it works well over a wide range of frequencies and produces answers at a steady predictable rate.

The PCoC implementation will consist of a comparator which will condition the input signal and give an “acquire” interrupt. A 16 bit timer with an interrupt on terminal count