Propose a general method for binding operations to hardware circuits and variables to

registers. The goal is to find the minimum amount of hardware that guarantees satisfying a

predefined timing constraint on a ADFG (Acyclic Dataflow Graph). Illustrate your algorithm on

an ADFG with more than 10 nodes that represent operations on at least 5 variables.

1. Assuming each node represents an operation, identify number of different node operations present in the graph.
2. If we have multiple variables performing the same operation and there is no dependency identify the ways in which these operations can be parallelized otherwise pipelining such that scheduling meets timing constraints.
3. In general parallelism has to be avoided to minimise hardware implementation but the trade off is timing constraint which is more important.
4. If timing constraint is not met first considering using pipelining and if even then timing constraint is not met then implement parallelism by using extra hardware resource for an operation.
5. The above step will occur in a loop until the timing constraint is met.

Draw figure 4.15 and 4.16 from textbook modify according to the question.

Office Hour Hints:

You have a graph and each node in the graph is an operations

Operations it requires variables

Then there is a timing constraint

Arcs tell you the sequence of the nodes in 4.15 each of the nodes is an operation that involves variables

So now you're given timing constraint

You have to figure out what resources are needed to execute the graph such that the timing is met

Given graph but you know that his has to end within 7 so now you have to figure out how how many of each module you require. How many adders how many multiplier how many memory modules such that the execution ends in 7

1. Come up with schedule that ends within that time
2. Once you have the schedule identify the resources needed for that schedule
   1. For that schedule come up with resources you need

Scheduling is dependant on timing constraint.

For other problem build a schedule that meets timing constraint and then for that schedule you find hardware resources which give you that schedule.