Is it possible to develop a hardware-only PSoC-based implementation for differentiation, assuming you only have Type 1 decimator blocks.

Yes, you can use a timer to implement the delay and the PSoC M8C has subtract routines. So for the continuous operation of the decimator, the timer can be set to a certain delay and generate an interrupt at the end of the delay. In the interrupt service routine, the output register from the Type 1 decimator block (accumulator) and read in the routine. The ‘SUB’ instructions will be used to perform the necessary subtractions. This way the processor is off loaded.

WAHOOO!