Propose a general approach for scheduling the operations pertaining to parallel loop iterations.

Assume that there are no data dependencies between operations in different iterations. Consider

an example of 5 parallel iterations and explain the scheduling result of your algorithm

A general approach for scheduling the operations pertaining to parallel loop iterations, will be as follows, with the assumption that there are no data dependencies between operations in different iterations and there is sufficient available hardware on the architecture (3 memory modules). Relating an example of 5 parallel iterations to figure 4.16 on page 161 there will be an additional loop iteration. The new diagram will contain at least 3 CA modules that can compute the address of an array element in parallel and at least 3 MA modules that can access the data memory in memory. In other words the there should be more than enough resources to execute 5 of them in parallel. Lastly there will only need to be one multiplication element since all multiplies are done sequentially.

Draw diagram 4.16 (b) with 5th column