Bug-5 Report
Group-8

1. **Failing Test name –** Data cache write hit test by using MESI protocol

2. **Test description (Describe the planned scenario and the expected result)**
   Making a block into modified state by performing the write operation to specified address in core1 and then making it to shared state when a read operation is performed for the same address but in the second core. This address in second core writes the new value and makes the state to modified and changes state to Invalid in the core1.
   Now second Core performs read operation to check if the new value got updated into the address and changes core1 status to shared from Invalid by performing read operation.

3. **Failing assertion that helped you identify the bug**

4. **Debugging:** Verified outputs from the waveform by simulating the test and by following processor write hit steps from HAS document.
   As per has document write operation is completed when the cpu_wr_done was raised high but in the above waveform it's not being asserted. Along with this all_invalidation_done is not being asserted even though the invalidate was being asserted because invalidation_done is giving high impedance.
   After comparing the design code with HAS document we concluded that invalidation_done is initialized with Z (high impedance)

5. **Erroneous RTL file name –** main_func_lv1_dl.sv

6. **Lines of RTL file responsible for the bug**
   Line no 138. Invalidation_done <=1'bz;

7. **Corrected RTL code**
   Line no 138. Invalidation_done <=1'b0;

8. **Corrected Wave form**