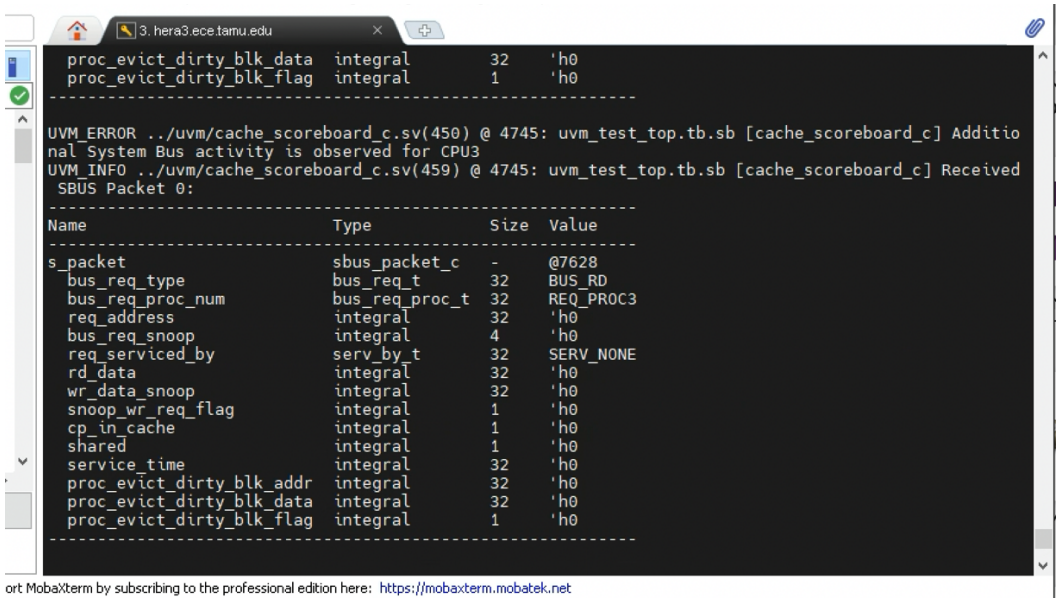
# Group-8
# Bug-1 Report

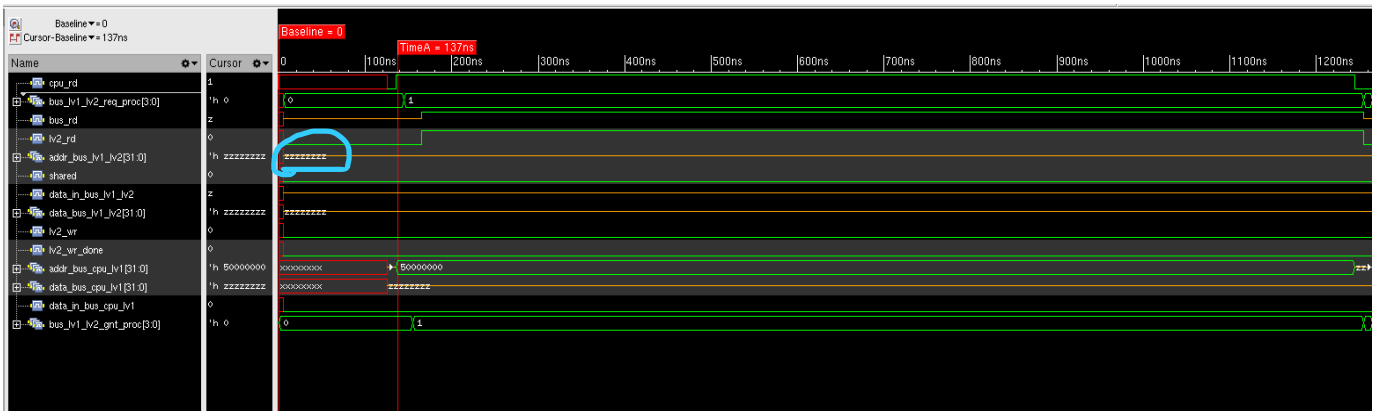
1. **Failing Test name** – Read miss test in Data cache

2. **Test description (Describe the planned scenario and the expected result) –** Performed read operation on data cache and verified whether we are getting data from level- 2 cache or not

3. **Debugging:**
   Error message:




4. **Failing assertion that helped you identify the bug -** Verified outputs from the waveform by simulating the test (read_miss_dcache.sv) and by following processor read miss steps from HAS document.




Waveform was observed, and it was found that addr_bus_lv1_lv2 has high impedance with no assigned value. So, the design files were checked for address bus assignments.

5. **Erroneous RTL file name** - main_func_lv1_dl.sv
6. **Lines of RTL file responsible for the bug (mention the line numbers and lines of the bug)**
   Line no – 104, assign addr_bus_lv1_lv2 = data_bus_lv1_lv2_reg;
7. **Corrected RTL code (only mention the corrections)-** Line no - 104. assign addr_bus_lv1_lv2 = addr_bus_lv1_lv2_reg;