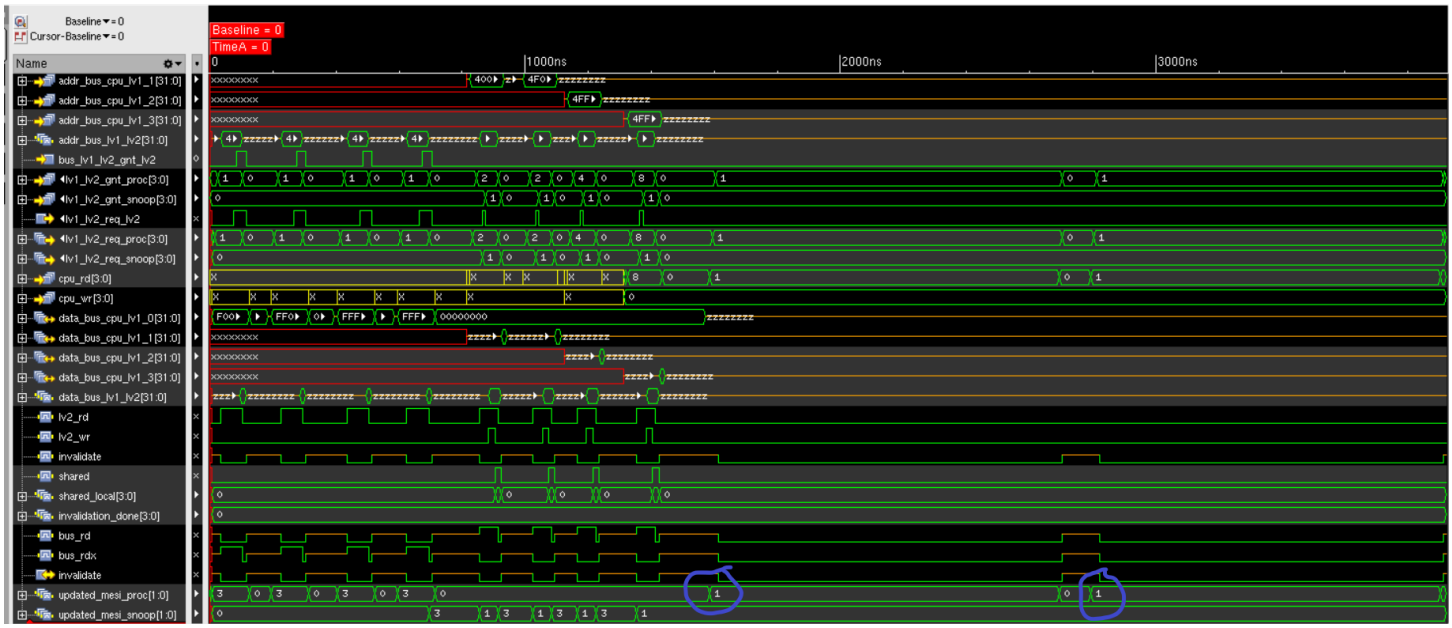
Bug-7 Report

Group-8

1. **Failing Test name –** Data cache read miss test with no free block by using MESI protocol

2. **Test description (Describe the planned scenario and the expected result)**
   Making all the blocks into modified state by performing the write operation to specified addresses in core1 and then making it to shared state when a read operation is performed for the same addresses but from different processors. Then read operation is performed on core1 for a different address which was not used at the beginning for write. This makes the MESI state for the block with previous address to 'I'. The block will be replaced with new address, it should have MESI state set to 'E'.

3. **Failing assertion that helped you identify the bug**



4. **Debugging:** Verified outputs from the waveform by simulating the test and by following processor read miss with block replacement steps from HAS document.
   As per HAS document for read miss with block replacement operation, when the MESI state is in 'S' or 'E' then we should make MESI state to 'I' and then write miss free block available steps are followed. As we are performing read on the core1 with different address, MESI state changes to 'E'(which is 2 but it is showing 1 in waveform which is 'S').
5. **Erroneous RTL file name –** main_func_lv1_dl.sv
6. **Lines of RTL file responsible for the bug**
   Line 185: `CACHE_CURRENT_MESI_PROC<=SHARED
7. **Corrected RTL code**
   Line no 185. `CACHE_CURRENT_MESI_PROC<=INVALID

8. Corrected Wave form