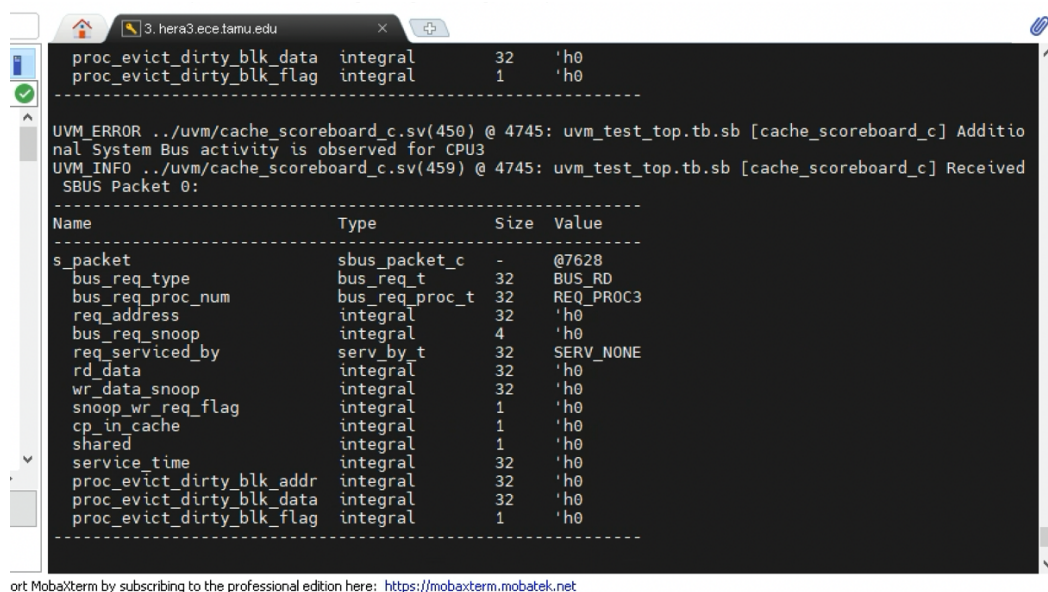


Group-8

Bug-1 Report

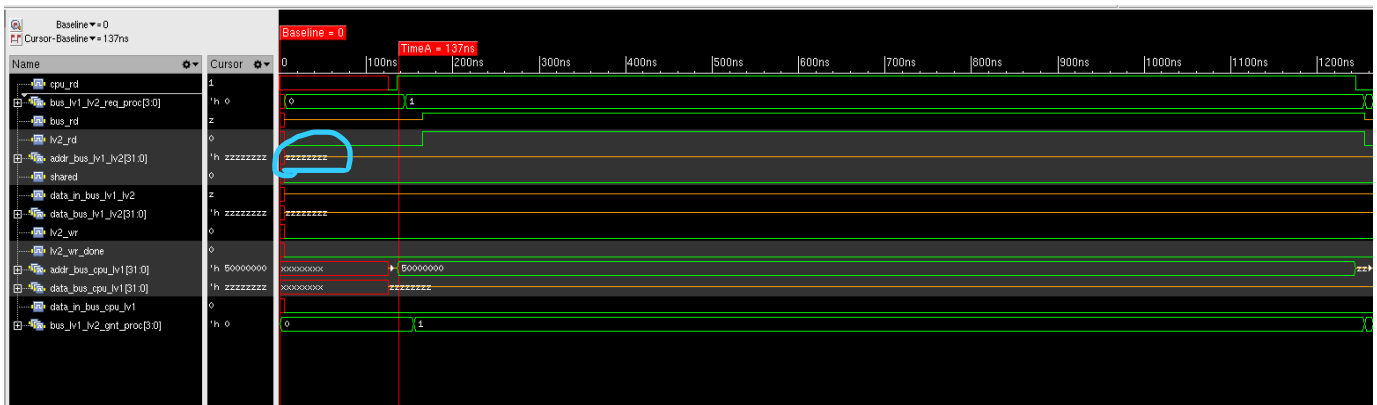
1. **Failing Test name** – Read miss test in Data cache
2. **Test description (Describe the planned scenario and the expected result)** – Performed read operation on data cache and verified whether we are getting data from level- 2 cache or not
3. **Debugging:**

Error message:



```
proc_evict_dirty_blk_data integral 32 'h0
proc_evict_dirty_blk_flag integral 1 'h0
-----
UVM_ERROR ../uvm/cache_scoreboard_c.sv(459) @ 4745: uvm_test_top.tb.sb [cache_scoreboard_c] Additional System Bus activity is observed for CPU3
UVM_INFO ../uvm/cache_scoreboard_c.sv(459) @ 4745: uvm_test_top.tb.sb [cache_scoreboard_c] Received SBUS Packet 0:
-----
Name                               Type             Size  Value
-----
s_packet                           sbus_packet_c    -      @7628
bus_req_type                       bus_req_t        32     BUS_RD
bus_req_proc_num                   bus_req_proc_t   32     REQ_PROC3
req_address                        integral         32     'h0
bus_req_snoop                      integral         4       'h0
req_served_by                      serv_by_t        32     SERV_NONE
rd_data                           integral         32     'h0
wr_data_snoop                     integral         32     'h0
snoop_wr_req_flag                 integral         1       'h0
cp_in_cache                       integral         1       'h0
shared                           integral         1       'h0
service_time                      integral         32     'h0
proc_evict_dirty_blk_addr          integral         32     'h0
proc_evict_dirty_blk_data          integral         32     'h0
proc_evict_dirty_blk_flag          integral         1       'h0
-----
```

4. **Failing assertion that helped you identify the bug** - Verified outputs from the waveform by simulating the test (read_miss_dcachc.sv) and by following processor read miss steps from HAS document.



Waveform was observed, and it was found that addr_bus_lv1_lv2 has high impedance with no assigned value. So, the design files were checked for address bus assignments.

5. **Erroneous RTL file name** - main_func_lv1_dl.sv
6. **Lines of RTL file responsible for the bug (mention the line numbers and lines of the bug)**
Line no – 104, assign addr_bus_lv1_lv2 = data_bus_lv1_lv2_reg;
7. **Corrected RTL code (only mention the corrections)**- Line no - 104. assign addr_bus_lv1_lv2 = addr_bus_lv1_lv2_reg;