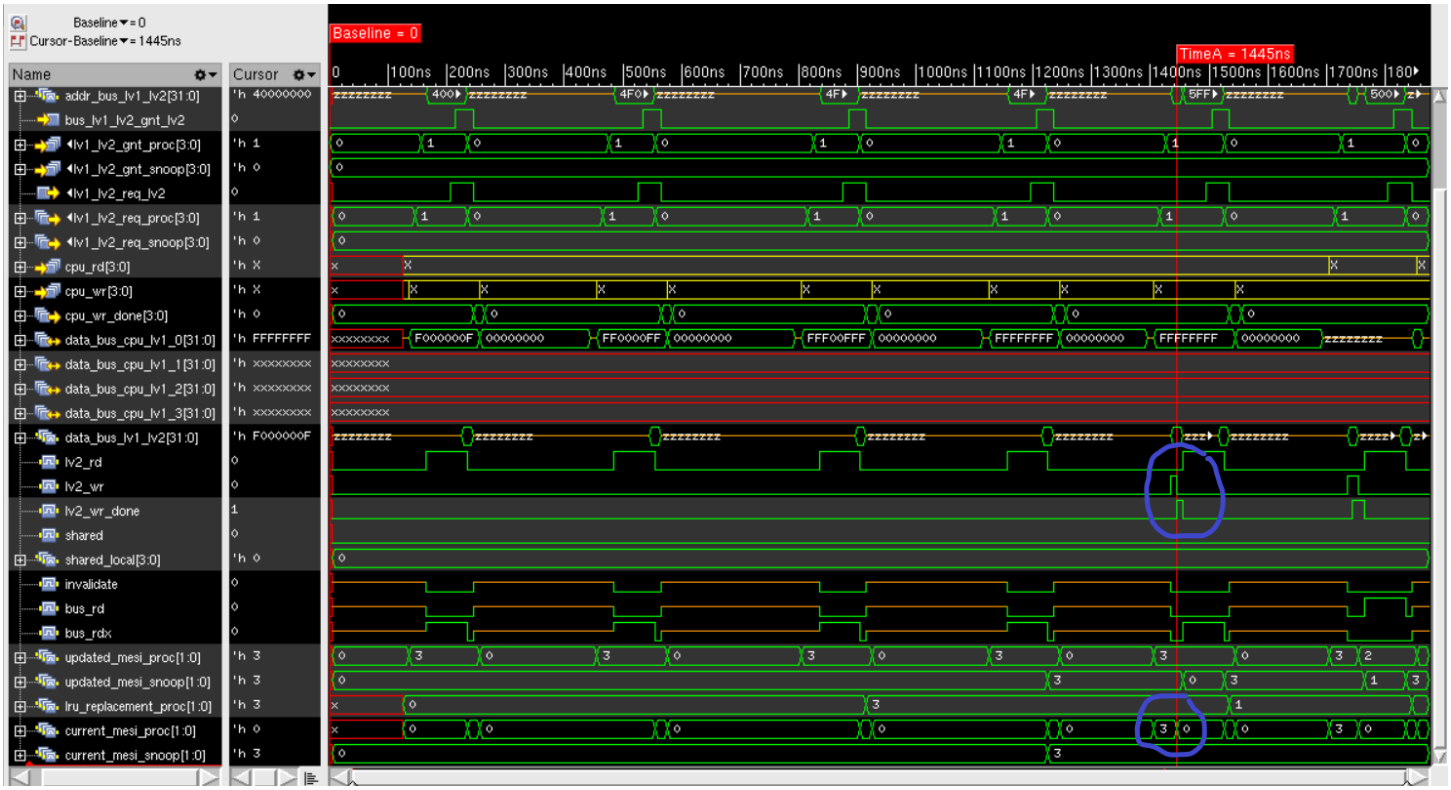
# Bug-8 Report

# Group-8

1. **Failing Test name –** Data cache write miss test with no free block by using MESI protocol

2. **Test description (Describe the planned scenario and the expected result)**
   Making all the blocks into modified state by performing the write operation to specified addresses in core1. Then write operation is performed on core1 again with a different address which was not used at the beginning for write. The modified data which was present in the old address should be written to level 2, once this done the MESI state of block with old address is set to ‘I’. The block will be replaced with new address, it should have MESI state set to ‘M’.

3. **Failing assertion that helped you identify the bug**




4. **Debugging:** Verified outputs from the waveform by simulating the test and by following processor write miss with block replacement steps from HAS document.
   As per HAS document for write miss with block replacement operation, when the MESI state is in ‘M’ for the block to be replaced then we should make bus_lv1_lv2_gnt_proc high and address of replacement block is loaded into addr_bus_lv1_lv2. Dirty data is loaded into data_bus_lv1_lv2 then lv2_wr is made high to update the value in lv2. Once lv2_wr_done is made high then MESI state of block to be replaced is set to ‘I’. Later, steps similar to write miss operation with free block available.
   In the above waveform the current_mesi_proc[1:0] is changed to 0 (which is ‘I’) even though lv2_wr_done was not asserted.
5. **Erroneous RTL file name –** main_func_lv1_dl.sv
6. **Lines of RTL file responsible for the bug** Line 281: if (lv2_wr) begin

7. **Corrected RTL code** Line 281: if (lv2_wr_done) begin
8. **Corrected Wave form**