Bug-4 Report
Group-8

1. **Failing Test name –** read miss dcache on CPU1
2. **Test description (Describe the planned scenario and the expected result)**
   Performed read operation on data cache for CPU1 and verified whether we are getting data from level- 2 cache or not
3. **Debbuging:**
   Error message:

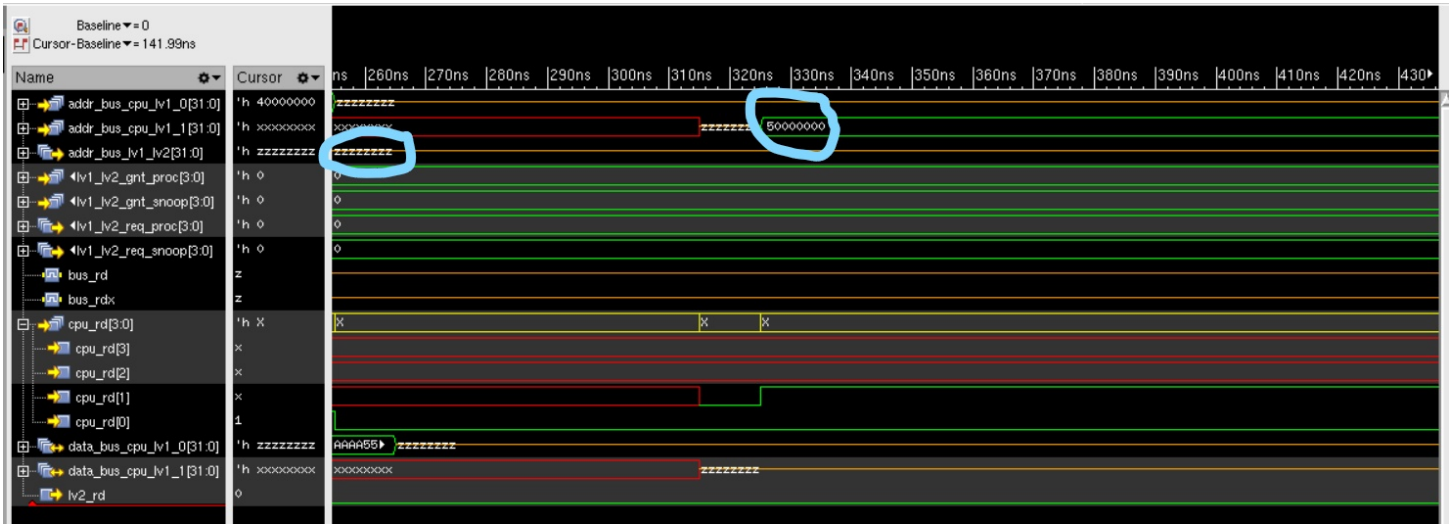
```
                                                .addr_bus_lv1_lv2(addr_bus_lv1_lv2),
                                                                  |
xmelab: *W,CUVMPW (../design/lv1/cache_lv1_multicore.sv,165|81): port sizes differ in port connection (32/15).
                                                .addr_bus_cpu_lv1(addr_bus_cpu_lv1_1),
                                                                  |
xmelab: *W,CUVMPW (../design/lv1/cache_lv1_multicore.sv,167|83): port sizes differ in port connection (32/15).
```

This above messaged was observed while compiling, this gave the idea to run the read miss dcache on CPU1.

4. **Failing assertion that helped you identify the bug**
   Even though addr_bus_cpu_lv1_1[31:0] shows address 32'h50000000, it is not reflected in addr_bus_lv1_lv2[31:0] due to which lv2_rd is not asserted. This can be observed in the waveform.

```
UVM_INFO ../uvm/cpu_driver_c.sv(83) @ 275: uvm_test_top.tb.cpu[0].driver [cpu_driver_c] Ended Driving transaction
UVM_INFO ../uvm/cpu_driver_c.sv(66) @ 275: uvm_test_top.tb.cpu[1].driver [cpu_driver_c] Input Data to Send:
-----------------------------------------------------------------------------------------------
Name                          Type              Size  Value
-----------------------------------------------------------------------------------------------
trans                         cpu_transaction_c -     @7659
  data                        integral          32    'haaaa5555
  address                     integral          32    'h50000000
  request_type                request_t         1     READ_REQ
  access_cache_type           access_cache_t    1     DCACHE_ACC
  begin_time                  time              64    275
  depth                       int               32    'd2
  parent sequence (name)      string            20    read_miss_dcache_seq
  parent sequence (full name) string            47    uvm_test_top.tb.vsequencer.read_miss_dcache_seq
  sequencer                   string            32    uvm_test_top.tb.cpu[1].sequencer
-----------------------------------------------------------------------------------------------

UVM_INFO ../uvm/cpu_monitor_c.sv(55) @ 325: uvm_test_top.tb.cpu[1].monitor [cpu_monitor_c] Packet creation triggered
UVM_INFO ../uvm/cpu_monitor_c.sv(67) @ 325: uvm_test_top.tb.cpu[1].monitor [cpu_monitor_c] Dcache Packet creation triggered
UVM_INFO ../uvm/cpu_driver_c.sv(83) @ 1455: uvm_test_top.tb.cpu[1].driver [cpu_driver_c] Ended Driving transaction
UVM_INFO ../uvm/virtual_seqs.sv(38) @ 1455: uvm_test_top.tb.vsequencer@@read_miss_dcache_seq [read_miss_dcache_seq] drop_objection
UVM_INFO /opt/coe/cadence/XCELIUM/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 1455: reporter [TEST_DONE] 'run' phase is ready t
o proceed to the 'extract' phase
```



5. **Erroneous RTL file name:** cache_lv1_multicore.sv

6. **Lines of RTL file responsible for the bug (mention the line numbers and lines of the bug):** Line 140 - .ADDR_WID(INDEX_MSB)
7. **Corrected RTL code (only mention the corrections)-**
   Line no – 140 - .ADDR_WID(ADDR_WID)
8. **Corrected Waveform (Waveform after bug fix) :**

log file:

```
UVM_INFO ../uvm/cpu_monitor_c.sv(84) @ 445: uvm_test_top.tb.cpu[1].monitor [cpu_monitor_c] Write cache packet
UVM_INFO ../uvm/cache_scoreboard_c.sv(523) @ 445: uvm_test_top.tb.sb [cache_scoreboard_c] cpu_mon_packet from CPU1:
----------------------------------------------------
Name            Type              Size  Value
----------------------------------------------------
packet          cpu_mon_packet_c  -     @7713
  dat           integral          32    'haaaa5555
  address       integral          32    'h50000000
  num_cycles    integral          32    'h1
  illegal       integral          1     'h0
  request_type  request_t         1     READ_REQ
  addr_type     addr_t            32    DCACHE
----------------------------------------------------

UVM_INFO ../uvm/cache_scoreboard_c.sv(293) @ 445: uvm_test_top.tb.sb [cache_scoreboard_c] CHECK_DATA CPU1
UVM_INFO ../uvm/cache_scoreboard_c.sv(295) @ 445: uvm_test_top.tb.sb [cache_scoreboard_c] Data match!!! expected = aaaa5555 received =
5555
UVM_INFO ../uvm/cache_scoreboard_c.sv(430) @ 445: uvm_test_top.tb.sb [cache_scoreboard_c] System bus activity matched for this request
UVM_INFO ../uvm/cache_scoreboard_c.sv(431) @ 445: uvm_test_top.tb.sb [cache_scoreboard_c] Expected & Received SBUS Packet
------------------------------------------------------------
Name                        Type           Size  Value
------------------------------------------------------------
s_packet                    sbus_packet_c  -     @7748
  bus_req_type              bus_req_t      32    BUS_RD
  bus_req_proc_num          bus_req_proc_t 32    REQ_PROC1
  req_address               integral       32    'h50000000
  bus_req_snoop             integral       4     'h0
  req_serviced_by           serv_by_t      32    SERV_L2
  rd_data                   integral       32    'haaaa5555
  wr_data_snoop             integral       32    'h0
  snoop_wr_req_flag         integral       1     'h0
  cp_in_cache               integral       1     'h0
  shared                    integral       1     'h0
  service_time              integral       32    'h0
  proc_evict_dirty_blk_addr integral       32    'h0
  proc_evict_dirty_blk_data integral       32    'h0
  proc_evict_dirty_blk_flag integral       1     'h0
------------------------------------------------------------

UVM_INFO ../uvm/cpu_driver_c.sv(83) @ 465: uvm_test_top.tb.cpu[1].driver [cpu_driver_c] Ended Driving transaction
```