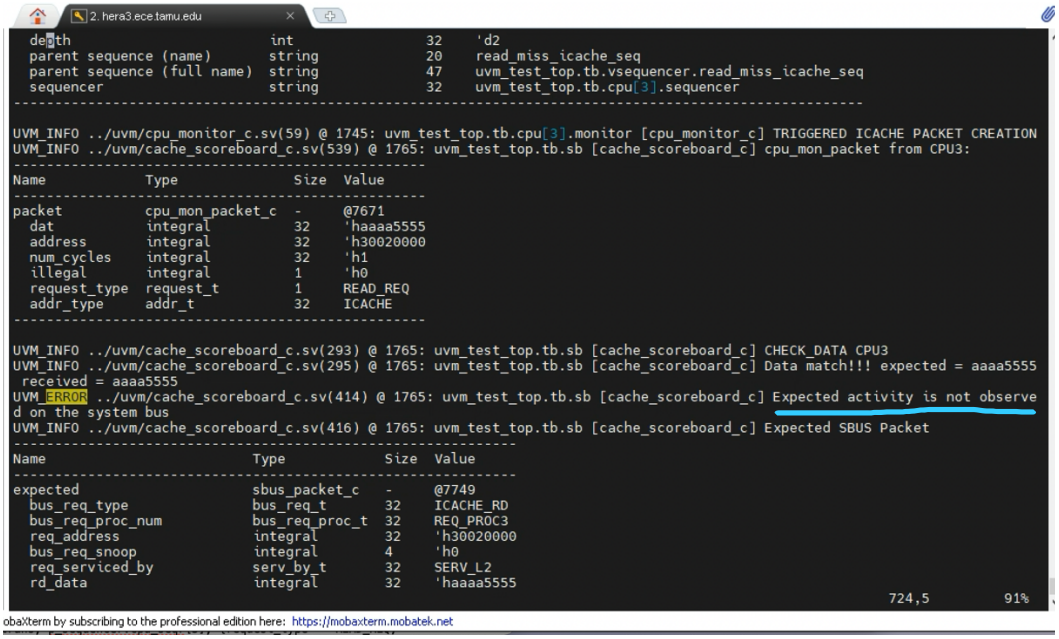
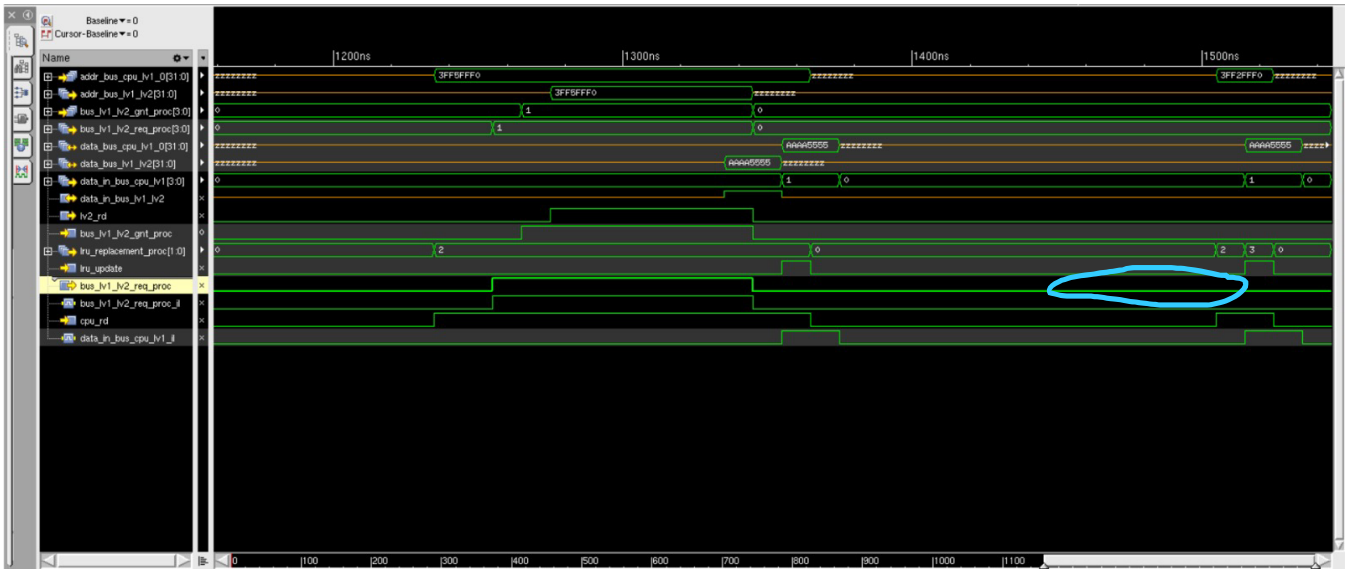
Group 8
Bug report - 6

1. **Failing Test name** – Instruction cache Read Miss test with no free block available and replacement needed
2. **Test description (Describe the planned scenario and the expected result)**
   Performed a read_miss_icache test on L1 and L2 cache by giving the read requests to both the caches. Here L1 Instruction cache read miss with no free block is available and it requires the LRU Replacement. Our test targets that L2 cache should through a read miss for the read request but from the log file and waveforms we observed that L1 cache is serviced instead of L2 cache.
3. **Failing assertion that helped you identify the bug**
   Scoreboard does not receive packets from system bus and throws error.
   Error message:



4. **Debug Process -** Verified outputs from the waveform by simulating the test (read_miss_icache.sv) and observed that Block serviced by LV1 instead of LV2 which means that block should have been replaced but was not replaced. Bus_lv1_lv2_req_proc did not assert high



5. **Erroneous RTL file name –** lru_block_lv1.sv
6. **Lines of RTL file responsible for the bug (mention the line numbers and lines of the bug)**

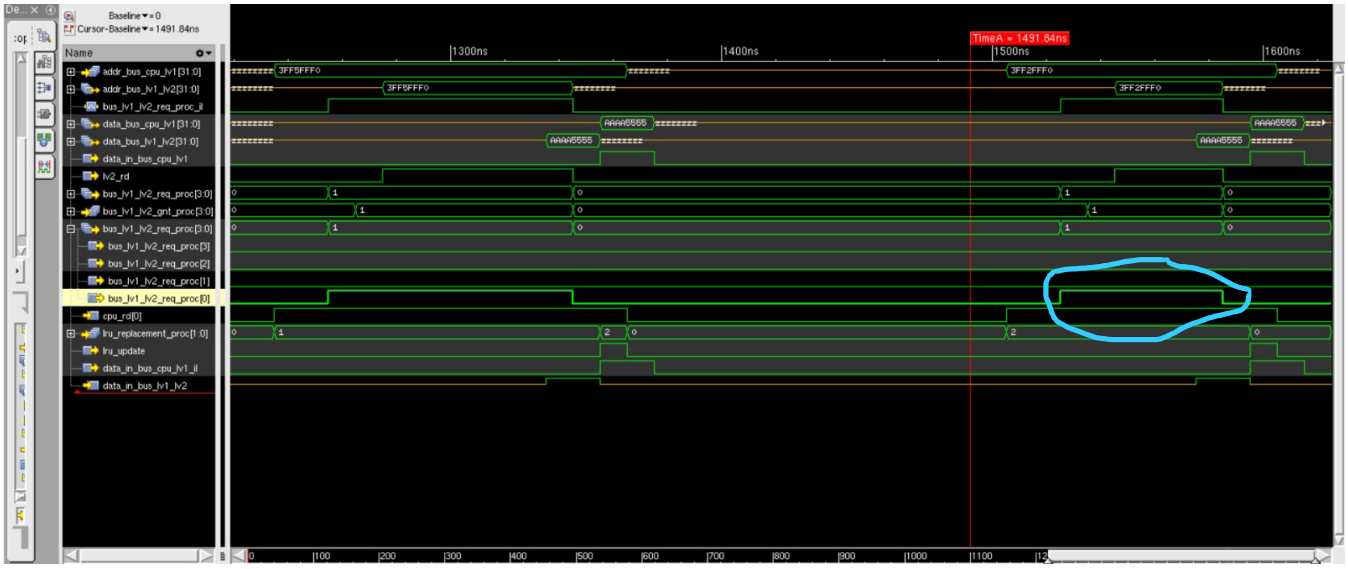
   Line no 38. BLK1_REPLACEMENT: lru_replacement_proc = 2'b10;

   Line no 39. BLK2_REPLACEMENT: lru_replacement_proc = 2'b01;
7. **Corrected RTL code (only mention the corrections)**

   Line no 38. BLK1_REPLACEMENT: lru_replacement_proc = 2'b01;

   Line no 39. BLK2_REPLACEMENT: lru_replacement_proc = 2'b10;

8. **Corrected Waveform**



Read request being serviced by L2 as block was replaced.

9. **Corrected log:**

```
UVM_INFO ../uvm/cpu_monitor_c.sv(59) @ 1745: uvm_test_top.tb.cpu[3].monitor [cpu_monitor_c] TRIGGERED ICACHE PACKET CREATION
UVM_INFO ../uvm/system_bus_monitor_c.sv(67) @ 1775: uvm_test_top.tb.sbus_monitor [system_bus_monitor_c] Packet creation trig
gered
UVM_INFO ../uvm/system_bus_monitor_c.sv(107) @ 1815: uvm_test_top.tb.sbus_monitor [system_bus_monitor_c] Bus read or bus rea
dX successful
UVM_INFO ../uvm/system_bus_monitor_c.sv(125) @ 1825: uvm_test_top.tb.sbus_monitor [system_bus_monitor_c] Packet to be writte
n
UVM_INFO ../uvm/cache_scoreboard_c.sv(539) @ 1845: uvm_test_top.tb.sb [cache_scoreboard_c] cpu_mon_packet from CPU3:
-------------------------------------------------
Name            Type              Size  Value
-------------------------------------------------
packet          cpu_mon_packet_c  -     @7671
  dat           integral          32    'haaaa5555
  address       integral          32    'h30020000
  num_cycles    integral          32    'h1
  illegal       integral          1     'h0
  request_type  request_t         1     READ_REQ
  addr_type     addr_t            32    ICACHE
-------------------------------------------------

UVM_INFO ../uvm/cache_scoreboard_c.sv(293) @ 1845: uvm_test_top.tb.sb [cache_scoreboard_c] CHECK_DATA CPU3
UVM_INFO ../uvm/cache_scoreboard_c.sv(295) @ 1845: uvm_test_top.tb.sb [cache_scoreboard_c] Data match!!! expected = aaaa5555
 received = aaaa5555
UVM_INFO ../uvm/cache_scoreboard_c.sv(430) @ 1845: uvm_test_top.tb.sb [cache_scoreboard_c] System bus activity matched for t
his request
UVM_INFO ../uvm/cache_scoreboard_c.sv(431) @ 1845: uvm_test_top.tb.sb [cache_scoreboard_c] Expected & Received SBUS Packet
-------------------------------------------------------------
Name                        Type             Size  Value
-------------------------------------------------------------
s_packet                    sbus_packet_c    -     @7849
  bus_req_type              bus_req_t        32    BUS_RD
  bus_req_proc_num          bus_req_proc_t   32    REQ_PROC3
  req_address               integral         32    'h30020000
  bus_req_snoop             integral         4     'h0
  req_serviced_by           serv_by_t        32    SERV_L2
  rd_data                   integral         32    'haaaa5555
  wr_data_snoop             integral         32    'h0
  snoop_wr_req_flag         integral         1     'h0
  cp_in_cache               integral         1     'h0
  shared                    integral         1     'h0
  service_time              integral         32    'h0
  proc_evict_dirty_blk_addr integral         32    'h0
  proc_evict_dirty_blk_data integral         32    'h0
  proc_evict_dirty_blk_flag integral         1     'h0
-------------------------------------------------------------
```