

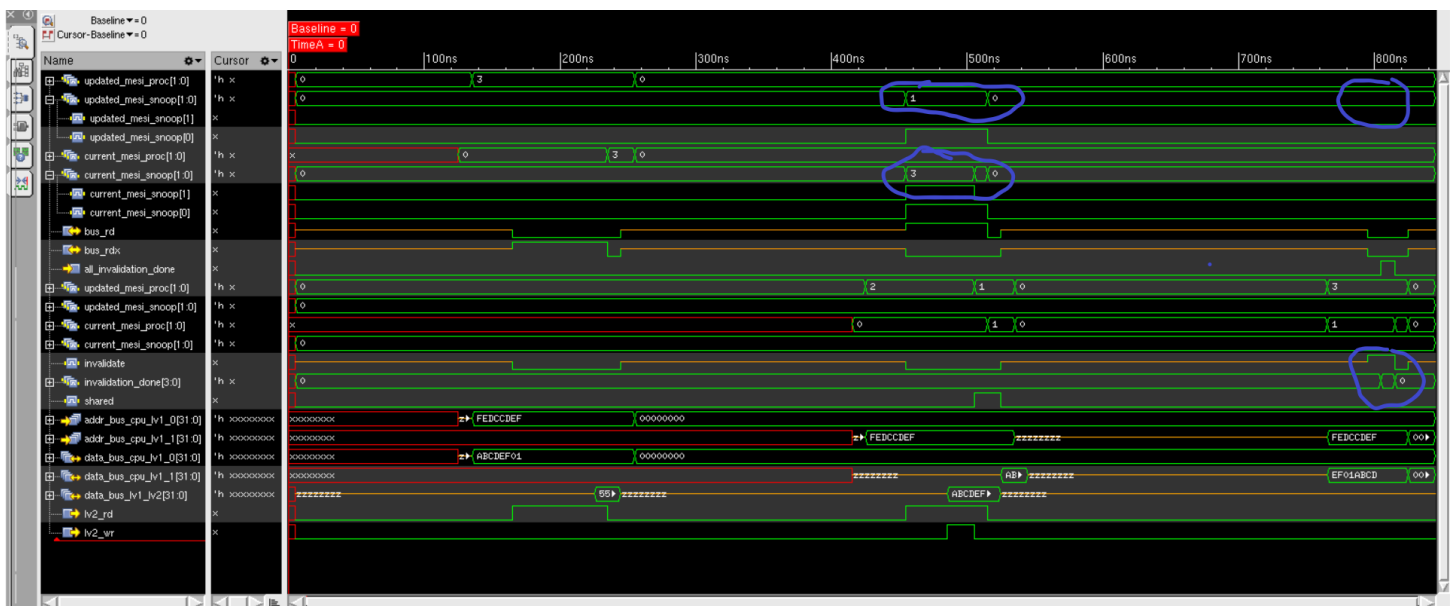
Bug-10 Report

Group-8

1. **Failing Test name** – MESI Testing for the data cache, MSI sequence testing
2. **Test description (Describe the planned scenario and the expected result)**

Making a block into Modified state by performing write operation on a specific address in core1. Read operation is performed on the same address from core2, it is 'read miss' condition so MESI state of the modified block in core1 will change to 'S'. Write operation is performed on the same address from core2, it is 'write hit' condition so MESI state of the block in core2 changes to 'M' whereas MESI state of the block with same address in core1 changes to 'I'.

3. **Failing assertion that helped you identify the bug**



4. **Debugging:** Verified outputs from the waveform by simulating the test and by following processor read miss and then write hit steps from HAS document.
For write hit on the proc side, MESI is in 'S' state then bus_lv1_lv2_gnt_proc is made high then address of the block to be invalidated is sent through addr_bus_lv1_lv2. Along with this invalidate is made high indicating to other processors to make this address MESI state to 'I'. When all the processors make this address MESI state to 'I' then all_invalidation_done is asserted then MESI of proc is updated. The cpu_wr_done signal is raised.
For snoop side MESI of proc is made Invalid, invalidation_done is raised and then shared_local is asserted.
In the above waveform it can be observed that the shared is high when invalidation_done is raised
5. **Erroneous RTL file name** – main_func_lv1_dl.sv
6. **Lines of RTL file responsible for the bug** Line 297: `CACHE_CURRENT_MESI_SNOOP <= updated_mesi_proc;
7. **Corrected RTL code** Line 297: `CACHE_CURRENT_MESI_SNOOP <= updated_mesi_snoop;
8. **Corrected Wave form**

