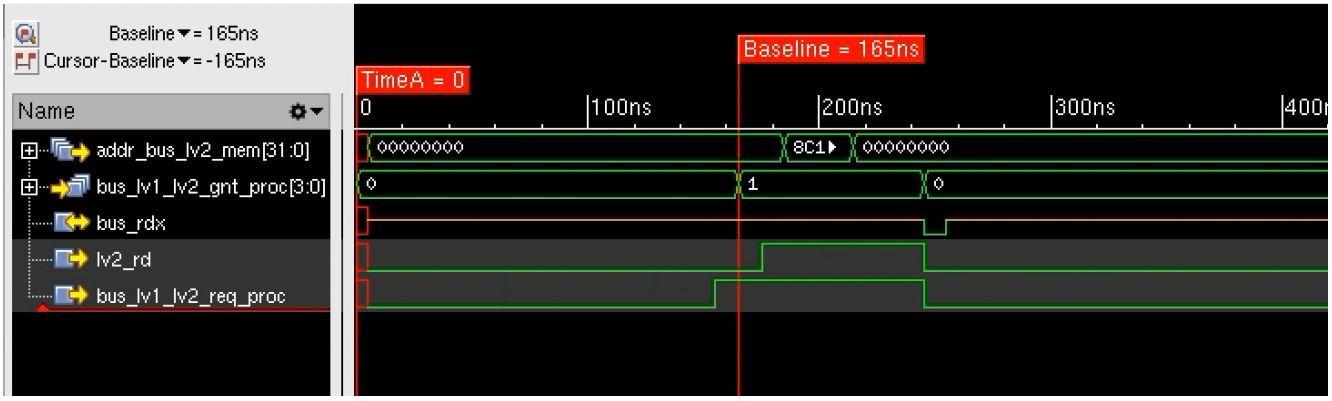
Bug-3 Report
Group-8

1. **Failing Test name -** Data cache Write Miss Test

2. **Test description (Describe the planned scenario and the expected result)-** write_miss_dcache: Performing write operation on different CPU's and checking whether the read operation on same address is working or not

3. **Failing assertion that helped you identify the bug**



4. **Brief description of diagnosis:** Verified outputs from the waveform by simulatingthe test (write_miss_dcache.sv) and by following processor write miss steps from HAS document.
   Observed that lv2_rd has been asserted, bus_rdx has not been asserted and has the high impedance even though the bus_lv1_lv2_req_proc, bus_lv1_lv2_gnt_proc are asserted and a free block available and compulsory miss

5. **Erroneous RTL file name -** main_func_lv1_dl.sv

6. **Lines of RTL file responsible for the bug (mention the line numbers and lines of the bug)**
   Line no.248, bus_rdx_reg <= 1'bz;

7. **Corrected RTL code (only mention the corrections)**
   Line no.248, bus_rdx_reg <= 1'b1;

8. **Corrected waveform:** bus_rdx got asserted