

## Group- 8

### Bug report – 2

1. **Failing Test name** – Read miss test in Data cache
2. **Test description (Describe the planned scenario and the expected result)** – Performed read operation on data cache and verified whether we are getting data from level- 2 cache or not
3. **Debugging:** Error message was found by the score board and gave error message as data mismatch because both expected and received files are different.

```

UVM_INFO ../uvm/cache_scoreboard_c.sv(293) @ 255: uvm_test_top.tb.tb [cache_scoreboard_c] CHECK_DATA CPU0
UVM_ERROR ../uvm/cache_scoreboard_c.sv(297) @ 255: uvm_test_top.tb.tb [cache_scoreboard_c] Data MISMATCH!!!
  expected = aaaa5555 received = 00000000
UVM_INFO ../uvm/cache_scoreboard_c.sv(430) @ 255: uvm_test_top.tb.tb [cache_scoreboard_c] System bus activity matched for this request
UVM_INFO ../uvm/cache_scoreboard_c.sv(431) @ 255: uvm_test_top.tb.tb [cache_scoreboard_c] Expected & Received SBUS Packet
-----
Name          Type       Size  Value
-----
s_packet      sbus_packet_c -    @7763
bus_req_type  bus_req_t   32   BUS_RD
bus_req_proc_num bus_req_proc_t 32   REQ_PROC0
req_address   integral   32   'h40000000
bus_req_snoop integral   4    'h0
req_serviced_by serv_by_t  32   SERV_L2
rd_data       integral   32   'haaaa5555
wr_data_snoop integral   32   'h0
snoop_wr_req_flag integral   1    'h0
cp_in_cache   integral   1    'h0
shared         integral   1    'h0
service_time  integral   32   'h0
proc_evict_dirty_blk_addr integral 32   'h0
proc_evict_dirty_blk_data integral 32   'h0
proc_evict_dirty_blk_flag integral 1    'h0
-----
UVM_INFO ../uvm/cpu_driver_c.sv(83) @ 275: uvm_test_top.tb.cpu[0].driver [cpu_driver_c] Ended Driving transaction
UVM_INFO ../uvm/virtual_seqs.sv(38) @ 275: uvm_test_top.tb.vsequencer@read_miss_dcache_seq [read_miss_dcache_seq] drop_objection
UVM_INFO /opt/coe/cadence/XCELIUM/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 275
: reporter [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
---Test Summary---
---Final Test Status---
Test FAIL
xmsim: *E,ERRSEV (.../test/base_test.sv,65): (time 275 NS).
top.base_test.report_phase
-----
```



4. **Failing assertion that helped you identify the bug** - Verified outputs from the waveform by simulating the test (read\_miss\_dcache.sv) and observed that data\_bus\_cpu\_lv1 is getting '0' even though correct data is present data\_bus\_lv1\_lv2.



5. Erroneous RTL file name - main\_func\_lv1\_dl.sv

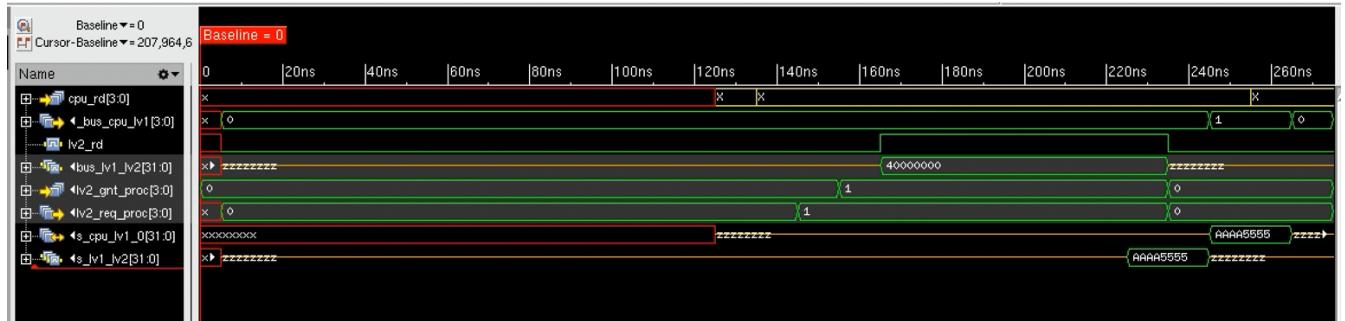
6. Lines of RTL file responsible for the bug (mention the line numbers and lines of the bug)

Line no.170, cache\_var[{index\_proc, 2'b00}] <= data\_bus\_lv1\_lv2;

7. Corrected RTL code (only mention the corrections)

Line no.170, cache\_var[{index\_proc, blk\_access\_proc}] <= data\_bus\_lv1\_lv2;

8. Corrected waveform:



9. Corrected log file:

```
UVM_INFO ..../uvm/cache_scoreboard_c.sv(293) @ 255: uvm_test_top.tb.sb [cache_scoreboard_c] CHECK_DATA CPU0
UVM_INFO ..../uvm/cache_scoreboard_c.sv(295) @ 255: uvm_test_top.tb.sb [cache_scoreboard_c] Data match!!! expected =
aaaa5555 received = aaaa5555
UVM_INFO ..../uvm/cache_scoreboard_c.sv(430) @ 255: uvm_test_top.tb.sb [cache_scoreboard_c] System bus activity matched for this request
UVM_INFO ..../uvm/cache_scoreboard_c.sv(431) @ 255: uvm_test_top.tb.sb [cache_scoreboard_c] Expected & Received SBUS
Packet
-----
Name          Type       Size  Value
-----
s_packet      sbus_packet_c  -    @7763
bus_req_type  bus_req_t   32   BUS_RD
bus_req_proc_num bus_req_proc_t 32   REQ_PROC0
req_address   integral    32   'h40000000
bus_req_snoop integral    4    'h0
req_serviced_by serv_by_t  32   SERV_L2
rd_data       integral    32   'haaaa5555
wr_data_snoop integral    32   'h0
snoop_wr_req_flag integral   1    'h0
cp_in_cache   integral    1    'h0
shared         integral    1    'h0
service_time   integral    32   'h0
proc_evict_dirty_blk_addr integral 32   'h0
proc_evict_dirty_blk_data integral 32   'h0
proc_evict_dirty_blk_flag integral 1    'h0
-----
UVM_INFO ..../uvm/cpu_driver_c.sv(83) @ 275: uvm_test_top.tb.cpu[0].driver [cpu_driver_c] Ended Driving transaction
UVM_INFO ..../uvm/virtual_seqs.sv(38) @ 275: uvm_test_top.tb.vsequencer@read_miss_dcache_seq [read_miss_dcache_seq]
drop_objection
UVM_INFO /opt/coe/cadence/XCELIUM/tools/methodology/UVM/CDNS-1.1d/sv/src/base/uvm_objection.svh(1268) @ 275: report
er [TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase
---Test Summary---
---Final Test Status---
Test PASS
[REDACTED]
```