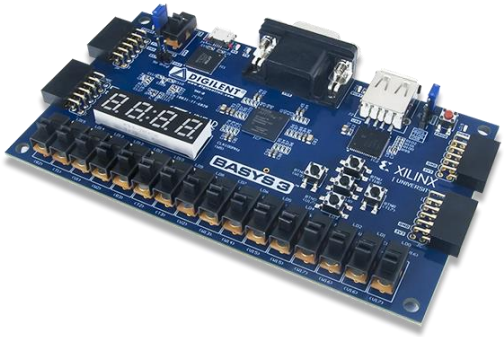
Programmable Logic Devices – Laboratory

1. FPGA development board:

Digilent Basys 3 (*Xilinx* Artix-7 FPGA)



2. Install desgin software:

Xilinx Vivado Design Suite WebPack (for 1a)

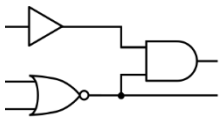
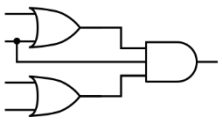
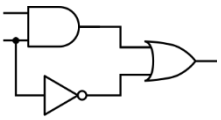
https://www.xilinx.com/products/design-tools/vivado/vivado-webpack.html

3. Go through tutorial:

https://www.xilinx.com/support/documentation/university/Vivado-Teaching/HDL-Design/2015x/VHDL/docs-pdf/Vivado_Tutorial.pdf

Mini projects (use buttons, switches and LEDs to test functionality):

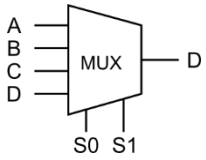
1. Design **selected** circuit:

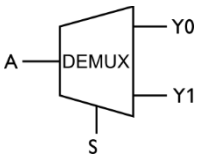
2. Design **selected** circuit:
   a. T_4={0,1,5,7,10,12,15}
   b. Y=(AB+C)D
   c. Truth table:

X1	X2	X3	X4	Y
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	-
0	1	1	0	-
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	-
1	1	1	1	-

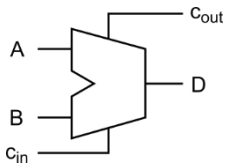
3. Design **selected** code converter:
   a. NB to 1-hot converter
   b. NB to BCD converter
   c. NB 7-segment display converter (outputs connected to 7-segment display)
4. Design multiplexer 4x1.



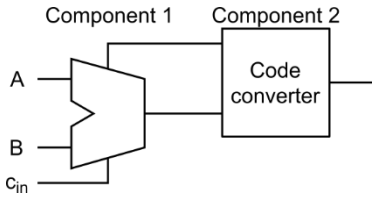
5. Design demultiplexer 1x2.



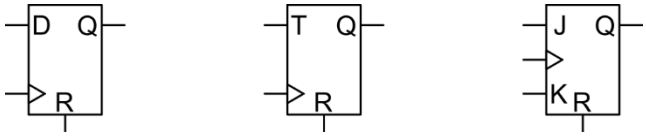
6. Design 4-bit adder.



7. Design combinational circuit, presented below, using previously designed circuit as components (VHDL port map instruction):



8. Design **selected** flip-flop witch asynchronous reset:



9. Design **selected** flip-flop with enable signal.

10. Design 8-bit shift register.
11. Design N-bit counter with synchronous reset (choose any N form 3 to 6).
12. Design modulo N counter (choose any N form 8 to 32).
13. Design frequency divider (divide input signal by 2/4/8 or 10).
14. Design selected state machine:
15. Write testbench for one previously designed circuit.

Number of mini projects accepted	Grade
8	3
9-10	3+
11-12	4
13-14	4+
15	5