

Q1] Use 2K Byte Memory chip interface 8K bytes of memory to 8088

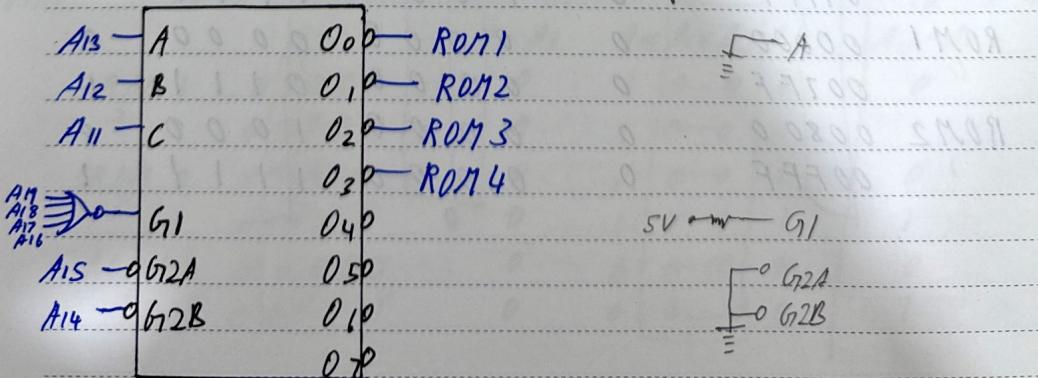
$$007FF \quad 2^11 = 2K$$

$$00FFF \quad 2^{12} = 4K$$

$$01FFF \quad 2^{13} = 8K$$

8KB - 8088 - available 2KB

	8K 01FFF							
	00000	01000	01000	01000				
	00000	01FFF	01FFF	01FFF				
ROM1	00000	00000	00000	00000	2K	2K	2K	2K
ROM2	00800	01000	01000	01000	ROM2	ROM3	ROM3	ROM4
ROM3	00FFF	017FF	017FF	017FF	00FFF	00FFF	00FFF	00FFF
ROM4	01800	01FFF	01FFF	01FFF	01800	01FFF	01FFF	01FFF
	A19-A16	A15-A14	A13-A12	A11-A10	A9-A8	A7-A6	A5-A4	A2-A0
ROM1	00000	0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0
ROM2	007FF	0	0 0 0 0	0 0 0 0	0 1 1 1	1 0 0 0	0	1
ROM3	00800	0	0 0 0 0	0 0 0 0	1 1 1 1	1 0 0 0	0	1
ROM4	00FFF	0	0 0 0 0	0 0 0 1	0 0 0 0	0 1 1 1	1 0 0 0	0
	A13-A16	G1	A15-A14	A13-A12	A11-A10	A9-A8	A7-A6	A5-A4
ROM1	000	040	050	050	050	050	050	050
ROM2	010	040	050	050	050	050	050	050
ROM3	020	040	050	050	050	050	050	050
ROM4	030	040	050	050	050	050	050	050
	A15-A14	A13-A12	A11-A10	A9-A8	A7-A6	A5-A4	A2-A1	A0-A1
G1	010	010	010	010	010	010	010	010
	A15-A14	A13-A12	A11-A10	A9-A8	A7-A6	A5-A4	A2-A1	A0-A1
G2A	010	010	010	010	010	010	010	010
G2B	010	010	010	010	010	010	010	010



Q2] 2K - 4K - 2716 (ROM) starting at 00000H
 2K - 8K - 6116 (SRAM) starting at 08000H
 $27 \cdot \frac{16}{8} = 2K$ $\frac{6116}{8} = 2K$ $007FF = 2^11 = 2K$
 $00FFF = 2^{12} = 4K$
 $01FFF = 2^{13} = 8K$

Available chip size:

SRAM

08000
8K
09FFF

08000
08FFF

2K

SRAM1
08000
087FF

SRAM2
08800
08FFF

SRAM3
09000
097FF

SRAM4
09800
09FFF

2K

ROM
00000
4K
00FFF

ROM2
00800
00FFF

A19-A16 A15-A14 A13-A12 A11-A10 A9-A8 A7-A6

SRAM1	08000	0	1	0	0	0	0	0	0	0
4	087FF	0	1	0	0	0	0	1	1	1

SRAM2	08800	0	1	0	0	0	1	0	0	0
5	08FFF	0	1	0	0	0	1	1	1	1

SRAM3	09000	0	1	0	0	1	0	0	0	0
6	097FF	0	1	0	0	1	0	1	1	1

SRAM4	09800	0	1	0	0	1	1	0	0	0
7	09FFF	0	1	0	0	1	1	1	1	1

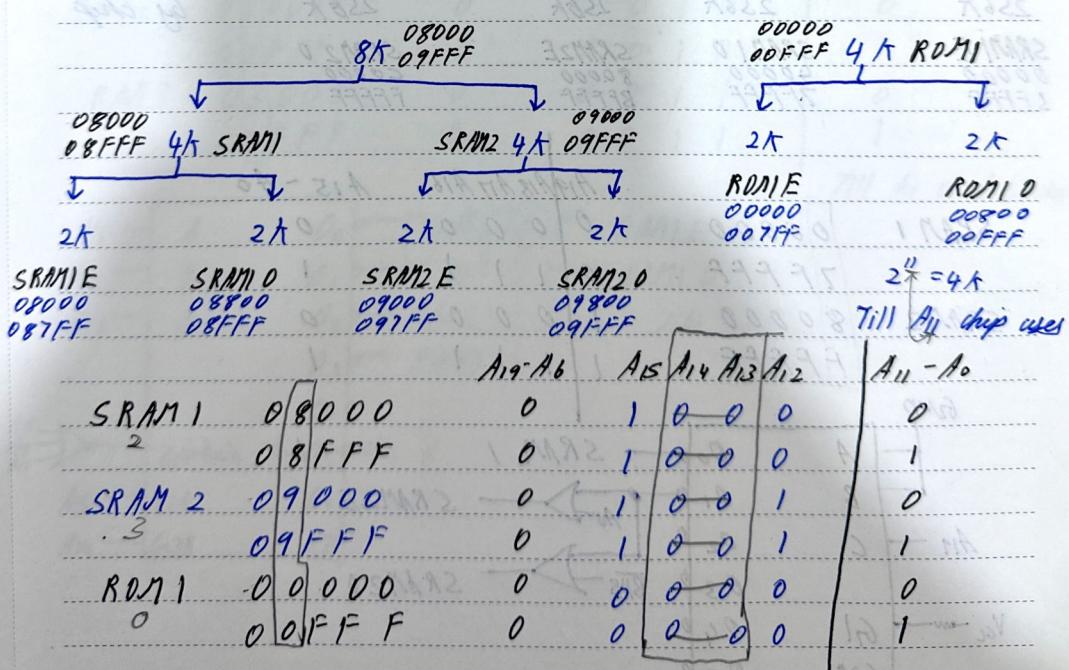
ROM1	00000	0	0	0	0	0	0	0	0	0
0	007FF	0	0	0	0	0	0	1	1	1

ROM2	00800	0	0	0	0	0	1	0	0	0
1	00FFF	0	0	0	0	0	1	1	1	1

A_{15}	A	000	— ROM1	$007FFF \quad 2^8 = 2K$
A_{12}	B	010	— ROM2	$00FFF \quad 2^{12} = 4K$
A_{11}	C	020		$01FFF \quad 2^{13} = 8K$
		030		
		040	— SRAM1	
	G1	050	— SRAM2	
A_{14}	062A	060	— SRAM3	
A_{13}	062B	070	— SRAM4	

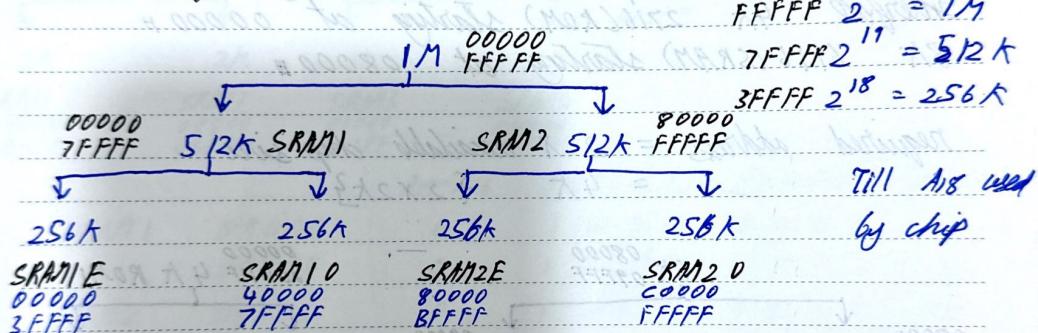
Q3] If memory chips available are only 2KB each.
 Interface 4K 2716 (RAM) starting at 00000H
 8K 6116 (SRAM) starting at 08000H

$$\text{required address} = 2 \times \text{available chip size} \\ = 4K \quad \{ 2 \times 2K \}$$



A16	A	000	$A_0 \rightarrow$	ROM1 E
A15	B	010	$BHE \rightarrow$	ROM1 O
A12	C	020	SRAM1	draw line above
		030	SRAM2	
		040		
	G1	050		
A14	G2A	060		
A13	G2B	070		

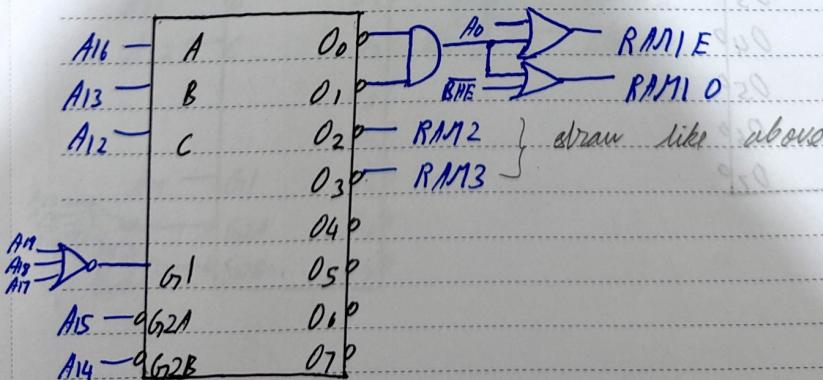
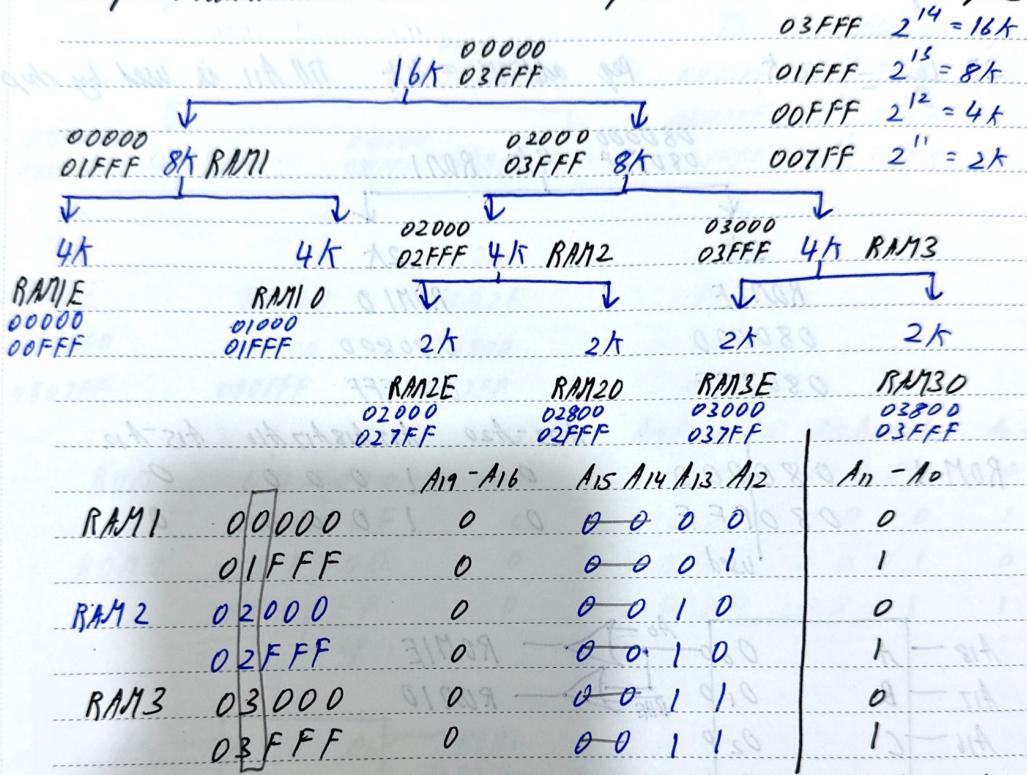
Q4] Interface 1M of SRAM to 8086 . chip available 256K each



	$A_19 A_18 A_17 A_16$	$A_{15} - A_0$
SRAM1	00000 7FFF	0 0 0 0 0
SRAM2	80000 FFFFF	0 1 1 1 1

GND	A	000	SRAM1	draw line below
	B	010	$A_0 \rightarrow$	SRAM2 E
A11	C	020	$BHE \rightarrow$	SRAM2 O
Vcc	G1	040		
	G2A	050		
	G2B	060		
		070		

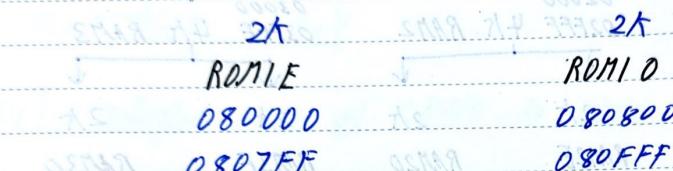
Q5] Interfall 16K of RAM to 8086 starting at 00000. chip available are 2ABC(4 chips) and 4KB(2 chips)



Q6] Interface 4K of ROM to 80286 starting at 080000₁₆
 chip available are 2716

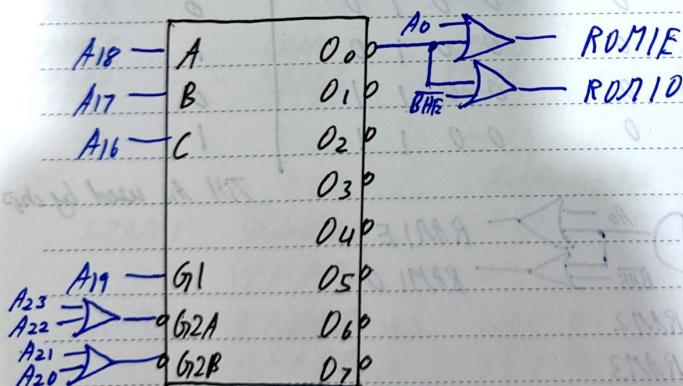
$\frac{27}{8} = 2K$ pg address = 4K till A11 is used by chip

080000
080FFF 4K ROM1

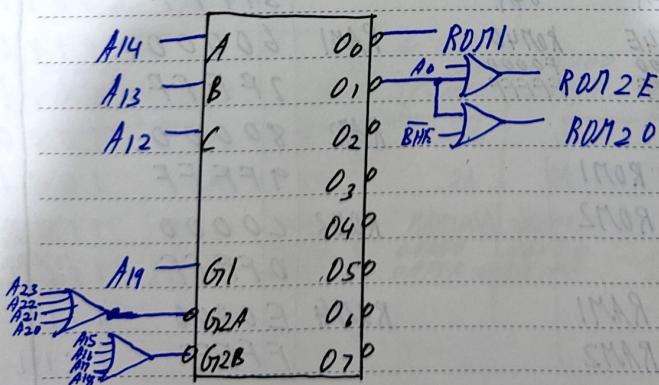
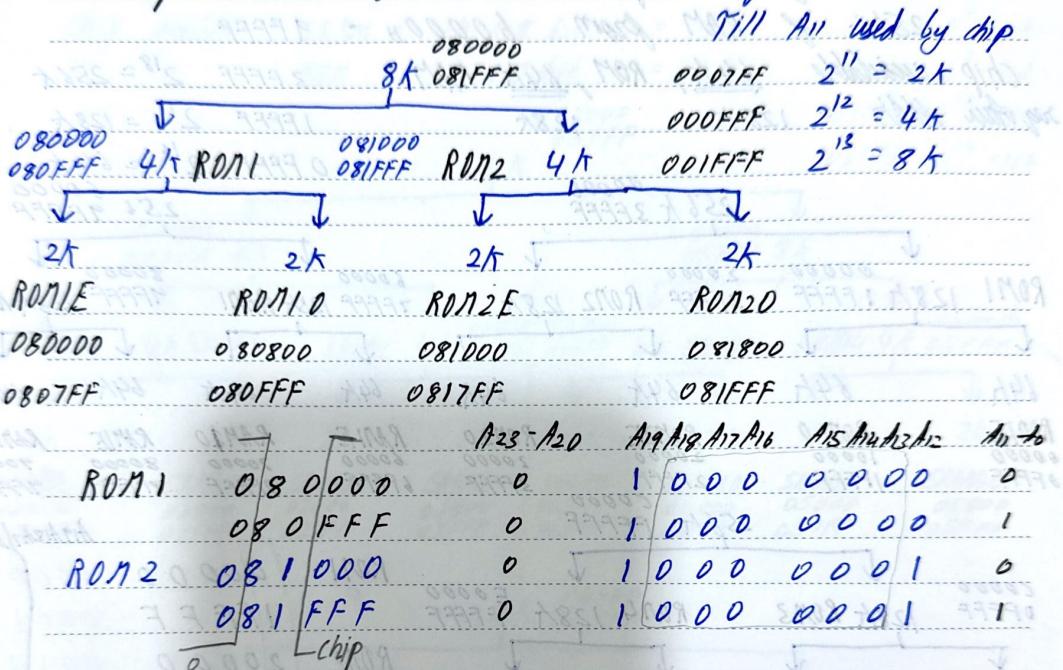


	A23-A20	A19	A18-A17	A16	A15-A12
ROM1	080000	0	1	0 0 0	0
	080FFF	0	1	0 0 0	0

used



Q7] Interface 8k of ROM to 80286 starting at 080000H
 chip available are 2KB each. Pg add = 4k



Till A16 chip uses

8686

Q8] 256K of ROM from 00000H - 3FFFF

256K of ROM from C0000H - FFFFF

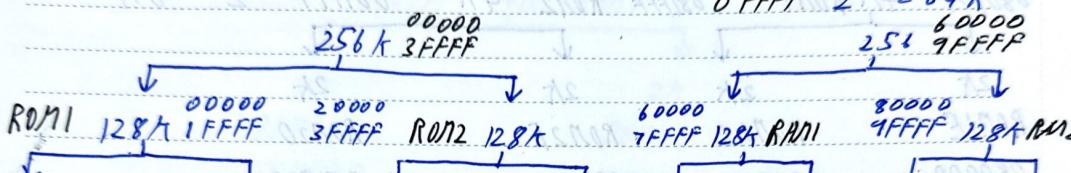
256K of RAM from 60000H - 9FFFF

chip available 64K, ROM, 64K RAM : $3\text{FFFF } 2^8 = 256\text{K}$

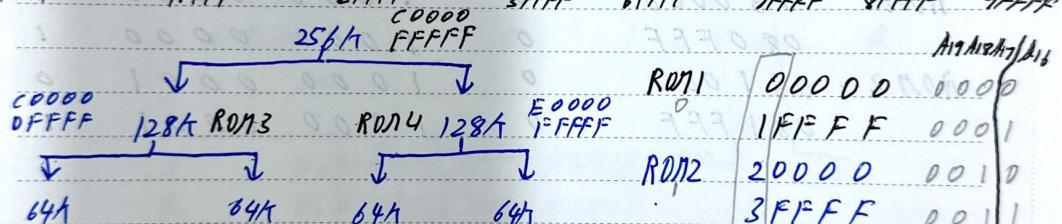
reg chain address = 128K 128K $1\text{FFFF } 2^7 = 128\text{K}$

$0\text{FFFF } 2^6 = 64\text{K}$

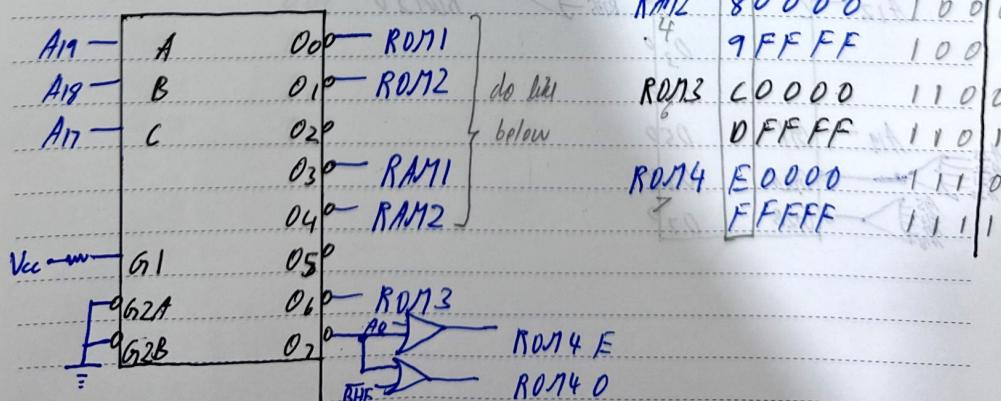
$256\text{K } 60000\text{H } 9\text{FFFF}$



ROM1	128K 00000H 1FFFFF	128K 20000H 3FFFFF	128K 60000H 7FFFFF	128K 80000H 9FFFFF
ROM1E	64K 00000H 0FFFFF	64K 10000H 1FFFFF	64K 20000H 2FFFFF	64K 30000H 3FFFFF
ROM1I	64K 40000H 4FFFFF	64K 50000H 5FFFFF	64K 60000H 6FFFFF	64K 70000H 7FFFFF
RAM1E	64K 80000H 8FFFFF	64K 90000H 9FFFFF	64K A0000H AFFFFF	64K B0000H BFFFFF
RAM1I	64K C0000H CFFFFF	64K D0000H DFFFFF	64K E0000H EFFFFF	64K F0000H FFFFFF



ROM3E	128K ROM3	128K ROM4	128K RAM1	128K RAM2
00000H CFFFFF	00000H 0FFFFF	00000H EFFFFF	00000H FFFFFF	00000H FFFFFF
01000H 0FFFFF	01000H 0FFFFF	01000H 1FFFFF	01000H 1FFFFF	01000H 1FFFFF



b : bites

standard form → B: Bytes

8bites = 1 Bytes

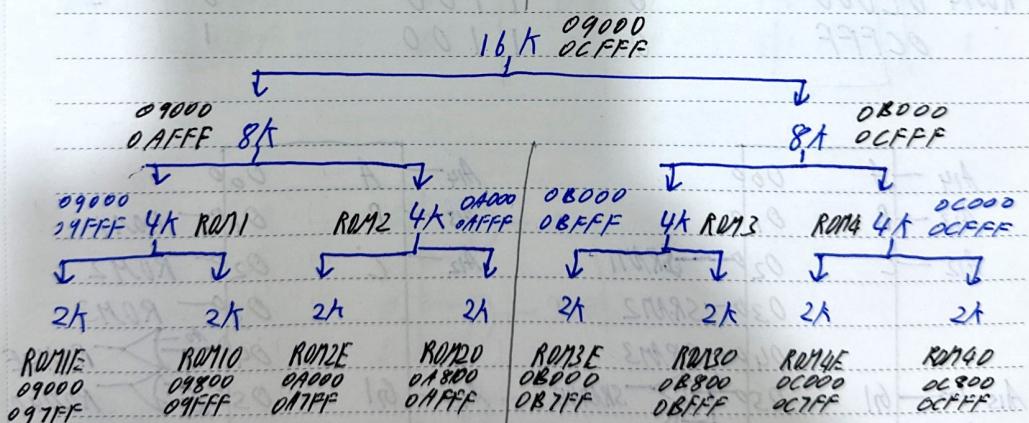
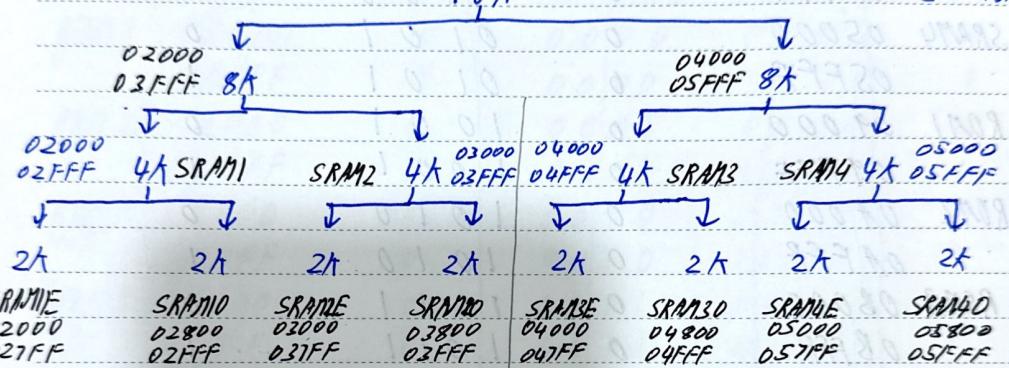
convert to bytes

8086

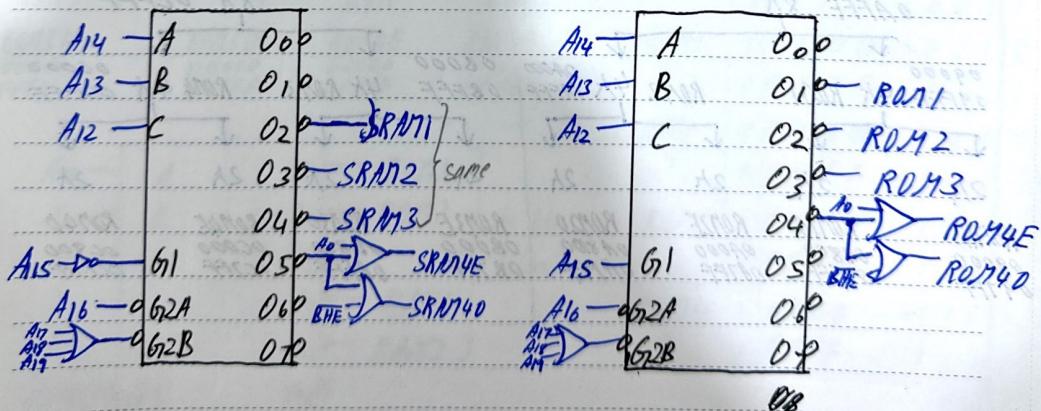
Q9] SRAM: 16KB from 02000H - 05FFF

ROM: 16KB from 09000H - 0CFFFF

chip available SRAM = $2K \times 8\text{ bit} = 2KB$ $007FFF \cdot 2^0 = 2K$
 ROM = $2K \times 8\text{ bit} = 2KB$ $00FFF \cdot 2^{12} = 4K$
 02000 $05FFF$ $01FFF \cdot 2^{13} = 8K$
 $03FFF \cdot 2^{14} = 16K$



	chip	A19-A16	A15	A14	A13	A12	A11-A10	
SRAM1	02000	-	0	0	1	0	0	2
	02FFF	-	0	0	0	1	0	
SRAM2	03000	-	0	0	0	1	1	3
	03FFF	-	0	0	0	1	1	
SRAM3	04000	-	0	0	1	0	0	4
	04FFF	-	0	0	1	0	1	
SRAM4	05000	-	0	0	1	0	0	5
	05FFF	-	0	0	1	0	1	
RDM1	09000	-	0	1	0	0	1	1
	09FFF	-	0	1	0	0	1	
RDM2	0A000	-	0	1	0	1	0	2
	0AFFF	-	0	1	0	1	1	
RDM3	0B000	-	0	1	0	1	0	3
	0BFFF	-	0	1	0	1	1	
RDM4	0C000	-	0	1	1	0	0	4
	0CFFF	-	0	1	1	0	1	



8088

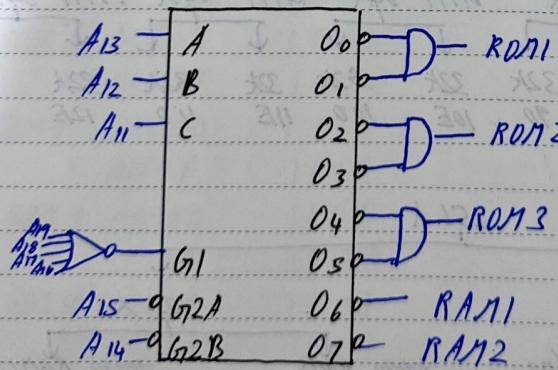
910] 4K ROM - 2732 chip for address 00000 - 02FFFF
 2K RAM - 4016 chip for address 03000 - 03FFFF

$$00FFF \cdot 2^{12} = 4K$$

$$27 \cdot 32 = 4K \quad 2 = 16 \cdot 16 = 2K \Rightarrow \cancel{\text{RAM}} \quad 01FFF \cdot 2^{13} = 8K$$

$$007FF \cdot 2^7 = 2K$$

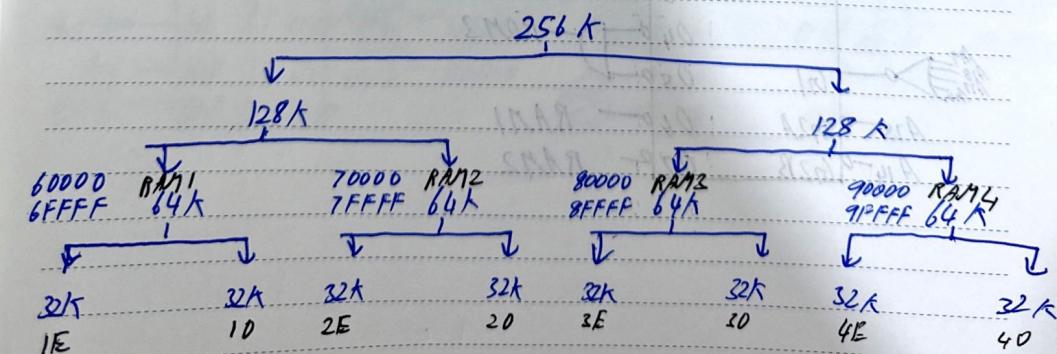
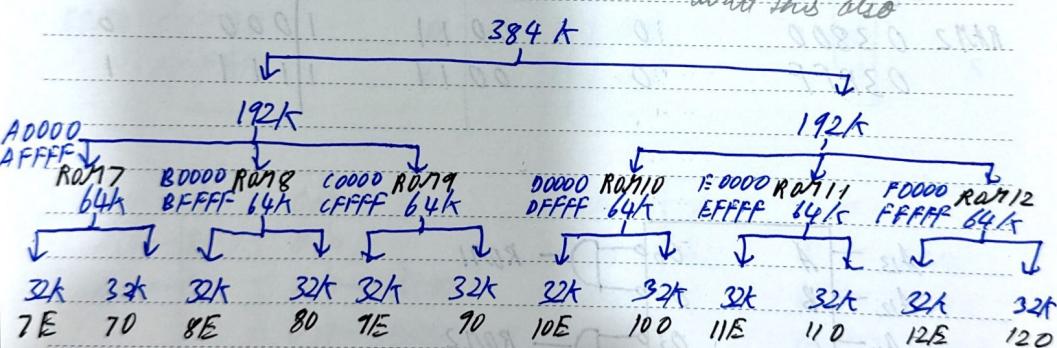
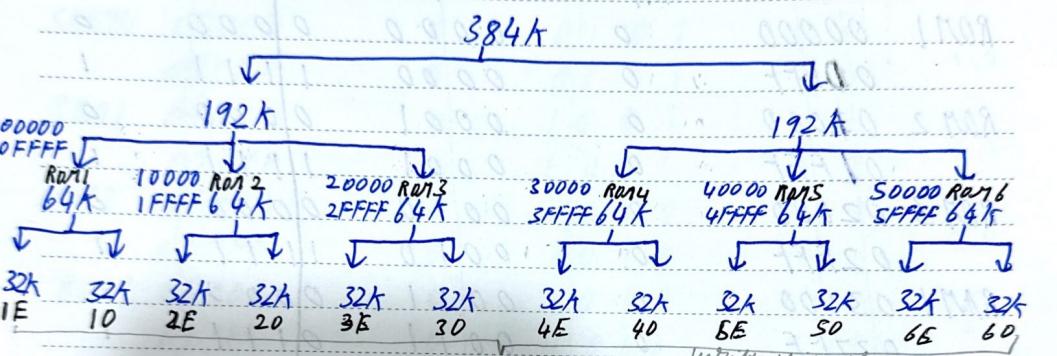
	A19-A16	A15A14A13A12	A11A10A9A8	A7-A10
ROM1 0,1	00000	0 0 0 0	0 0 0 0	0
	00FFF	0 0 0 0	1 1 1 1	1
ROM2 2,3	02000	0 0 0 1	0 0 0 0	0
	01FFF	0 0 0 1	1 1 1 1	1
ROM3 4,5	02000	0 0 1 0	0 0 0 0	0
	02FFF	0 0 1 0	1 1 1 1	1
RAM1 6	03000	0 0 1 1	0 0 0 0	0
	037FF	0 0 1 1	0 1 1 1	1
RAM2 7	03800	0 0 1 1	1 0 0 0	0
	03FFF	0 0 1 1	1 1 1 1	1



$$0 FFFF \quad 2^{16} = 64K$$

8086

Q1L] 384 K - ROM from 00000H - ~~8086 value~~
 384 K - ROM from A0000H - ~~8086 value~~
 256 K - RAM from 60000H
 chip available 32K ROM, 32K RAM - 8, LS138-4
 req 64K 64K



Till A15 used by chip

		A ₉ A ₈ A ₇ A ₆			
RAM1	0 0 0 0 0	0 0 0 0	A ₁₈ — A	0 0	— RAM1
	0 FFFF	0 0 0 0	A ₁₇ — B	0 1	— RAM2
RAM2	1 0 0 0 0	0 0 0 1	A ₁₆ — C	0 2	— RAM3
	1 FFFF	0 0 0 1		0 3	— RAM4
RAM3	2 0 0 0 0	0 0 1 0		0 4	— RAM5
	2 FFFF	0 0 1 0		0 5	— RAM6
RAM4	3 0 0 0 0	0 0 1 1	A ₁₅ — G1	0 5	— RAM6
	3 FFFF	0 0 1 1	A ₁₀ — G2A	0 6	— RAM1
RAM5	4 0 0 0 0	0 1 0 0	E — G2B	0 7	— RAM2
	4 FFFF	0 1 0 0			
RAM6	5 0 0 0 0	0 1 0 1			Use A10 & BHE
	SFFFF	0 1 0 1			
RAM7	6 0 0 0 0	0 1 1 0	A ₁₈ — A	0 0	— RAM3
	6 FFFF	0 1 1 0	A ₁₇ — B	0 1	— RAM4
RAM2	7 0 0 0 0	0 1 1 1	A ₁₆ — C	0 2	— RAM7
	7 FFFF	0 1 1 1		0 3	— RAM8
RAM3	8 0 0 0 0	1 0 0 0		0 4	— RAM9
	8 FFFF	1 0 0 0	A ₁₅ — G1	0 5	— RAM10
RAM4	9 0 0 0 0	1 0 0 1	BHE — G2A	0 6	— RAM11
	9 FFFF	1 0 0 1	E — G2B	0 7	— RAM12
RAM7	A 0 0 0 0	1 0 1 0			
	A FFFF	1 0 1 0			
RAM8	B 0 0 0 0	1 0 1 1			
	B FFFF	1 0 1 1			
RAM9	C 0 0 0 0	1 1 0 0			
	C FFFF	1 1 0 0			
RAM10	D 0 0 0 0	1 1 0 1			
	D FFFF	1 1 0 1			
RAM11	E 0 0 0 0	1 1 1 0			
	E FFFF	1 1 1 0			
RAM12	F 0 0 0 0	1 1 1 1			
	F FFFF	1 1 1 1			

8088

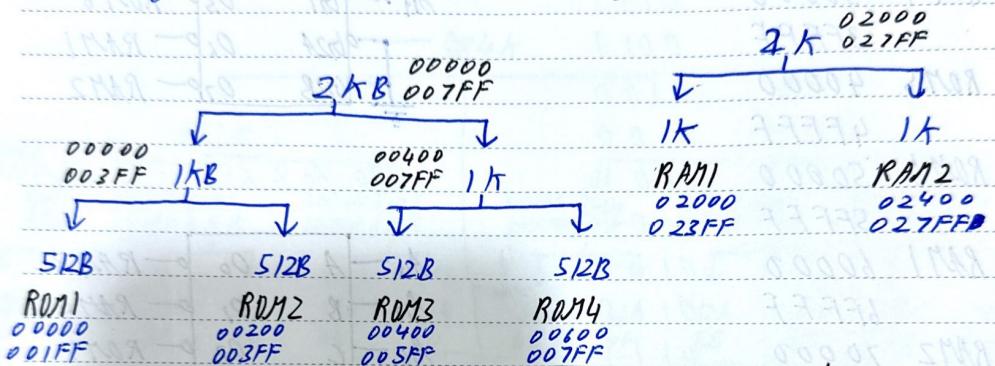
Q12] 512 - 2K - ROM from 00000.H - 007FF

512 - 2K - RAM from 02000.H - 027FF

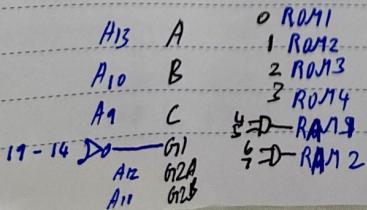
chips available 2704, 1608, LS138 003FF $2^{10} = 1K$
 $001FF \cdot 2^7 = 512B$

$$\frac{27}{8} \cdot \frac{04}{8} = 512 \text{ bytes}$$

$$\frac{16}{8} \cdot \frac{08}{8} = 1 KB$$



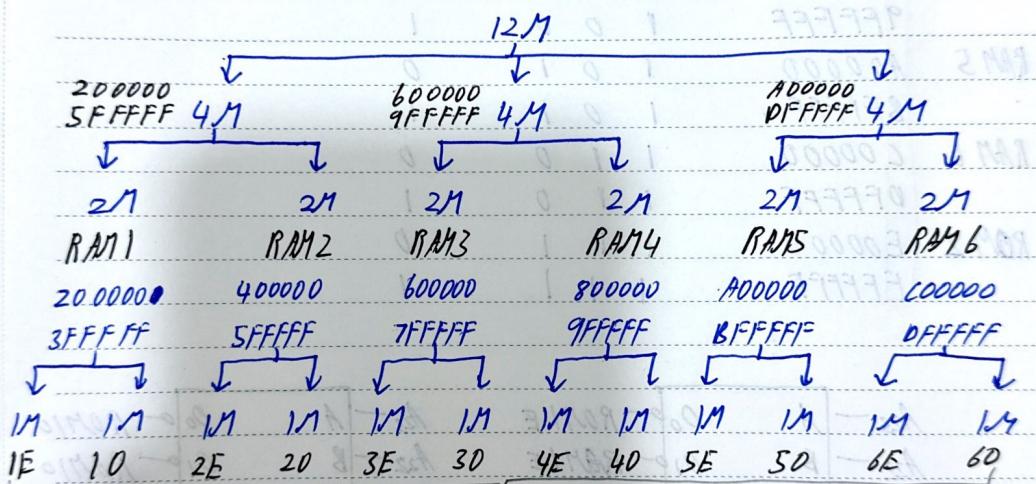
	A19-A16	A15	A14	A13-A12	A11	A10	A9	A8	A7-A0
ROM1	00000	0	0	0	0	0	0	0	0
	001FF	0	0	0	0	0	1	1	1
ROM2	00200	0	0	0	0	0	1	0	0
	003FF	0	0	0	0	0	1	1	1
ROM3	00400	0	0	0	0	0	1	0	0
	005FF	0	0	0	0	0	1	0	1
ROM4	00600	0	0	0	0	0	1	0	0
	007FF	0	0	0	0	0	1	1	1
RAM1	02000	0	0	0	1	0	0	0	0
	023FF	0	0	0	1	0	0	1	1
RAM2	02400	0	0	0	1	0	0	1	0
	027FF	0	0	0	1	0	0	1	1



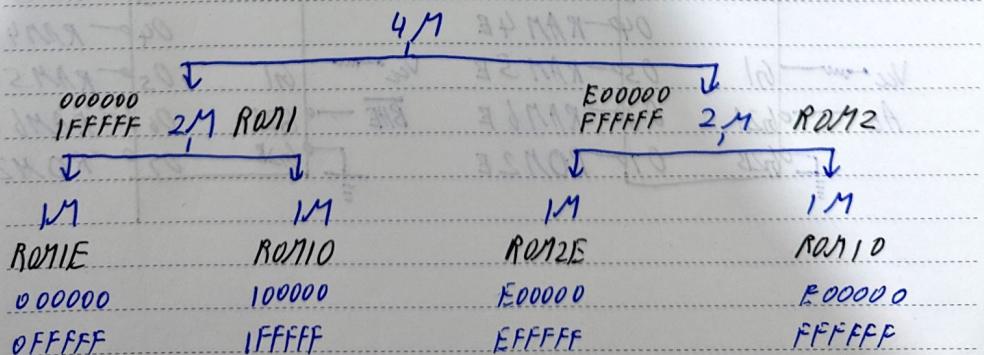
Q13] For an 80286 processor, that has 16MB of memory of which 4M is ROM and the rest is RAM. Half of the ROM - mapped from 00 0000H other from E0 0000H. RAM is from 20 00 00H. chips available are

1M ROM, 1M RAM, LS-138-2

000000 0FFFFF $2^{20} = 1MB$
 2M 4M - ROM < E0 00 00 1FFF $2^{21} = 2MB$
 2M 12M - RAM - 20 00 00H - 3FFF $2^{22} = 4MB$
 7FFF $2^{23} = 8MB$



write for them also in exam



Till A₂₀ is used by the chip

A₂₃ A₂₂ A₂₁ A₂₀ A₀

RAM 1	000000	0 0 0	0 0
	1FFFFFF	0 0 0	1
RAM 1	200000	0 0 1	0
	3FFFFFF	0 0 1	1
RAM 2	400000	0 1 0	0
	5FFFFFF	0 1 0	1
RAM 3	600000	0 1 1	0
	7FFFFFF	0 1 1	1
RAM 4	800000	1 0 0	0
	9FFFFFF	1 0 0	1
RAM 5	A00000	1 0 1	0
	BFFFFFF	1 0 1	1
RAM 6	C00000	1 1 0	0
	DFFFFFF	1 1 0	1
RAM 2	E00000	1 1 1	0
	FFFFFFFF	1 1 1	1

A ₂₃ — A	00 — ROM1E	A ₂₃ — A	00 — ROM10
A ₂₂ — B	01 — RAM1E	A ₂₂ — B	01 — RAM10
A ₂₁ — C	02 — RAM2E	A ₂₁ — C	02 — RAM20
	03 — RAM3E		03 — RAM30
	04 — RAM4E		04 — RAM40
V _{cc} — G1	05 — RAM5E	V _{cc} — G1	05 — RAM50
A ₀ — G2A	06 — RAM6E	G2A — G2B	06 — RAM60
I — G2B	07 — ROM2E	G2B — M1	07 — ROM20