**BPDC, Dubai - First Semester,**

**DEPARTMENT OF CS**

|  |  |  |
| --- | --- | --- |
| **Course No: CS F342** | **TUTORIAL 9** | **Course Title: Computer Architecture** |

1. Identify all data dependencies beside each instruction. Work out and diagram the *optimal* pipeline schedule using forwarding from EX or MEM stages to any other stage, then compute the pipeline CPI:

lw $t2, 60($t1)

lw $t1, 40($t2)

slt $t1, $t1, $t2

sw $t1, 20($t2)

**cc1 cc2 cc3 cc4 cc5 cc6 cc7 cc8 cc9 cc10**

**L\_1 lw $t2, 60($t1) IF ID Ex MEM WB**

**L\_2 lw $t1, 40($t2) Stall IF ID EX MEM WB**

**L\_3 slt $t1, $t1, $t2 Stall IF ID EX MEM WB**

**L\_4 sw $t1, 20($t2) IF ID EX MEM WB**

**CPI = \_10\_\_ cycles / \_4\_\_ instructions = \_\_2.5 cycles per instruction\_\_\_**

1. A MIPS pipeline has the following timings for the different stages. IF = 150ps, Reg Rd=100ps, ALU op=150ps, MEM Data Access=300ps, Reg Wr=100ps.
2. What is the Tc of Single Cycle based CPU, & the Tc for Pipelined CPU?
3. Diagrammatically show the non-pipelined vs pipelined execution of the following three instructions. (Timing scale to be shown)

ld $1, 1000($2)

add $3, $2, $4

sub $6, $2, $4

sw $5, 1000($2)

1. Consider an instruction pipeline with four stages with the stage delays 5 nsec, 6 nsec, 11 nsec, and 8 nsec respectively. The delay of an inter-stage register stage of the pipeline is 1 nsec. What is the approximate speedup of the pipeline in the steady state under ideal conditions as compared to the corresponding non-pipelined implementation?

Time taken to execute N instructions in non-pipelined implementation will

be (5 + 6 + 11 + 8)N = 30N

Clock period for pipelined implementation = max{5,6,11,8} + 1 = 12.

Time taken for the pipelined implementation = (3 + N)12 = 12N (approx.)

1. Speedup = 30N / 12N = 2.5
2. Identify all data dependencies beside each instruction. Work out and diagram the *optimal* pipeline schedule using forwarding from EX or MEM stages to any other stage, then compute the pipeline CPI:

lw $t1, 120($t0)

lw $t0, 80($t1)

add $t0, $t0, $t1

sw $t0, 90($t1)

sub $t1, $t0, $t1

sw $t1, 90($t0)

