BITS PILANI DUBAI CAMPUS

DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI UAE

BITS Pilani
Dubai Campus

II SEM 2016-2017

Evaluation Component: **Test-II (Open Book)**	Date/Time/Duration: **11-APR-2017, Tuesday 08:30AM to 09:20AM (50 Mins)**
Course No : **CS/ECE/EEE/INSTR F241**	Course Name : **MIRCOPROC & INTERFACING**
Maximum Marks : **60**	Weightage : **20%**

Note: Answer all the questions and any missing data can be assumed suitably

Q.1 Write an assembly language program to add two 16 digit hexadecimal numbers available in memory locations 2001H and 2004H using Macro (use macro name as 'MYADD'). Store the sum with carry in memory location 4000H. **08M**

(Note: Complete program is not required write only core part of the program)

Q.2 Write an assembly program to read a lower case alphabet from the keyboard and display its upper case equivalent on the console **07M**

(Hex ASCII values for 'a' to 'z' is 61H to 7AH and 'A' to 'Z' is 41H to 5AH)

(Note: Complete program is not required write only core part of the program)

Q.3 Consider a 16-bit microprocessor, with a 16-bit external data bus, driven by an 5-MHz input clock. In the given program

Program	Machine code
Mov AX, 4000h	**B80040**
Mov DS, AX	**8ED8**
Mov ECX, CC001267h	**66B9671200CC**
Mov EAX, 4020[BX+DI]	**668B812040**

a. What is the number and type of the machine cycle required for executing each line in the program? **4+**
b. What is the total number of machine cycle and instruction cycle required to execute the entire program? **0.5+**
c. What is the number of T states required for executing each line in the program? **2+**
d. What is the total number of T states required to execute the entire program? **0.5+**
e. What is the time required for executing each line in the program without any wait state? **2+1=10M**
f. What is the total time required to execute the entire program without any wait state?

Q.4	For a paging enabled system, the linear address is 00ED4225. CR3 = 20000000 Find the physical address. Given following tables: **Page Directory** **Address** / **Data** 20000000 / 06000000 20000004 / 07000000 20000008 / 08000000 2000000C / 09000000 20000010 / 0A000000 20000014 / 0B000000 20000018 / 0C000000 **Paging Table** **Address** / **Data** 09000B44 / 3A000000 09000B48 / 3B000000 09000B4C / 3C000000 09000B50 / 3D000000 09000B54 / 3E000000 09000B58 / 3F000000 09000B5C / 40000000	**15M**
Q.5	Design an 80286 based system that has the following memory requirements: • 192K of ROM with a starting address 000000H • 128K of RAM with starting address 050000H The following chips are available • 27256, 16256, and LS138. Design the memory interfacing circuit. Use absolute addressing.	**20M**

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Evaluation Component: **Compre Exam (Closed Book)**	Date/Time/Duration: **25-MAY-2017, THURSDAY 12:30PM to 03:30PM (03 Hours)**
Course No : **CS/ECE/EEE/INSTR F241**	Course Name : **MIRCOPROC & INTERFACING**
Maximum Marks : **90**	Weightage : **30%**

Note: Answer all the questions and any missing data can be assumed suitably

Answer Part A and Part B in a separate answering book

PART A

Q.1 The content of the following registers are CS=1111H, DS=3333H, SS=2526H, IP=1232H and DI=0020H. Calculate the corresponding physical and ending addresses for the bytes in CS, DS and SS. (8086 is working under real mode operation) — 3M

Q.2 What will be the content of status flags in 8086 after performing the following arithmetic operation? — 3M

a) 92 + 69
b) 5CH + C5H

Q.3 Fill the following table based on the control bus of 8086 — **2M**

M/IO'	RD'	WR'	Bus Cycle
1	0	?	?
1	1	?	?
0	0	?	?
0	1	?	?

Q.4 Find the number of machine cycle, the T- states and the total time required for executing the following instructions (Input clock frequency is 2 MHz) — **9M**

i. MOV AX, [BX+10H]
ii. MOV [80+EBX], EAX
iii. MOV AX, CS:[DI+40H]

Q.5 What is bidirectional buffer and unidirectional buffer and what is the difference between them? Also discuss about the various signals used in the buffer. — **3M**

Q.6	Draw a block diagram of microcomputer organization and explain the working	**5M**
Q.7	Using diagrams and examples, explain difference between SISD, SIMD and MIMD	**5M**
Q.8	Assume a word-addressable memory system (a word is 4 bytes). Suppose the page size is 16 KB, and the physical memory is 2GB. a) If the logical addressable space is 32 bits, how many entries would the page table have? b) What is the minimum size of the page table?	**5+5=10M**

PART B

Q.1	80286-based system has the following memory requirements 224K of memory 128K ROM rest RAM. The mapping is as follows 64 K ROM with starting address 000000H 64 K ROM with starting address 0F0000H RAM with starting address 040000H Chips available: 27128. 61128. LS138. Design the memory interfacing circuit. Use absolute addressing.	**20M**
Q.2	Assuming 16-bit Intel instructions translate 67668B860210 from machine to assembly code (*Note : use the table given in Appendix*)	**5M**
Q.4	Write an ALP to transfer a block of 10 bytes of data from a location 2000h to 4000h using string instructions.	**5M**
Q.5	Interface an 8255 chip with 8086 to work as an I/O port. Initialize port A as output port, Port B as I/P port and Port C as O/P port. Port A address should be 0740H. Write an ALP to sense switch positions SW0 – SW7 connected at port B. The sensed pattern is to be displayed on port A, to which 8 LED's are connected, while port C lower displays number of on switches out of the total eight switches ?	**10M**
Q.6	Write a program to generate a square wave of 1KHz frequency on OUT 1 pin of 8253/54. Assume CLK1 frequency is 1MHz and address for control register = 0CH, counter 1 = 08H and counter 2 = 0AH	**10M**

8253/8254 Contro, word format

Control Word Format

$A_1, A_0 = 11$ $\overline{CS} = 0$ $\overline{RD} = 1$ $\overline{WR} = 0$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write

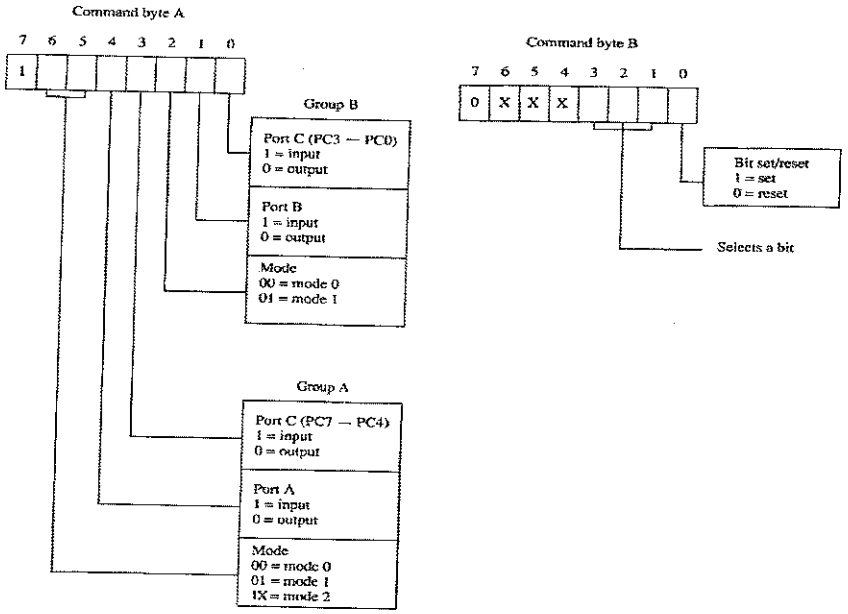
RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

8255 Contro, word format



Tables for PART B Question No.2

REG	
EAX/AX/AL	000
EBX/BX/BL	011
ECX/CX/CL	001
EDX/DX/DL	010
ESP/SP/AH	100
EBP/BP/CH	101
ESI/SI/DH	110
EDI/DI/BH	111

MOD / R/M	00	01	10	11	
				W = 0	W = 1
000	[BX] + [SI]	[BX]+[SI]+d8	[BX]+[SI]+d16	AL	AX
001	[BX] + [DI]	[BX]+[DI]+d8	[BX]+[DI]+d16	CL	CX
010	[BP] + [SI]	[BP]+[SI]+d8	[BP]+[SI]+d16	DL	DX
011	[BP] + [DI]	[BP]+[DI]+d8	[BP]+[DI]+d16	BL	BX
100	[SI]	[SI]+d8	[SI]+d16	AH	SP
101	[DI]	[DI]+d8	[DI]+d16	CH	BP
110	d16	[BP] + d8	[BP] + d16	DH	SI
111	[BX]	[BX]+d8	[BX]+d16	BH	DI

MOD / R/M	00	01	10	11	
				W = 0	W = 1
000	EAX	EAX+d8	EAX+d32	AL	EAX
001	ECX	ECX+d8	ECX+d32	CL	ECX
010	EDX	EDX+d8	EDX+d32	DL	EDX
011	EBX	EBX+d8	EBX+d32	BL	EBX
100	Scaled Index	Scaled Index +d8	Scaled Index +d32	AH	ESP
101	d32	EBP+d8	EBP+d32	CH	EBP
110	ESI	ESI+d8	ESI+d32	DH	ESI
111	EDI	EDI+d8	EDI+d32	BH	EDI

66h = operand size override
67h = address size override

```
2EH     CS segment override prefix
36H     SS segment override prefix
3EH     DS segment override prefix
26H     ES segment override prefix
64H     FS segment override prefix
65H     GS segment override prefix
66H     Operand-size override
67H     Address-size override
```

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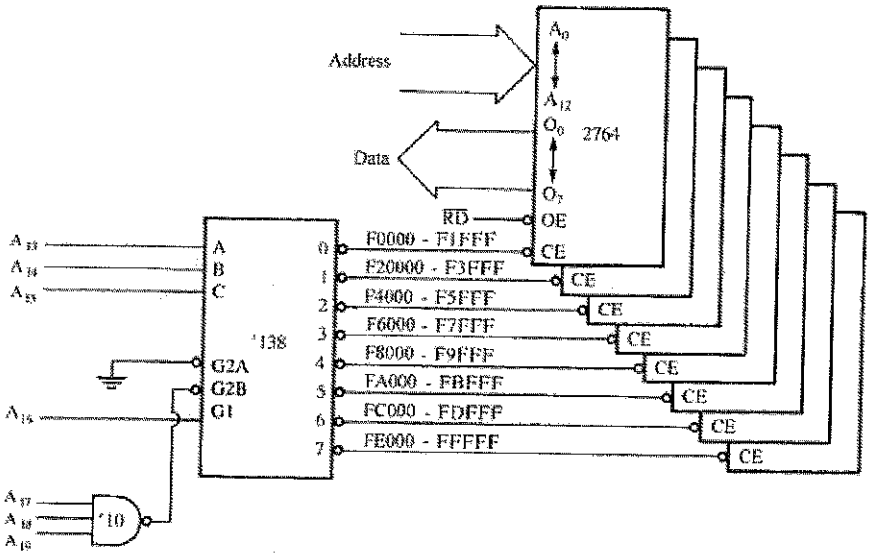
Evaluation Component: Tutorial –QUIZ-6	Date/Time/Duration: Surprise 30 Minutes
Course No : **CS/ECE/EEE/INSTR F241**	Course Name : **MIRCOPROC & INTERFACING**
Maximum Marks : **15**	Weightage : **05%**

Note: Answer all the questions and any missing data can be assumed suitably

ID.No.	**Name:**	**Faculty:**

Q.1	To address a memory location out of N memory locations, the number of address lines required is a) log N (to the base 2) b) log N (to the base 10) c) log N (to the base e) d) log (2N) (to the base e) **Ans:**	1M
Q.2	In a 8086 system, the memory requirements are: 384K ROM, 256K RAM. The available chips are 32K ROM and 16K RAM. What is the minimum number of 138 decoders needed? **Ans**:	1M
Q.3	80286-based system has the following memory requirements 640KB of memory 128KB is ROM and rest are RAM Available chip are 27256 and 61512. How many ROM and RAM chips are required for memory design. Ans: _____ _____	1M

Q.4	It is requried to interface **256 KB RAM** and **128 KB EPROM** to an **8086-2** microprocessor a) There are 4 numbers of 64KB RAM chips are available If the starting address of the RAM is **00000H**, fill-in the boundary addresses on the following memory map. RAM1 even: RAM1 odd: RAM2 even: RAM2 odd: b) **four** EPROM (32KB) chips. If the last address of the EPROM is **FFFFFH**, fill-in the boundary addresses on the following memory map. EPROM1 even: EPROM1 odd: EPROM2 even: EPROM2 odd:	4+4=8M

Q.5	Following is the address decoding circuit for the address range F0000-FFFFF  Modify the above decoder circuit for address range 70000-7FFFF Ans:	3M