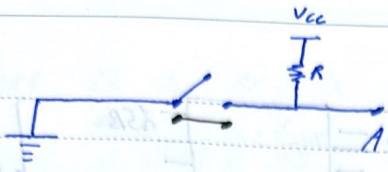
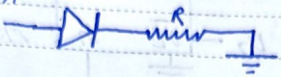


ON switch
OFF

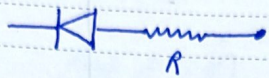
OFF 0 A

To Turn ON send 1



To Turn ON send 0

OFF 1



Acc, Port IN AL, PORT

Port, Acc OUT PORT, AL

8 bit - AL
16 bit - AX
32 bit - EAX

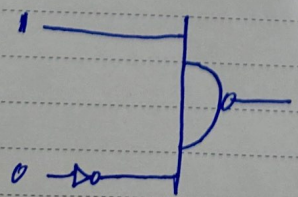
Fixed addressing
8 bit give direct address / port

Variable addressing
16 bit
move data to 'DX'
OUT DX, AL

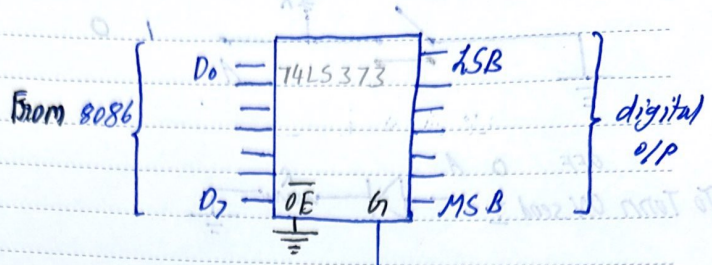
IN AL, DX

For input device use buffer to provide isolation as well as to strengthen the signal

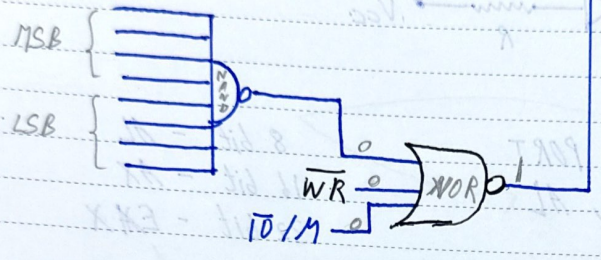
For output device use latches to retain data for longer time as the data sent by µp is available for only short period of time



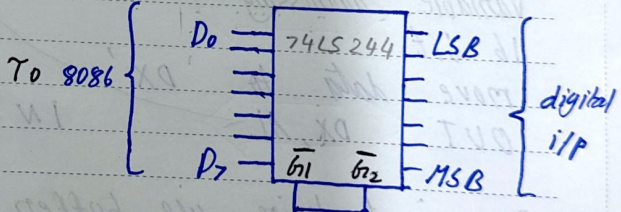
OUT → , AL

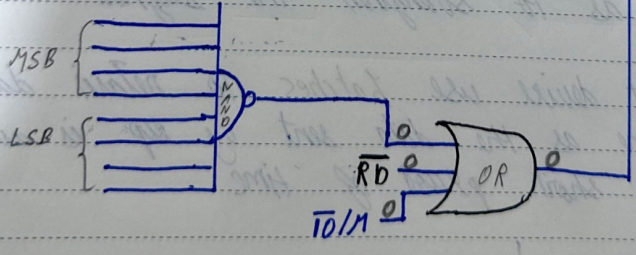


MSB LSB



IN AL, —H





8086	$\overline{CS}$	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	Port
	0	X	X	X	X	X	0	0	X	A
fixed (use to activate $\overline{CS}$)							0	1		B
if $\overline{CS}$ = 1 then 8255 not selected							1	0		C
8086							1	1		CR (control register)
8255							A_1	A_0		

Group A : Port A (8) + Upper Port C (4) (no. of pin)

Group B : Port B (8) + Lower Port C (4)

D_7 = 1 – I/O mode
0 – BSR mode

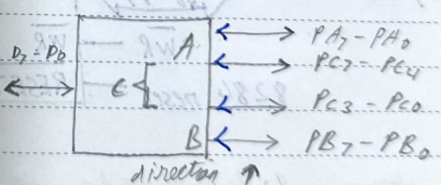
U - upper L - Lower

D_7 = 1 0 - output : 1 - input

D_7	D_6 D_5	D_4	D_3	D_2	D_1	D_0
1	Port A mode 00 - mode 0 01 - mode 1 1X - mode 2	Port A 0 - o/p 1 - i/p	U Port C 0 - o/p 1 - i/p	Port B mode 0 - mode 0 1 - mode 1	Port B 0 - o/p 1 - i/p	L Port C 0 - o/p 1 - i/p

Simple mode D_6 D_5 D_2 = 0 0 0

Max pins : 24



Here Input and output can be given to any port

Mode 0	Mode 1	Mode 2
Simple I/O (A, B, C)	Handshake I/O (A, B) C - handshake	handshake Bidirec I/O (A) B - mode 0, 1 C - handshake

D_7	D_6 D_5 D_4	D_3	D_2	D_1	D_0
0	X X X	Bit 2	Bit 1	Bit 0	1-set
	don't care				0-Reset

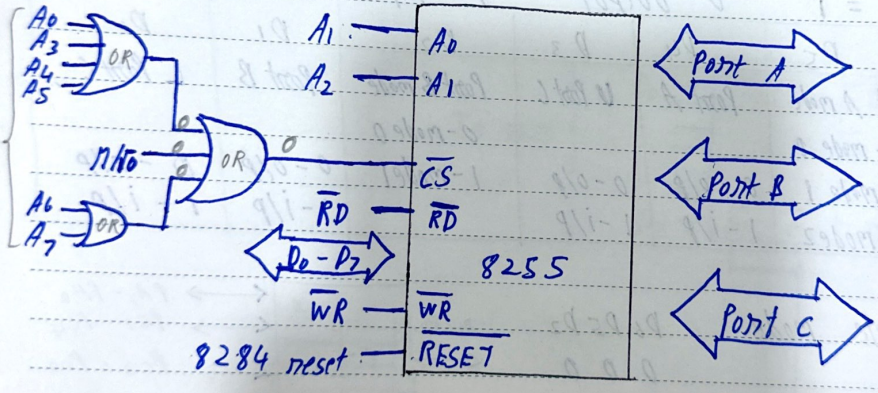
Bit 2	Bit 1	Bit 0	Port C	
0	0	0	0	PC_0
0	0	1	1	PC_1
0	1	0	2	PC_2
0	1	1	3	PC_3
1	0	0	4	PC_4
1	0	1	5	PC_5
1	1	0	6	PC_6
1	1	1	7	PC_7

In BSR you can use only CR to give I/P or O/P and only Port C works here.

General

PA	x
PB	x+2
PC	x+4
CR	x+6

General



Arrange $A_7 A_6 A_5 A_4 A_3 A_0$ in a manner that $\overline{CS}$ is 0 in order to get $\overline{CS}$ activated for selection of 8255

General Prog

i) Give address control
ii) MOV AL, CW/word
OUT Creg, AL
:

DSR Prog

"
"
"
all out are CREG