BITS PILANI DUBAI CAMPUS

DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI UAE

BITS Pilani
Dubai Campus

II SEM 2015-2016

Evaluation Component: Compre Exam	Date/Time/Duration: **02-JUN-2016 12:30PM-03:30PM/ 3 Hrs**
Course No : **CS/ECE/EEE/INSTR F241**	Course Name : **MIRCOPROC & INTERFACING**
Maximum Marks : **90**	Weightage : **30%**

Note: Answer all the questions and any missing data can be assumed suitably

Write PART A, PART B and PART C in separate answer sheets

PART A

Q.1	Draw the 8086 programmers model and Explain its constituent elements	**5M**
Q.2	Convert the following assembly instruction to machine instruction (16 bit instruction format) **MOV EAX,[ECX+2000H]** *(Tables are given in page no. 10)*	**5M**
Q.3	Convert the following machine instruction to assembly instruction **8B871020** *(Tables are given in page no. 10)*	**5M**
Q.4	The 8 data bytes are stored from memory location E000H to E007H. Write 8086 ALP to transfer the block of data to new location B001H to B008H	**5M**
Q.5	Write an ALP to find number of times letter e exist in the string "exercise", Store the count at memory ans.	**10M**

PART B

Q.1	For an 80286 processor, GDTR =100000 DS = 0050H INST –MOV AX,[4200H] Find the Physical Address, Type of Segment, Protection Level and size of the segment. (Refer to the GDT given below)	**8M**

GDT

Address	Data							
100008	00	00	82	01	00	00	FF	FF
100010	00	00	82	20	00	00	FF	FF
100018	00	00	83	03	00	00	00	3F
100020	00	00	FC	0A	00	00	00	1F
100028	00	00	DF	B0	00	00	01	FF
100030	00	00	92	B1	00	00	0F	FF
100038	00	00	B2	7B	00	00	03	FF
100040	00	00	D2	7A	00	00	07	FF
100048	00	00	9F	A1	00	00	1F	FF
100050	00	00	C4	A3	00	00	3F	FF
100058	00	00	82	B1	00	00	FF	FF
100060	00	00	B3	50	00	00	1F	FF

WISH YOU GOOD LUCK

ACCESS RIGHTS BYTE FORMAT

P	DPL	DPL	S	E	ED/C	R/W	A

E	ED/C	R/W	?
0	0	0	Data- Expands Upward – Read Only
0	0	1	Data- Expands Upward - Write
0	1	0	Data - Expand Downward – Read Only
0	1	1	Data- Expand Downward - Write
1	0	0	Code – Ignore DPL – Execute Only
1	0	1	Code – Ignore DPL – Read allowed
1	1	0	Code – Abide DPL – Execute Only
1	1	1	Code – Abide DPL – Read allowed

Q.2 If the microprocessor 80386 sends linear address 00 A3 00 34 to the paging mechanism, what is the physical address generated when the content of CR3 is FF 00 00 00 in paging enabled system. Refer tables below attached to do the same. **7M**

PD

Address	Data			
FF000000	01	00	00	00
FF000004	02	00	00	00
FF000008	03	00	00	00
FF00000C	04	00	00	00
FF000010	05	00	00	00
FF000014	06	00	00	00
FF000018	08	00	00	00
FF00001C	0A	00	00	00
FF000020	0B	00	00	00
FF000024	0C	00	00	00
FF000028	0E	00	00	00
FF00002C	0F	00	00	00

PT

Address	Data			
03000000	21	00	00	00
03000004	22	00	00	00
03000008	23	00	00	00
0300000C	24	00	00	00
03000010	25	00	00	00
03000014	26	00	00	00
03000018	28	00	00	00
0300001C	2A	00	00	00
03000020	2B	00	00	00
03000024	2C	00	00	00
03000028	2D	00	00	00
0300002C	30	00	00	00

Address	Data			
030008C0	10	00	00	00
030008C4	11	00	00	00
030008C8	12	00	00	00
030008CC	13	00	00	00
030008D0	14	00	00	00
030008D4	15	00	00	00
030008D8	16	00	00	00
030008DC	1A	00	00	00
030008E0	1B	00	00	00
030008E4	1C	00	00	00
030008E8	10	00	00	00
030008EC	12	00	00	00

Q.3 Assume that four 8K ROM is available. Write address range of 32K ROM for 80286 processor with starting address 020000_H **5M**

Q.4 Design an 8088 based system that has the following memory requirements: **10M**

8K of ROM from 02000_H

4K of RAM from 00000_H

Chip available are: 2716 and 6116 and LS138.

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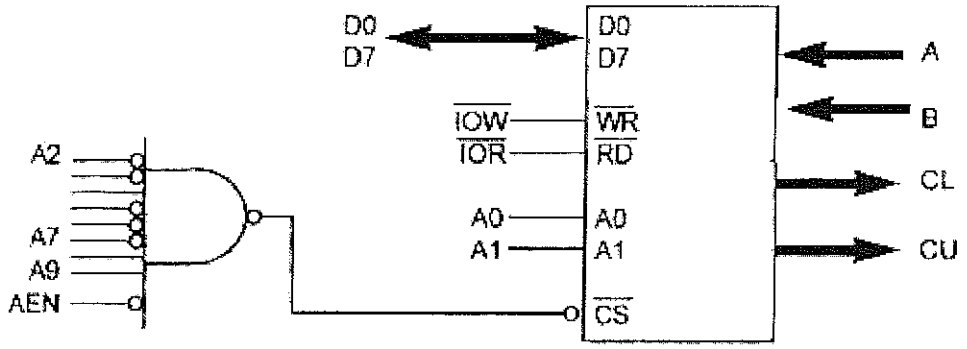
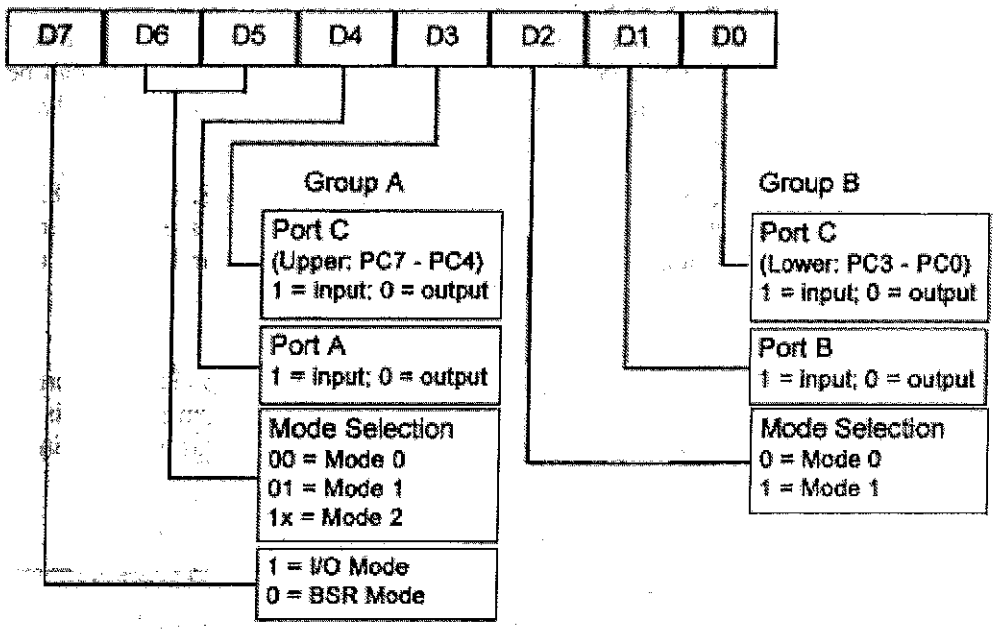
PART C

Q.1	(a) The 8255 shown in following figure is configured as follows: port A as input, B as output, and all the bits of port C as output.(a) Find the port addresses assigned to A, B, C, and the control register. Assign 0's for those address lines which are not mentioned in circuit. (b) Find the control word for this configuration.	5M
	(b) Design BCD adder using this configuration. Read BCD from Port A and Port B Assume higher nibble of Port A and Port B are zero. Use Port C for displaying result in 7 segment display. This addition process should take place continuously. Assume address of PORT A is 00H, PORT B is 02H , PORT C is 04H and control word is 06H.Draw block diagram for this interfacing	10M





8255 Control Word Format (I/O Mode)

Q.2	A weather monitoring system has the following specifications: 1) The weather has to be to monitored regular at intervals of 10 minutes. 2) There are inputs from 12 analog sensors. 3) The digital value is represented with 8 bits. 4) You are given ADC 0808 IC with the following pin out: (ADC 0808 works at 1 MHz clock):	15M

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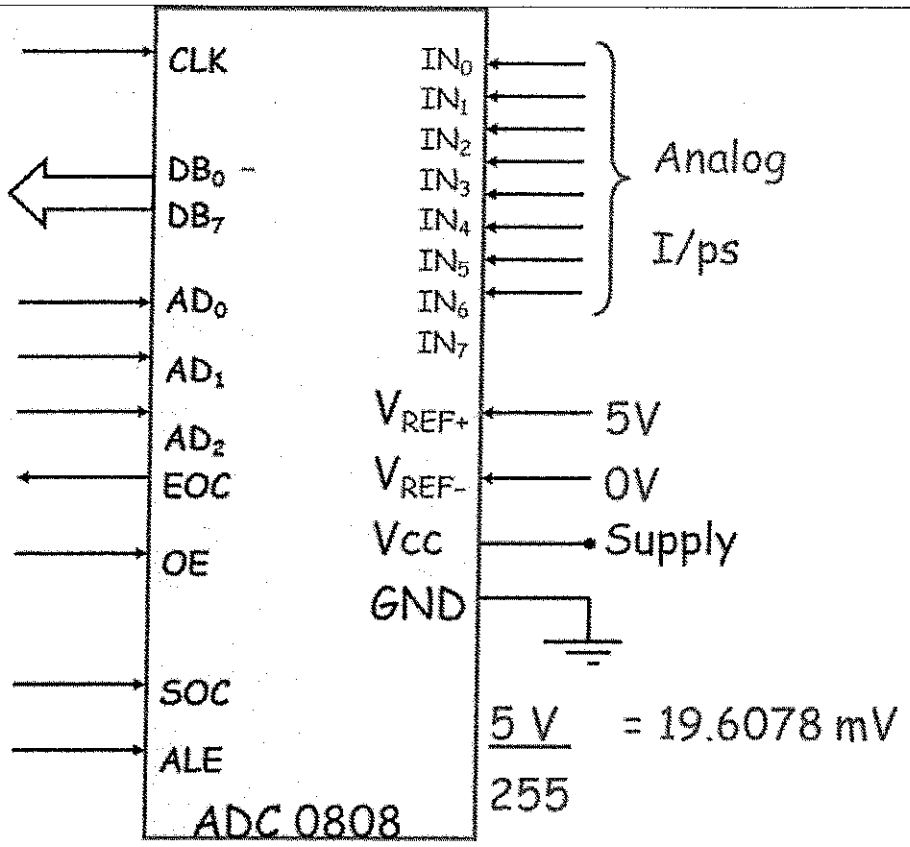

5) Design the requirements of 8254 and 8259 for the above 80x86 system.
5.1) You can assume that a 5 MHz clock is available.
5.2) Design the inputs, outputs. modes and counts required for 8254. Write the program for initializing the 8254. You are provided with the following.
Address of Counter 0 = 80H,90H
Address of Counter 1= 82H, 92H
Address of Counter 2= 84H , 94H
Address of Control register = 86H, 96H
5.3) Assume the following in designing 8259:

- round robin-fair priority on EOI
- starting vector addresses of 50H
- interrupt is edge triggered
- interrupt vector address of 60H

The design should include all control words. Write the program for initializing the 8259.
(Use the tables given below)

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Control Word Format

A_1,A_0 = 11 $\overline{CS}$ = 0 $\overline{RD}$ = 1 $\overline{WR}$ = 0

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 7. Control Word Format

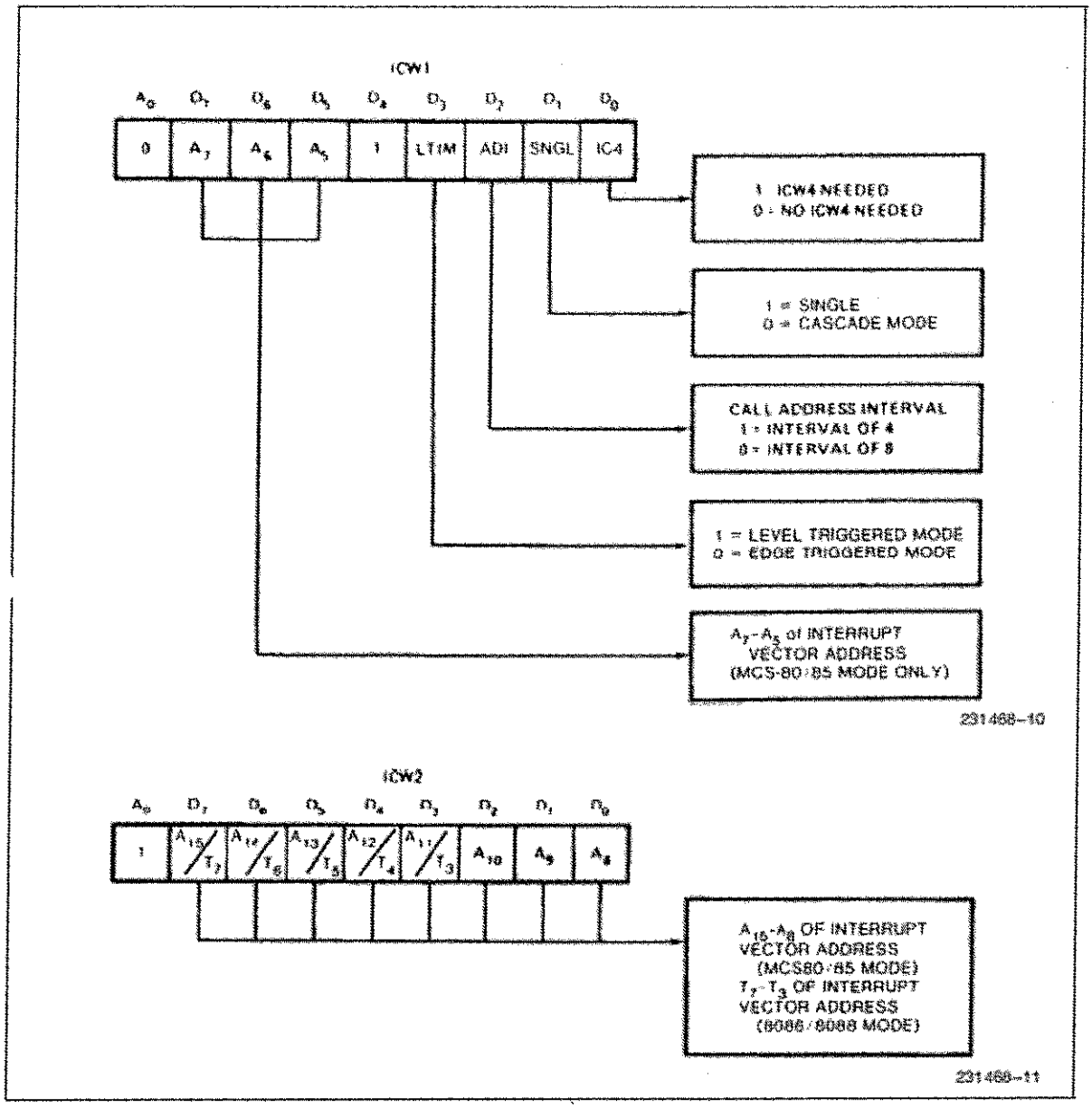
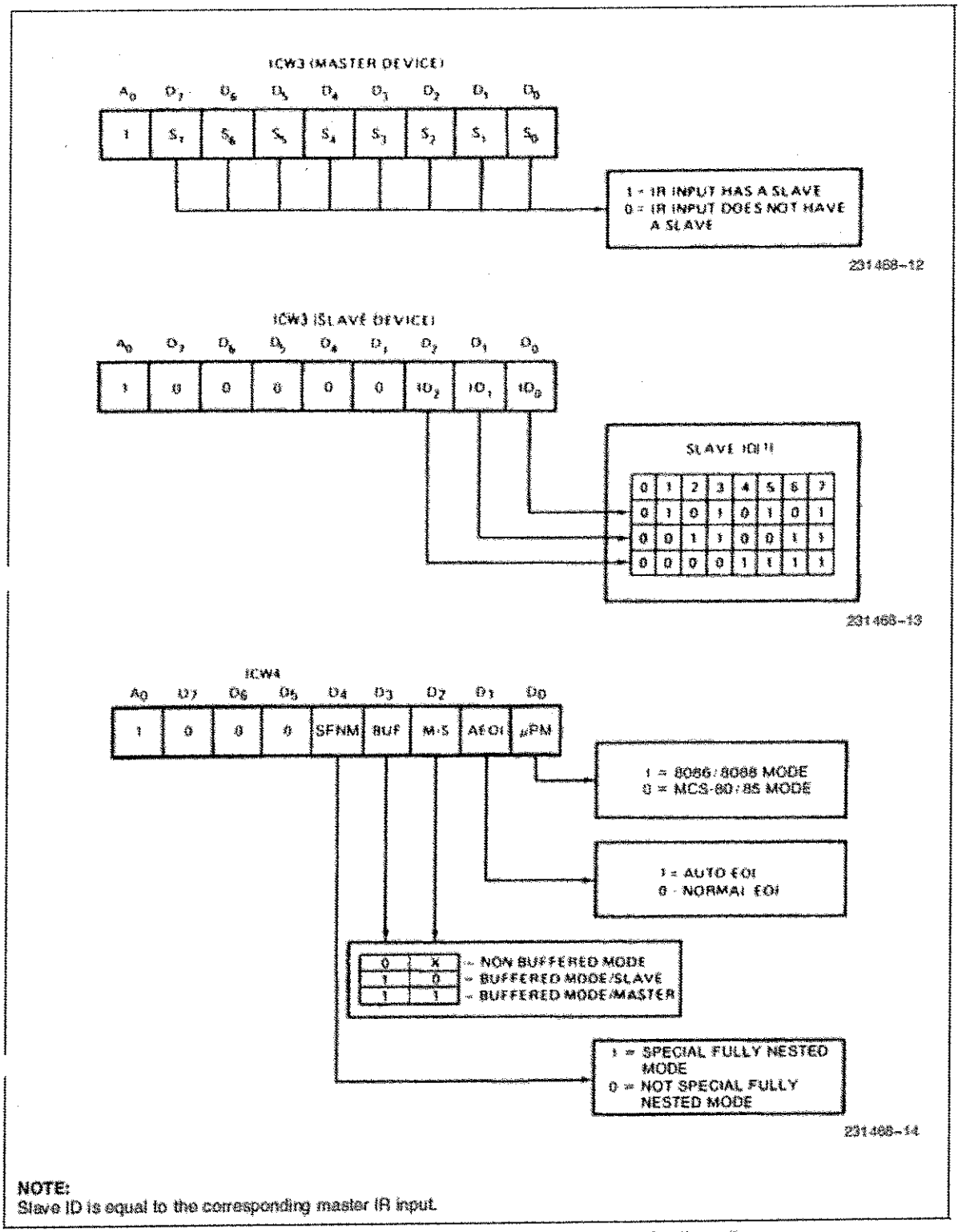


Figure 7. Initialization Command Word Format



NOTE:
Slave ID is equal to the corresponding master IR input.

Figure 7. Initialization Command Word Format (Continued)

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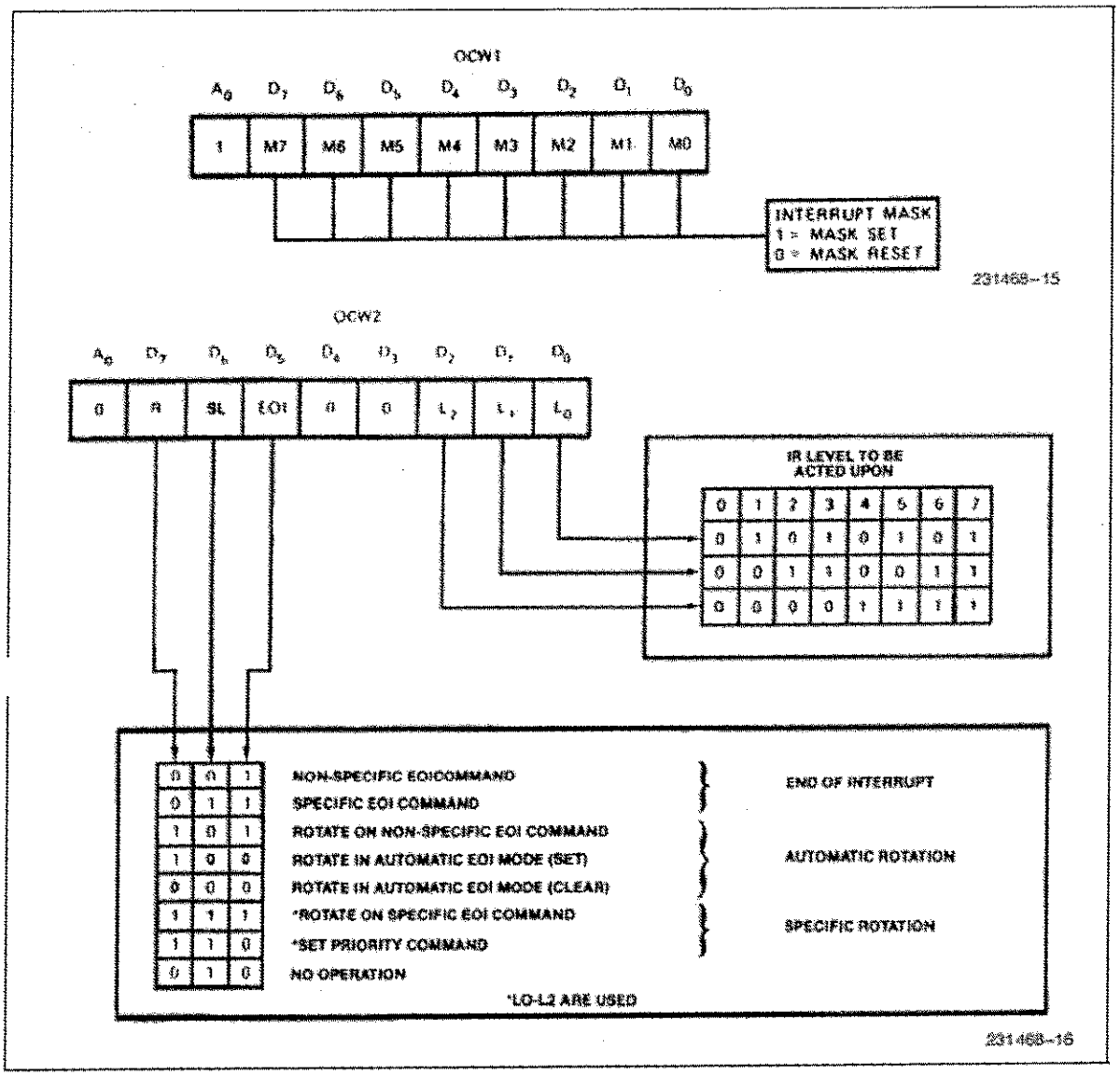

Figure 8. Operation Command Word Format

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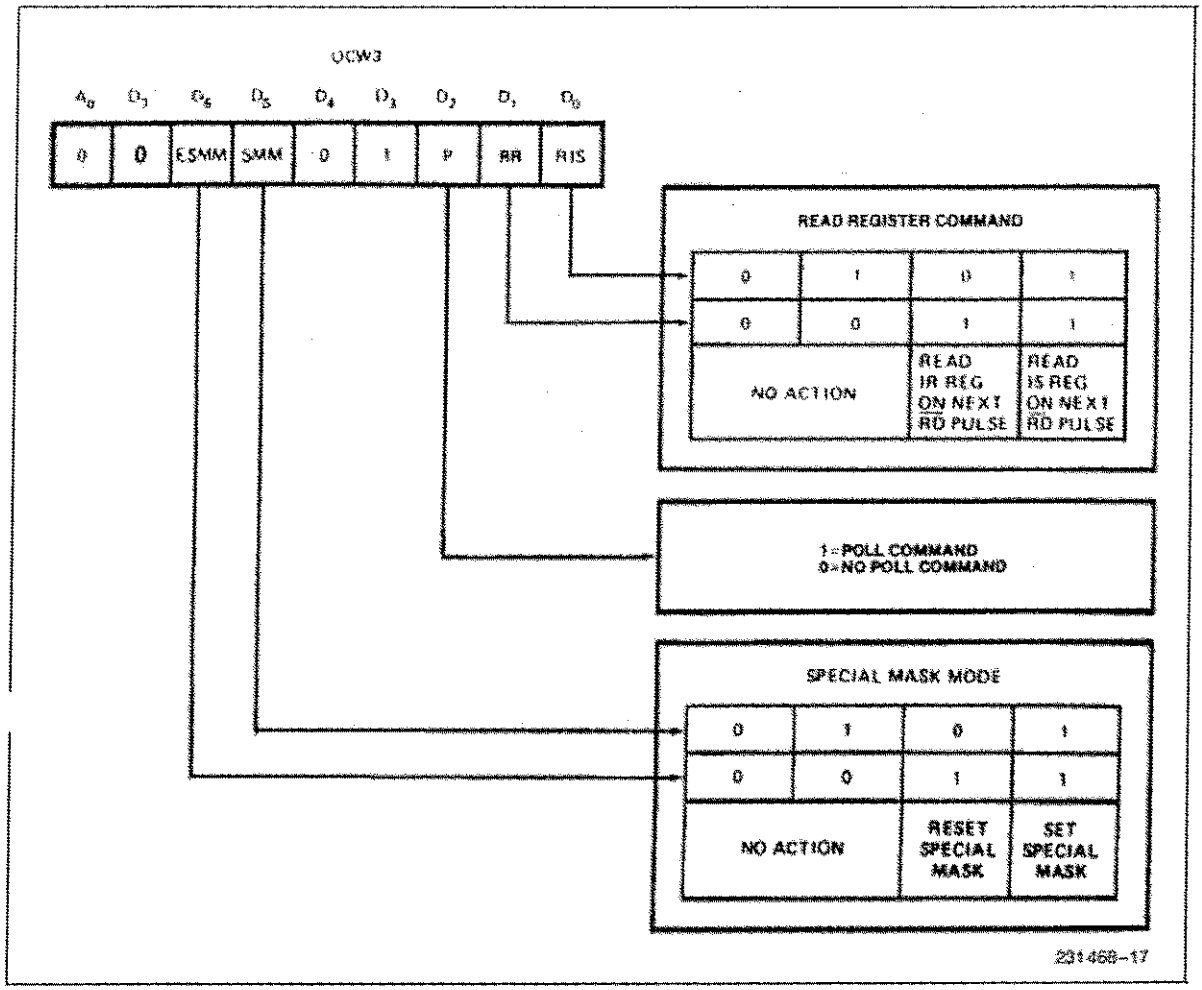

Figure 8. Operation Command Word Format (Continued)

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Tables for Part A Question No. 2 and 3

REG	
EAX/AX/AL	000
EBX/BX/BL	011
ECX/CX/CL	001
EDX/DX/DL	010
ESP/SP/AH	100
EBP/BP/CH	101
ESI/SI/DH	110
EDI/DI/BH	111

MOD / R/M	00	01	10	11	
				W = 0	W = 1
000	[BX] + [SI]	[BX]+[SI] +d8	[BX]+[SI]+d16	AL	AX
001	[BX] + [DI]	[BX]+[DI]+d8	[BX]+[DI]+d16	CL	CX
010	[BP] + [SI]	[BP]+[SI]+d8	[BP]+[SI]+d16	DL	DX
011	[BP] + [DI]	[BP]+[DI]+d8	[BP]+[DI]+d16	BL	BX
100	[SI]	[SI]+d8	[SI]+d16	AH	SP
101	[DI]	[DI]+d8	[DI]+d16	CH	BP
110	d16	[BP] + d8	[BP] + d16	DH	SI
111	[BX]	[BX]+d8	[BX]+d16	BH	DI

OPCODE FOR MOV INSTRUCTION = 1 0 0 0 1 0

MOD / R/M	00	01	10	11	
				W = 0	W = 1
000	EAX	EAX+d8	EAX+d32	AL	EAX
001	ECX	ECX+d8	ECX+d32	CL	ECX
010	EDX	EDX+d8	EDX+d32	DL	EDX
011	EBX	EBX+d8	EBX+d32	BL	EBX
100	Scaled Index	Scaled Index +d8	Scaled Index +d32	AH	ESP
101	d32	EBP+d8	EBP+d32	CH	EBP
110	ESI	ESI+d8	ESI+d32	DH	ESI
111	EDI	EDI+d8	EDI+d32	BH	EDI

D = 0 (Direction from Reg)
= 1 (Direction to Reg)

W = 0 (Data - byte)
= 1 (Data - word)

66h = operand size override
67h = address size override

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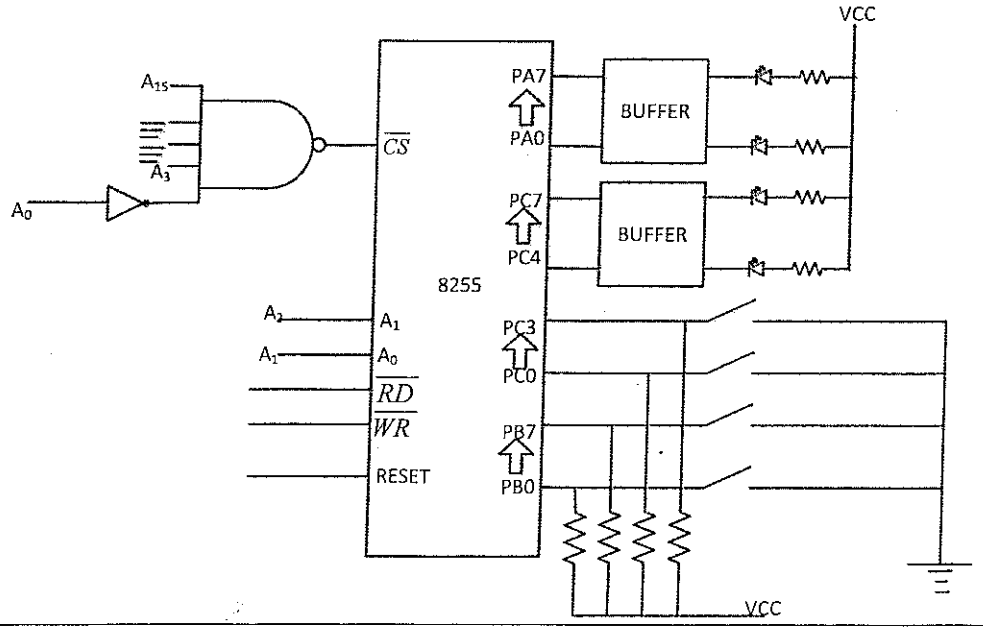
II SEM 2015-2016

Evaluation Component: TEST-2 (OPEN BOOK)	Date/Time/Duration: **27-APR-2016 / 08:30AM-09:20PM/20Mins**
Course No : **CS/ECE/EEE/INSTR F241**	Course Name : **MIRCOPROC & INTERFACING**
Maximum Marks : **45**	Weightage : **15%**

Note: Answer all the questions and any missing data can be assumed suitably

Q.1	a) Design an 8086 based system that has the following memory requirements: 8K of ROM from 00000_H 12K of RAM from 04000_H Chip available are: 2716 and 6116 and 2-LS138. b) Assume that four 4K ROM is available. Write address range of 16K ROM for 80286 processor with starting address 080000	**10+5= 15M**

Q.2	a) Write the steps on the interrupt of type *n* or software instruction INT *n* in 80x86. At what address CS *50* and IP *50* are stored in memory?
	b) Which interrupts are generally used for critical events? List out some critical events.
	c) Display the result in terms of interrupt for the following program
	MOV Ax,05
	MOV Dx, 03
	MOV Bx, 03
	SUB Bx, Dx
	DIV Bx
		2.5+1.5+1 =5M

Q.3	Figure shows an 8255A interfaced with 8086 microprocessor. Perform the following- (a) Identify the Port Address. (b) Identify the Mode 0 control word to configure Port A and Port C_U as output ports and Port B and Port C_L as input ports. (c) Write a program to read the DIP switches and display the reading from Port B at Port A, and from Port C_L at Port C_U. 	**2+3+5= 10M**

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Q.4	Interface 8253 with following specifications Addresses A1 and A2 of 8086 acts as A0 and A1 of 8253. Counter0 has address 7430. Clock frequency is 2 MHz. Generate squarewave of 1 KHz at counter 0, output of Counter 0 is fed as clock for counter1. Generate an interrupt on terminal count at counter1 for every 100ms. Write a program for above requirements.	**5M**
Q.5	The timer 8254 (operating @ 8MHz) is used to generate interrupt requests at a rate of 500 pulses/sec at IR2 input of 8259 PIC. The Interrupt is edge triggered and the vector number associated with IR2 is 40H and only IR2 should be enabled. There is only one 8259 in the system. Give the required command words and program for initializing the 8254 and 8259. (Use automatic EOI).	**10M**

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