BITS PILANI DUBAI CAMPUS

DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI UAE
II SEM 2017-2018

BITS Pilani
Dubai Campus

Evaluation Component: Comprehensive Examination (Closed Book)	Date/Time/Duration: 31 – MAY - 2018, Thursday 12:30PM to 03:30PM **03 Hours**
Course No : **CS/ECE/EEE/INSTR F241**	Course Name : **MIRCOPROC & INTERFACING**
Maximum Marks : **60**	Weightage : **30%**

Note: *Answer all the questions and any missing data can be assumed suitably*
*Answer **PART A and PART B in a separate answer Book***

PART A

Q1	Write the machine code for the following instructions. Assume instructions are in 16 bit mode of operation. a. MOV BX, AX b. MOV EAX, [2000H]	2x2=4M
Q2	Convert the following machine code into assembly code, assuming 16 bit mode of operation a. 66B96A001122 b. 2E8B851234	2x2=4M
Q3	Data-1 is stored in memory location C000H to C00FH and Data-2 is stored from A000H to A00FH. Write an ALP to swap Data-1 and Data-2.	5M
Q4	Suppose that in 8086 DS = 1400H, BP = 0200H, SS =2000H ,SI = 0300H. Determine the address accessed by each of the following instructions. a. MOV AX,[BP+100H] b. MOV AL,[BP+SI-200H]	1x2=2M
Q5	If an 8086 processor is working at 5MHz clock frequency. How much time does 1 MEMW cycle will take if there is 3 wait state?	1M
Q6	Find the number of machine cycle, the T- states and the total time required for executing the following instructions (Assume the processor is 8086 with 800 kHz clock input) I. MOV AX,[BX+1230H] (32-bit Machine code) II. MOV 2341[ECX], EBX (48-bit Machine code) III. MOV BX, [AX+SI+1000H] (32-bit Machine code) IV. MOV AX, ES:[DI+3700H] (40-bit machine code)	7M

Q7	For 80286 processor, DS = 0032H, GDTR = 100008H, EBX = 000031A0H, SI=0023H and the instruction to be executed is MOV AX, [1600H+BX+SI]. The following table is given	7M

A. What is the size of the segment?
B. Is this a code or data segment?
C. Is this segment Read only/execute only /, Read or Write?
D. Has this segment been accessed before?
E. What is the starting address of the segment?
F. What is the minimum RPL required to access this segment?
G. Physical address

GDT

Address	Data							
100008	00	00	82	01	00	00	FF	FF
100010	00	00	82	20	00	00	FF	FF
100018	00	00	83	03	00	00	00	3F
100020	00	00	FC	0A	00	00	00	1F
100028	00	00	DF	B0	00	00	01	FF
100030	00	00	92	B1	00	00	0F	FF
100038	00	00	B2	7B	00	00	03	FF
100040	00	00	D2	7A	00	00	07	FF
100048	00	00	9F	A1	00	00	1F	FF
100050	00	00	C4	A3	00	00	3F	FF
100058	00	00	82	B1	00	00	FF	FF
100060	00	00	B3	50	00	00	1F	FF

P	DPL	DPL	S	E	ED/C	R/W	A

E	ED/C	R/W	?
0	0	0	Data- Expands Upward – Read Only
0	0	1	Data- Expands Upward - Write
0	1	0	Data - Expand Downward – Read Only
0	1	1	Data- Expand Downward - Write
1	0	0	Code – Ignore DPL – Execute Only
1	0	1	Code – Ignore DPL – Read allowed
1	1	0	Code – Abide DPL – Execute Only
1	1	1	Code – Abide DPL – Read allowed

PART B

Q1	Write the address space of each of the Chips in an 8086 processor, which has 40K of memory requirements. Out of this 16K is ROM with a final address of 23FFFH and rest are RAM with a final address of 55FFFH. Chips available: 27032. 61032.	5M
Q2	80286-based system is having a memory requirement of 512K. Out of this 192K of RAM and rest is ROM. The mapping is as follows RAM with starting address 000000H ROM with starting address 040000H Chips available: 27256. 61256. LS138. Design the memory interfacing circuit. Use absolute addressing.	10M
Q3	Interface an 8255 with 8086 at 80H as an I/O address of Port A. Interface five 7 segment displays with the 8255. Write an ALP to display 1, 2, 3, 4 and 5 over the 5 displays continuously as per their positions starting with 1 at the least significant position? (Draw schematic diagram)	10M
Q4	Interface 8253 PIT with Microprocessor 8086, and write an assembly language program to generate buzzer tone of 4 kHz. The system clock available is 2 MHz. Assume 0000H as counter 0 port address.	5M

8253/8254 Contro, word format

Control Word Format

$A_1, A_0 = 11$ $\overline{CS} = 0$ $\overline{RD} = 1$ $\overline{WR} = 0$

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RW1	RW0	M2	M1	M0	BCD

SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write

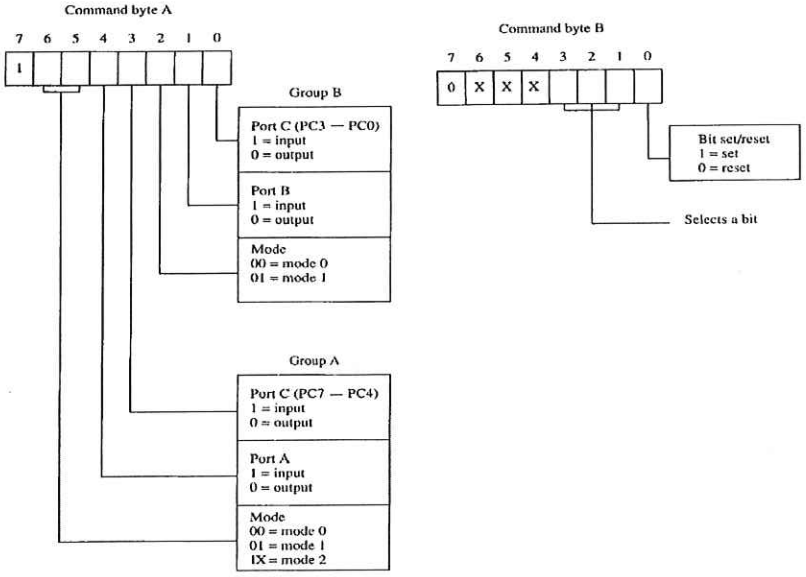
RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE:
Don't care bits (X) should be 0 to insure compatibility with future Intel products.

8255 Control word format



Tables for PART A Question No.1&2

REG	
EAX/AX/AL	000
EBX/BX/BL	011
ECX/CX/CL	001
EDX/DX/DL	010
ESP/SP/AH	100
EBP/BP/CH	101
ESI/SI/DH	110
EDI/DI/BH	111

MOD / R/M	00	01	10	11	
				W = 0	W = 1
000	[BX] + [SI]	[BX]+[SI] +d8	[BX]+[SI]+d16	AL	AX
001	[BX] + [DI]	[BX]+[DI]+d8	[BX]+[DI]+d16	CL	CX
010	[BP] + [SI]	[BP]+[SI]+d8	[BP]+[SI]+d16	DL	DX
011	[BP] + [DI]	[BP]+[DI]+d8	[BP]+[DI]+d16	BL	BX
100	[SI]	[SI]+d8	[SI]+d16	AH	SP
101	[DI]	[DI]+d8	[DI]+d16	CH	BP
110	d16	[BP] + d8	[BP] + d16	DH	SI
111	[BX]	[BX]+d8	[BX]+d16	BH	DI

MOD / R/M	00	01	10	11	
				W = 0	W = 1
000	EAX	EAX+d8	EAX+d32	AL	EAX
001	ECX	ECX+d8	ECX+d32	CL	ECX
010	EDX	EDX+d8	EDX+d32	DL	EDX
011	EBX	EBX+d8	EBX+d32	BL	EBX
100	Scaled Index	Scaled Index +d8	Scaled Index +d32	AH	ESP
101	d32	EBP+d8	EBP+d32	CH	EBP
110	ESI	ESI+d8	ESI+d32	DH	ESI
111	EDI	EDI+d8	EDI+d32	BH	EDI

66h = operand size override
67h = address size override

```
2EH     CS segment override prefix
36H     SS segment override prefix
3EH     DS segment override prefix
26H     ES segment override prefix
64H     FS segment override prefix
65H     GS segment override prefix
66H     Operand-size override
67H     Address-size override
 MOV Instruction opcode = 100010
```

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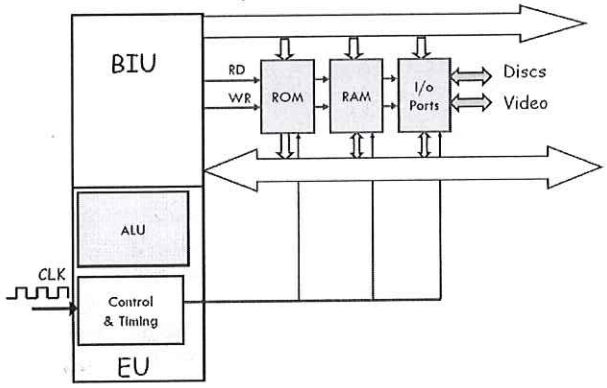
Evaluation Component: QUIZ-1	Date/Time/Duration: 11-FEB-2018, Sunday 03:00PM to 03:20PM **20 Minutes**
Course No : **CS/ECE/EEE/INSTR F241**	Course Name : **MIRCOPROC & INTERFACING**
Maximum Marks : **16**	Weightage : **08%**

Note: Answer all the questions and any missing data can be assumed suitably

ID.No.	**Name:**	**Faculty:**

Q.1	Instruction "ADD A, M1" , where A is register and M1 is memory belongs to what kind of processor (CISC/RISC) _____. Ans : _____	1M
Q.2	A Microprocessor supports upto 1MB of memory .The size of the address bus is Ans:_____	1M
Q.3	8088 microprocessor has (Tick the correct answer) (A) 16 bit data bus (B) 6 byte Instruction queue (C) 16 bit address bus (D) None of the Above	1M
Q.4	8086 has 20 address line so it is a 20 bit processor (Ture/False). _____	1M
Q.5	BIOS program is Residing in _____ of the Microcomputer system A. RAM B. ROM C. Hard disk D. None of the above	1M
Q.6	Separate the following registers as 8bit, 16 bit or 32 bit registers: AX, AH, EAX, BH, IP, EBX Ans:	3M

8 Bit	16 Bit	32 Bit

Q.7	The contents of the following registers are: CS = 9113 H, SS = 6928 H, IP = 4262 H, SP = 3105 H. Calculate the corresponding physical addresses for the address bytes in CS and SS using the default combination of Segment and displacement Registers. Ans : Physical Address for code : _____ Physical Address for Stack : _____	4M
Q.8	Following is a block diagram of a Microprocessor system, Identify the two types of buses and write your answer on the buses part shown.  	2M
Q.9	Physical address generated by the 8086 Microprocessor to fetch an instruction in real mode of operations is 30FFC, given that CS content is 2100 , calculate the content of the IP register (Show the steps in your answer) Ans : IP = _____	2M

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Evaluation Component: TEST -1 (Closed Book)	Date/Time/Duration: 28 – FEB - 2018, Wednesday 08:30AM to 09:20AM **50 Minutes**
Course No : **CS/ECE/EEE/INSTR F241**	Course Name : **MIRCOPROC & INTERFACING**
Maximum Marks : **30**	Weightage : **15%**

Note: Answer all the questions and any missing data can be assumed suitably

Use appropriate tables given in page 2

Q.1 (3+4=7M)

For the following instructions determine the machine code. Assume instructions are in 16-bit mode of operation

i. **MOV [SI+40h],AX**
ii. **MOV EAX,[2000H]**

Q.2A (4M)

Convert the following machine code to assembly code, assuming 16 bit mode of operation

8A5C88

Q.2B (1x3=3M)

Identify which of the following instructions are illegal/allowed and explain in one sentence why the instruction is illegal/allowed?

i. **MOV [EBX], [2000H]**
ii. **MOV BL, [AX]**
iii. **MOV DS, CX**

Q.3A (3M)

In the following commands , which of the following flags get affected (Put the √ mark in the table in your answer book)

	OF	SF	CF	ZF
LEA				
CMP				
ROL				

Q.3B (5M)

What will be the value in AX register after executing the following 8086 ALP? Assume that DS and ES are set up appropriately to access the variable 'num1'.

```
.model small
.data
num1 dw 1234h,5678h,9ABCh,0DEF0h
.code
start : mov ax,@data
        mov ds,ax
        mov bx,01h
        mov si,06h
        mov ax,num1[bx+si-2]
        int 3
        end start
```

Q.4 (8M)

Two arrays of unsigned 8 -bit data numbers are stored from location *arr1* and *arr2*. Write a program that will add the contents of *arr1* with *arr2* and store the addition result including the carry in an unsigned 16-bit array *arr3*. The count of data in *arr1* and *arr2* is 5.

For e.g. if the data in arr1 is 45h, 82h, 91h, 73h, 13h
And the data in arr2 is 20h, 7fh, 33h, 8eh, 45h
The result in arr3 will be 0065h, 0101h, 00c4h, 0101h, 0058h

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Evaluation Component: TEST -2 (Open Book)	Date/Time/Duration: 12 – APR - 2018, Thursday 08:30AM to 09:20AM **50 Minutes**
Course No : **CS/ECE/EEE/INSTR F241**	Course Name : **MIRCOPROC & INTERFACING**
Maximum Marks : **40**	Weightage : **20%**

Note: Answer all the questions and any missing data can be assumed suitably

Q1	Write a program to read a string using DOS interrupts (**Use MACRO**), transfer the given string from source to destination (**Use string instructions**) and also display the destination string on the screen (**Use MACRO**).	8M
Q2	Design a memory system for the 8088 microprocessor consisting of: a) ROM section using 2732 chips for the addresses from 00000H-02FFFH b) RAM section using 4016 chips for the addresses from 03000H-03FFFH c) LS138 Using absolute addressing mode.	10M
Q3	Design a 128 KB of ROM interface to 8086 Microprocessor system starting from the address 30000H using 27C128 EPROM and minimum number of 74LS138, other gates. (Note Use absolute addressing)	15M
Q4	For an 80286 Processor that has 8MB of memory. 4MB of ROM with starting address 00 00 00H and 4MB of RAM with starting address 50 00 00H. You have RAM and ROM chips of 1MB. How many chips you need for RAM and ROM interfacing? Mention starting and end address of each chip.	7M