



BITS PILANI DUBAI CAMPUS

DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI UAE

II SEM 2020-2021

Evaluation Component: Compre Part-A	Date/Time/Duration: 50 Minutes
Course No : EEE /ECE/INSTR / CSE F241	Course Name : Microprocessor and Interfacing
Maximum Marks : 20	Weightage :

1. Answer all questions on A4 sheets with your name and ID No. entered at the top of each page
 2. For getting full credit, shows all steps in arriving at your final answer.
 3. You have a maximum of 5 minutes after the part-A to scan and upload the single PDF in the Google Classroom under corresponding Part-A. Late submissions will not be entertained.

Q.1	<p>For the following instructions determine the Machine code. Assume both 16 bit mode of operation and 32 bit mode of operation. (Refer to the opcode table if needed)</p> <ul style="list-style-type: none"> I. MOV BX,SS:[ECX+10H], II. ADC AL,[SI], 	[2x2]
Q.2	<p>Convert the instruction to assembly code. Assume instructions are in 16 bit mode of operation</p> <ul style="list-style-type: none"> I. 6766 8B8D0010H II. 035C23H 	[2x2]
Q.3	<p>I. Given that the bl register contains 'b', the effect of the following instruction on bl would be</p> <p>AND bl, 1101 1111</p> <p>II. What will be the value in AX when the control reached to label2? Assume that DS and ES are set up appropriately to access the variable 'array'.</p> <pre> array dw 7,6,5,4 count dw 4 . . xor ax,ax stc mov cx,count mov si,offset array label1: adc ax,word ptr [si] add si,2 loop label1 label2: </pre>	[2+2]



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Q.4	<p>For a subroutine executed using the following instructions and given equivalent machine code</p> <p>SUMS:</p> <table style="margin-left: 100px;"> <tr><td>PROC NEAR</td></tr> <tr><td>MOV CX,AD4C_H</td><td>MC:B94CAD</td></tr> <tr><td>ADD AX, [SI]</td><td>MC:0304</td></tr> <tr><td>RET</td><td>MC: C3</td></tr> </table> <p>Calculate the following in decimals</p> <p>a) Type and Number of machine cycles required for each instruction b) Total number of T states required (Assume no wait states) c) Total time required for a 8086 microprocessor with a clock frequency of 8MHz. Assume that DS is loaded with the correct segment address</p>	PROC NEAR	MOV CX,AD4C _H	MC:B94CAD	ADD AX, [SI]	MC:0304	RET	MC: C3	[3]
PROC NEAR									
MOV CX,AD4C _H	MC:B94CAD								
ADD AX, [SI]	MC:0304								
RET	MC: C3								
Q5	<p>Consider the following assembly language code with required number of T states</p> <pre> mov cx,10 ; 4 xor ax,ax ; 3 mov si,0 ; 4 label: mov stuff[si],ax ; 9+9+4=22 add si,3 ;4 shl ax ;2 inc ax ;2 loop label ;17 except for the last iteration which is 5 </pre> <p>Calculate the Total number of T states and time required (Nano seconds) to execute following code snippet in a 8086 microprocessor with a clock frequency of 8MHz. Assume that DS is loaded with the correct segment address, so that no segment overrides are required to access the array 'stuff'.</p>	[3]							



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Q6	<p>The instruction shown in bold in the program listing is the current instruction being executed. [2]</p> <p>Listing of the program code:</p> <pre> 1266:0033 EB02 JMP 0037 1266:0035 46 INC SI 1266:0036 47 INC DI 1266:0037 803C00 CMP BYTE PTR [SI],00 1266:003A 7505 JNZ 0041 1266:003C 803D00 CMP BYTE PTR [DI],00 1266:003F 7412 JZ 0053 1266:0041 8A04 MOV AL,[SI] 1266:0043 3A05 CMP AL,[DI] 1266:0045 74EE JZ 0035 1266:0047 7305 JNB 004E 1266:0049 B8FFFF MOV AX,FFFF 1266:004C EB07 JMP 0055 1266:004E B80100 MOV AX,0001 1266:0051 EB02 JMP 0055 1266:0053 33C0 XOR AX,AX 1266:0055 C3 RET </pre> <p>While this instruction is executing, an NMI occurs. The NMI will be serviced before the next instruction begins executing. What is the address of the NMI interrupt service routine? The IVT is as follows</p> <p>Interrupt Vector Table:</p> <p>Dump of Interrupt Vector Table:</p> <pre> 0000:0000 BB 08 0B 02 65 04 70 00-16 05 DA 09 65 04 70 00e.p....e.p. 0000:0010 65 04 70 00 D7 04 00 C0-85 98 00 F0 53 FF 00 F0 e.p.....S... 0000:0020 00 00 00 C9 28 00 DA 05-3A 00 DA 05 52 00 DA 05(.....R... 0000:0030 6A 00 DA 05 82 00 DA 05-9A 00 DA 05 65 04 70 00 j.....e.p. </pre>
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MOD R/M	00	01	10	11	
				W = 0	W = 1
000	[BX] + [SI]	[BX]+[SI]+d8	[BX]+[SI]+d16	AL	AX
001	[BX] + [DI]	[BX]+[DI]+d8	[BX]+[DI]+d16	CL	CX
010	[BP] + [SI]	[BP]+[SI]+d8	[BP]+[SI]+d16	DL	DX
011	[BP] + [DI]	[BP]+[DI]+d8	[BP]+[DI]+d16	BL	BX
100	[SI]	[SI]+d8	[SI]+d16	AH	SP
101	[DI]	[DI]+d8	[DI]+d16	CH	BP
110	d16	[BP] + d8	[BP] + d16	DH	SI
111	[BX]	[BX]+d8	[BX]+d16	BH	DI

MOD R/M	00	01	10	11	
				W = 0	W = 1
000	EAX	EAX+d8	EAX+d32	AL	EAX
001	ECX	ECX+d8	ECX+d32	CL	ECX
010	EDX	EDX+d8	EDX+d32	DL	EDX
011	EBX	EBX+d8	EBX+d32	BL	EBX
100	Scaled Index	Scaled Index +d8	Scaled Index +d32	AH	ESP
101	d32	EBP+d8	EBP+d32	CH	EBP
110	ESI	ESI+d8	ESI+d32	DH	ESI
111	EDI	EDI+d8	EDI+d32	BH	EDI

EAX/AX/AL	000
EBX/BX/BL	011
ECX/CX/CL	001
EDX/DX/DL	010
ESP/SP/AH	100
EBP/BP/CH	101
ESI/SI/DH	110
EDI/DI/BH	111

REG

Segment	Prefix Value
ES	26 _H
CS	2E _H
SS	36 _H
DS	3E _H
FS	64 _H
GS	65 _H



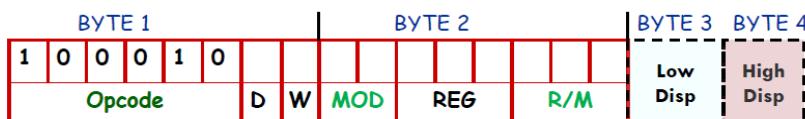
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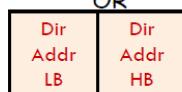
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OR



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Selected Instruction Formats

Instruction	Opcode	Addr.Mode
ADC reg/mem with reg	000100dw	modregr/m [addr]
ADC immed to reg/mem	100000sw	mod010r/m data
ADD reg/mem with reg	000000dw	modregr/m [addr]
ADD immed to accumulator	0000010w	data
ADD immed to reg/mem	100000sw	mod000r/m [addr] data
OR reg/mem with reg	000010dw	modregr/m
OR immed to reg/mem	100000sw	mod001r/m [addr] data
OR immed to accumlator	0000110w	data
INC reg16	01000reg	
INC reg/mem	1111111w	mod000r/m [addr]
MOV reg/mem to/from reg	100010dw	modregr/m [addr]
MOV reg/mem to segreg	10001110	modsegr/m (seg = segreg)
MOV immed to reg/mem	1100011w	mod000r/m [addr] data
MOV immed to reg	1011wreg	data
MOV direct mem to/from acc	101000dw	addr
XCHG reg/mem with reg	1000011w	modregr/m [addr]
XCHG reg16 with accum.	10010reg	



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ASCII - Hex - Binary Conversion Chart											
ASCII	Hex	Binary	ASCII	Hex	Binary	ASCII	Hex	Binary	ASCII	Hex	Binary
NUL	00	00000000	SP	20	00100000	@	40	01000000	`	60	01100000
SOH	01	00000001	!	21	00100001	A	41	01000001	a	61	01100001
STX	02	00000010	"	22	00100010	B	42	01000010	b	62	01100010
ETX	03	00000011	#	23	00100011	C	43	01000011	c	63	01100011
EOT	04	00000100	\$	24	00100100	D	44	01000100	d	64	01100100
ENQ	05	00000101	%	25	00100101	E	45	01000101	e	65	01100101
ACK	06	00000110	&	26	00100110	F	46	01000110	f	66	01100110
BEL	07	00000111	'	27	00100111	G	47	01000111	g	67	01100111
BS	08	00001000	(28	00101000	H	48	01001000	h	68	01101000
HT	09	00001001)	29	00101001	I	49	01001001	i	69	01101001
LF	0A	00001010	*	2A	00101010	J	4A	01001010	j	6A	01101010
VT	0B	00001011	+	2B	00101011	K	4B	01001011	k	6B	01101011
FF	0C	00001100	,	2C	00101100	L	4C	01001100	l	6C	01101100
CR	0D	00001101	-	2D	00101101	M	4D	01001101	m	6D	01101101
SO	0E	00001110	.	2E	00101110	N	4E	01001110	n	6E	01101110
SI	0F	00001111	/	2F	00101111	O	4F	01001111	o	6F	01101111
DLE	10	00010000	0	30	00110000	P	50	01010000	p	70	01110000
DC1	11	00010001	1	31	00110001	Q	51	01010001	q	71	01110001
DC2	12	00010010	2	32	00110010	R	52	01010010	r	72	01110010
DC3	13	00010011	3	33	00110011	S	53	01010011	s	73	01110011
DC4	14	00010100	4	34	00110100	T	54	01010100	t	74	01110100
NAK	15	00010101	5	35	00110101	U	55	01010101	u	75	01110101
SYN	16	00010110	6	36	00110110	V	56	01010110	v	76	01110110
ETB	17	00010111	7	37	00110111	W	57	01010111	w	77	01110111
CAN	18	00011000	8	38	00111000	X	58	01011000	x	78	01111000
EM	19	00011001	9	39	00111001	Y	59	01011001	y	79	01111001
SUB	1A	00011010	:	3A	00111010	Z	5A	01011010	z	7A	01111010
ESC	1B	00011011	;	3B	00111011	[5B	01011011	{	7B	01111011
FS	1C	00011100	<	3C	00111100	\	5C	01011100		7C	01111100
GS	1D	00011101	=	3D	00111101]	5D	01011101	}	7D	01111101
RS	1E	00011110	>	3E	00111110	^	5E	01011110	~	7E	01111110
US	1F	00011111	?	3F	00111111	_	5F	01011111	DEL	7F	01111111



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Q.1	<p>For the following instructions determine the Machine code. Assume both 16 bit mode of operation and 32 bit mode of operation. (Refer to the opcode table if needed)</p> <p>I. ADD [BX+SI+1234_H],CX, II. XCHG AX,[BX],</p>	[2x2]
Q.2	<p>Convert the instruction to assembly code. Assume instructions are in 16 bit mode of operation</p> <p>I. 67 8B5F12_H II. 138D3412_H</p>	[2x2]
Q.3	<p>I. Given that the bl register contains 'B', the effect of the following instruction on bl would be OR bl, 0010 0000</p> <p>II. Number of the times the instruction sequence below will loop before coming out of the loop is MOV AL, 00h A1: INC AL JNZ A1</p>	[2+2]
Q.4	<p>The following hypothetical program runs in 8086 processor with the given equivalent machine code</p> <p>MOV CX,100 MC: B90001 X1 MOV BL,[SI] MC: 8A1C CALL Mask MC: E8 DEC CX MC:49 JNZ X1 MC:75F7</p> <p>Calculate the following in decimals</p> <p>a) Type and Number of machine cycles required for each instruction b) Total number of T states required (Assume no wait states)</p>	[3]



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	c) Total time required for a 8086 microprocessor with a clock frequency of 8MHz. Assume that DS is loaded with the correct segment address.	
Q.5	<p>Consider the following assembly language code with required number of T states</p> <pre>mov cx,10 ; 4 xor ax,ax ; 3 mov si,0 ; 4 label: mov stuff[si],ax ; 9+9+4 add si,3 ;4 shl ax ;2 inc ax ;2 loop label ;17 except for the last iteration which is 5</pre> <p>Calculate the Total number of T states and time required (Nano seconds) to execute following code snippet in a 8086 microprocessor with a clock frequency of 8MHz. Assume that DS is loaded with the correct segment address, so that no segment overrides are required to access the array 'stuff'.</p>	[3]



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				W = 0	W = 1
000	[BX] + [SI]	[BX]+[SI]+d8	[BX]+[SI]+d16	AL	AX
001	[BX] + [DI]	[BX]+[DI]+d8	[BX]+[DI]+d16	CL	CX
010	[BP] + [SI]	[BP]+[SI]+d8	[BP]+[SI]+d16	DL	DX
011	[BP] + [DI]	[BP]+[DI]+d8	[BP]+[DI]+d16	BL	BX
100	[SI]	[SI]+d8	[SI]+d16	AH	SP
101	[DI]	[DI]+d8	[DI]+d16	CH	BP
110	d16	[BP] + d8	[BP] + d16	DH	SI
111	[BX]	[BX]+d8	[BX]+d16	BH	DI

MOD R/M	00	01	10	11	
				W = 0	W = 1
000	EAX	EAX+d8	EAX+d32	AL	EAX
001	ECX	ECX+d8	ECX+d32	CL	ECX
010	EDX	EDX+d8	EDX+d32	DL	EDX
011	EBX	EBX+d8	EBX+d32	BL	EBX
100	Scaled Index	Scaled Index +d8	Scaled Index +d32	AH	ESP
101	d32	EBP+d8	EBP+d32	CH	EBP
110	ESI	ESI+d8	ESI+d32	DH	ESI
111	EDI	EDI+d8	EDI+d32	BH	EDI

EAX/AX/AL	000
EBX/BX/BL	011
ECX/CX/CL	001
EDX/DX/DL	010
ESP/SP/AH	100
EBP/BP/CH	101
ESI/SI/DH	110
EDI/DI/BH	111

REG

Segment	Prefix Value
ES	26 _H
CS	2E _H
SS	36 _H
DS	3E _H
FS	64 _H
GS	65 _H



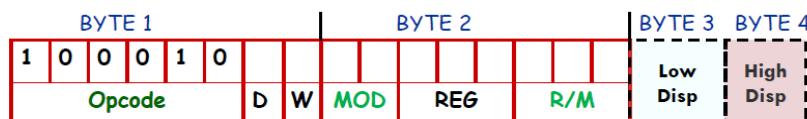
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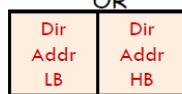
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Selected Instruction Formats

Instruction	Opcode	Addr.Mode
ADC reg/mem with reg	000100dw	modregr/m [addr]
ADC immed to reg/mem	100000sw	mod010r/m data
ADD reg/mem with reg	000000dw	modregr/m [addr]
ADD immed to accumulator	0000010w	data
ADD immed to reg/mem	100000sw	mod000r/m [addr] data
OR reg/mem with reg	000010dw	modregr/m
OR immed to reg/mem	100000sw	mod001r/m [addr] data
OR immed to accumlator	0000110w	data
INC reg16	01000reg	
INC reg/mem	1111111w	mod000r/m [addr]
MOV reg/mem to/from reg	100010dw	modregr/m [addr]
MOV reg/mem to segreg	10001110	modsegr/m (seg = segreg)
MOV immed to reg/mem	1100011w	mod000r/m [addr] data
MOV immed to reg	1011wreg	data
MOV direct mem to/from acc	101000dw	addr
XCHG reg/mem with reg	1000011w	modregr/m [addr]
XCHG reg16 with accum.	10010reg	



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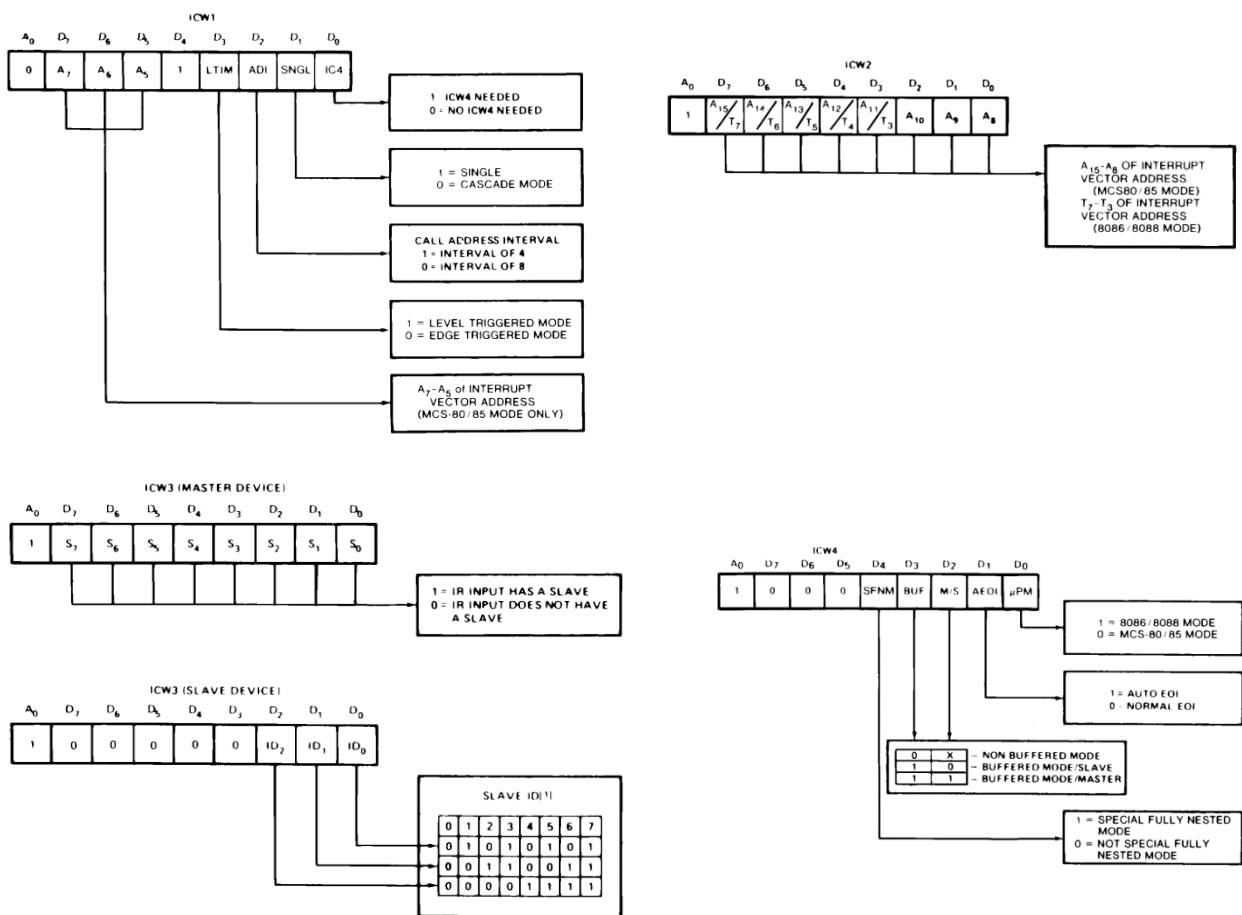
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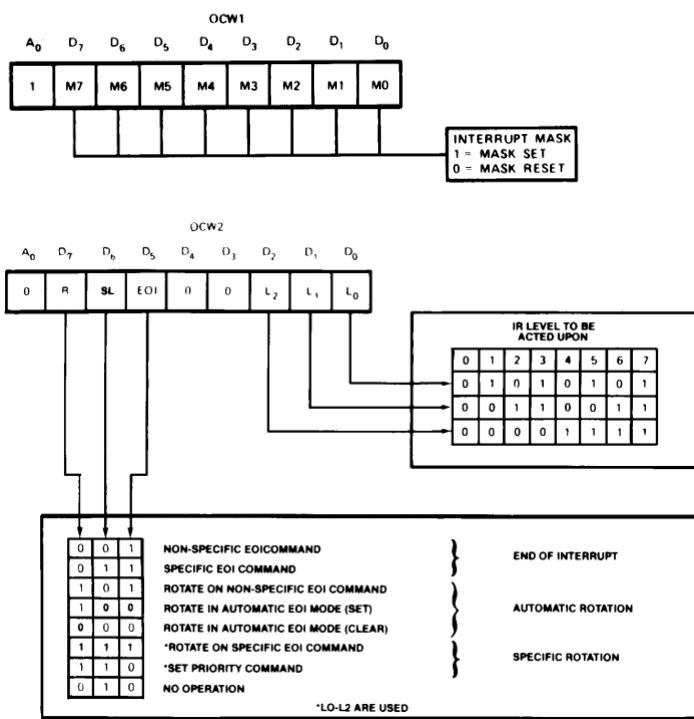
ASCII - Hex - Binary Conversion Chart											
ASCII	Hex	Binary	ASCII	Hex	Binary	ASCII	Hex	Binary	ASCII	Hex	Binary
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SOH	01	00000001	!	21	00100001	A	41	01000001	a	61	01100001
STX	02	00000010	"	22	00100010	B	42	01000010	b	62	01100010
ETX	03	00000011	#	23	00100011	C	43	01000011	c	63	01100011
EOT	04	00000100	\$	24	00100100	D	44	01000100	d	64	01100100
ENQ	05	00000101	%	25	00100101	E	45	01000101	e	65	01100101
ACK	06	00000110	&	26	00100110	F	46	01000110	f	66	01100110
BEL	07	00000111	'	27	00100111	G	47	01000111	g	67	01100111
BS	08	00001000	(28	00101000	H	48	01001000	h	68	01101000
HT	09	00001001)	29	00101001	I	49	01001001	i	69	01101001
LF	0A	00001010	*	2A	00101010	J	4A	01001010	j	6A	01101010
VT	0B	00001011	+	2B	00101011	K	4B	01001011	k	6B	01101011
FF	0C	00001100	,	2C	00101100	L	4C	01001100	l	6C	01101100
CR	0D	00001101	-	2D	00101101	M	4D	01001101	m	6D	01101101
SO	0E	00001110	.	2E	00101110	N	4E	01001110	n	6E	01101110
SI	0F	00001111	/	2F	00101111	O	4F	01001111	o	6F	01101111
DLE	10	00010000	0	30	00110000	P	50	01010000	p	70	01110000
DC1	11	00010001	1	31	00110001	Q	51	01010001	q	71	01110001
DC2	12	00010010	2	32	00110010	R	52	01010010	r	72	01110010
DC3	13	00010011	3	33	00110011	S	53	01010011	s	73	01110011
DC4	14	00010100	4	34	00110100	T	54	01010100	t	74	01110100
NAK	15	00010101	5	35	00110101	U	55	01010101	u	75	01110101
SYN	16	00010110	6	36	00110110	V	56	01010110	v	76	01110110
ETB	17	00010111	7	37	00110111	W	57	01010111	w	77	01110111
CAN	18	00011000	8	38	00111000	X	58	01011000	x	78	01111000
EM	19	00011001	9	39	00111001	Y	59	01011001	y	79	01111001
SUB	1A	00011010	:	3A	00111010	Z	5A	01011010	z	7A	01111010
ESC	1B	00011011	;	3B	00111011	[5B	01011011	{	7B	01111011
FS	1C	00011100	<	3C	00111100	\	5C	01011100		7C	01111100
GS	1D	00011101	=	3D	00111101]	5D	01011101	}	7D	01111101
RS	1E	00011110	>	3E	00111110	^	5E	01011110	~	7E	01111110
US	1F	00011111	?	3F	00111111	_	5F	01011111	DEL	7F	01111111

Evaluation Component: Comprehensive Examination (Closed Book) PART-B	Date/Time/Duration 02-JUN-2021 WED 50Mins
Course No: CS/EEE/ECE/INST F241	Course Name: MICRO & INTERAFING
Maximum Marks : 20	

Q1	Design a 64KBytes of RAM and 128 Kbytes of ROM interface to an 8086-microprocessor system using address decoding Logic. Use 32Kbytes ROM and RAM Chips. Your address decoding logic should have only NAND, OR and NOT gates. The ROM address will start from D0000H and RAM address will start from F0000H. Show entire memory interface with proper labels. Use absolute addressing.	10M
Q2	Interface an 8259 PIC to the 8086 microprocessors with an address of 0A8x. Write an ALP to Initialize the 8259 in an edge triggered mode without any nested mode. The 8259 has to work in non-buffered. The IR5 is masked and IR2 being the bottom most priority level. The 8259 is not working in Automatic End of Interrupt Mode. Let vector address of IR0 is 80H.	10M

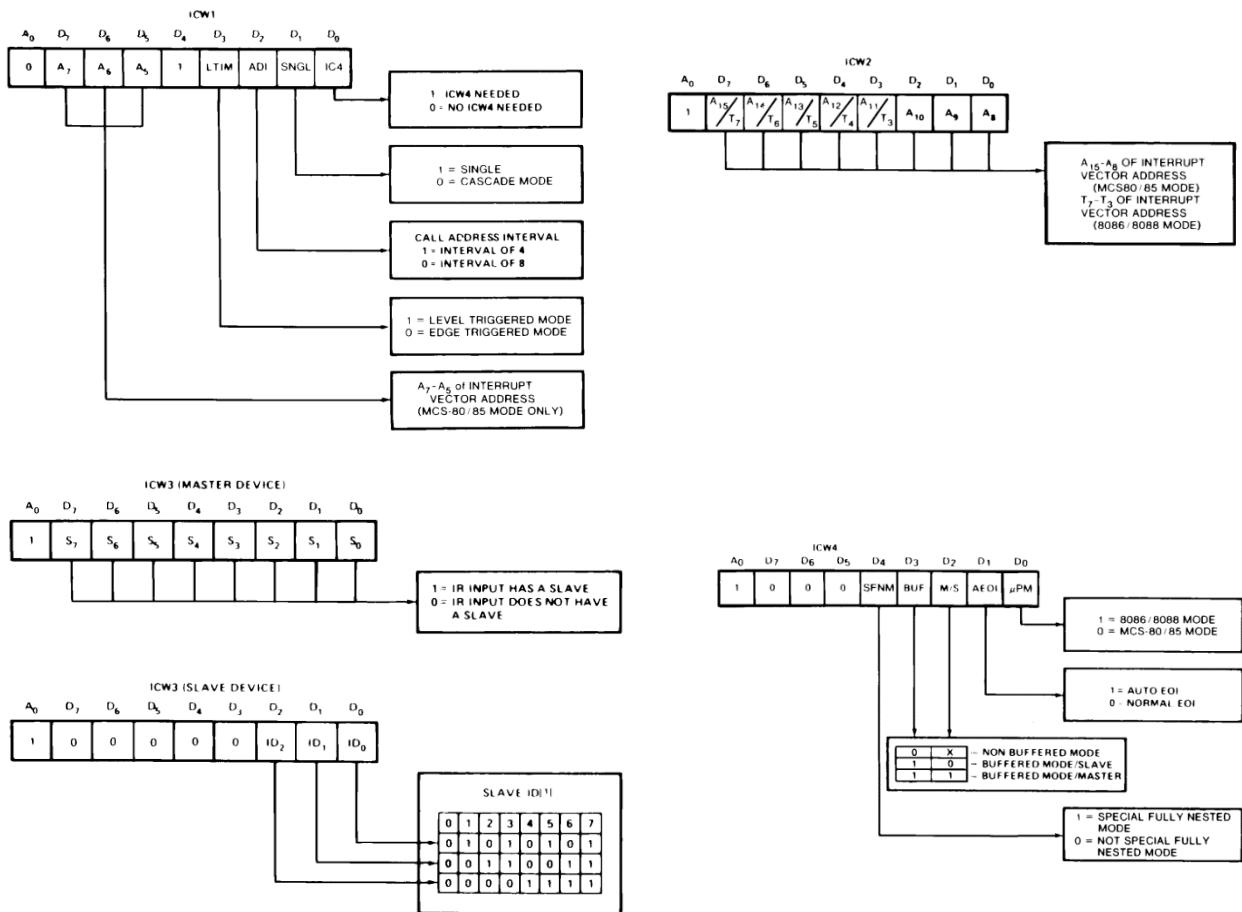


Evaluation Component: Comprehensive Examination (Closed Book) PART-B	Date/Time/Duration 02-JUN-2021 WED 50Mins
Course No: CS/EEE/ECE/INST F241	Course Name: MICRO & INTERAFCLNG
Maximum Marks : 20	

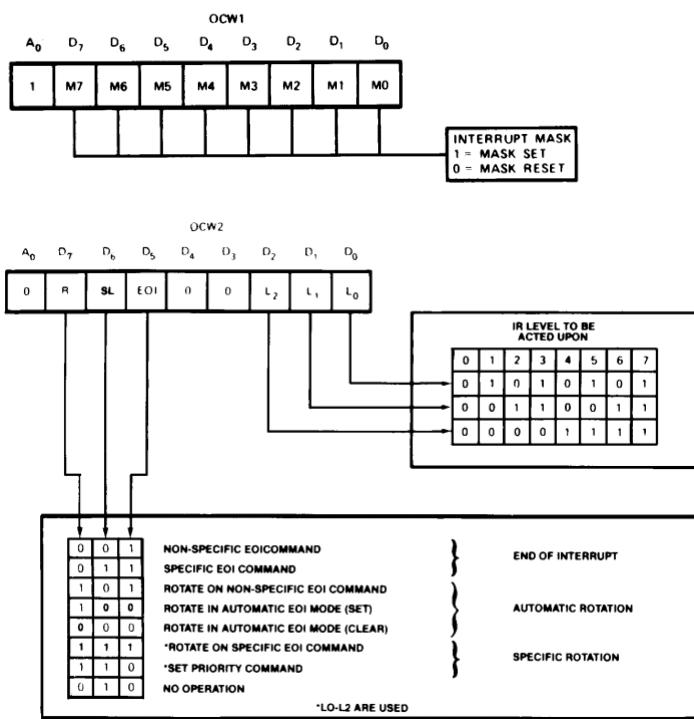


Evaluation Component: Comprehensive Examination (Closed Book) PART-B	Date/Time/Duration 02-JUN-2021 WED 50Mins
Course No: CS/EEE/ECE/INST F241	Course Name: MICRO & INTERAFING
Maximum Marks : 20	

Q1	Design a 32KBytes of RAM and 64 Kbytes of ROM interface to an 8086-microprocessor system using address decoding Logic. Use 32KBytes ROM and 16Kbytes RAM Chips. Your address decoding logic should have only NAND, OR and NOT gates. The ROM address will start from 00000H and RAM address will start from F8000H. Show entire memory interface with proper labels. Use absolute addressing.	10M
Q2	Interface an 8259 PIC to the 8086 microprocessors with an address of 096x. Write an ALP to Initialize the 8259 in a level triggered mode without any nested mode of operation. The 8259 has to work in buffered mode. The IR3 is masked and IR1 being the bottom most priority level. The 8259 is working in Automatic End of Interrupt Mode. Let vector address of IR0 is 90H.	10M



Evaluation Component: Comprehensive Examination (Closed Book) PART-B	Date/Time/Duration 02-JUN-2021 WED 50Mins
Course No: CS/EEE/ECE/INST F241	Course Name: MICRO & INTERAFING
Maximum Marks : 20	



BITS Pilani, Dubai Campus
Dubai International Academic City, Dubai.

SECOND SEMESTER: 2020 – 2021
COMPREHENSIVE EXAM – Part-C

Course Code:	EEE F241	Date:	02.06.2021
Course Title:	Microprocessor and Its Interfacing	Maximum Marks:	20
Duration:	50 min.		

1. Answer all questions on A4 sheets with your name and ID No. entered at the top of each page
 2. For getting full credit, shows all steps in arriving at your final answer.
 3. You have a maximum of 5 minutes after the part-C to scan and upload the single PDF in the Google Classroom under corresponding Part-C. Late submissions will not be entertained.
-

Q1: Design a 8086 based circuit using 8255 IC for the following requirement. **[10 Marks]**

You need to design 3x8 decoder with active low output. There are three switches to set the input of decoder and eight LEDs as output. **Example:** If switch-0, 1 and 2 are “000” then LED-0 should glow. If switch-0, 1 and 2 are “010” then LED-2 should glow and so on

Draw the block level circuit diagram and write the 8086 snippet code for the same.

8255 Control Word:

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1 - I/O Mode	Port A Mode 0 0 - Mode 0 0 1 - Mode 1 1 x - Mode2	Port A 1 - i/p 0 - o/p	Port C Upper 1 - i/p 0 - o/p	Port B Mode 0- Mode0 1- Mode1	Port B 1 - i/p 0 - o/p	Port C Lower 1 - i/p 0 - o/p	

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0 - BSR	x	x	x	Bit ₂	Bit ₁	Bit ₀	Bit Set/Reset
	Don't Care Condition			PC 0 1 2 3 4 5 6 7	B ₀ 0 1 0 1 0 1 0 1	B ₁ 0 0 1 1 0 0 1 1	B ₂ 0 0 0 0 1 1 1 1

1 - Set
0 - Reset

Q2: Design a 8086 based circuit using 8253 IC for the following requirements.

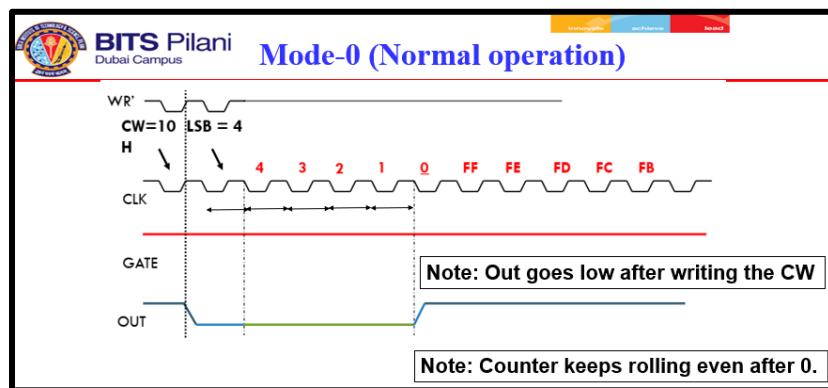
[10 Marks]

You need to generate the perfect square wave of 1 kHz from the Out pin of *counter-0* of 8253 which should run in **Mode-1**. Clock input pin of counter-0 is connected to 100 kHz signal. You can use other remaining counter(s) in any mode as per your requirement (to provide gate input to counter-0) with any frequency at their clock pin. You can use some minimum number of external logic gates if required. Ignore the time-period/frequency of out pins for initial few clock cycles.

Draw the block level circuit diagram and write the 8086 snippet code for the same.

8253 Control word

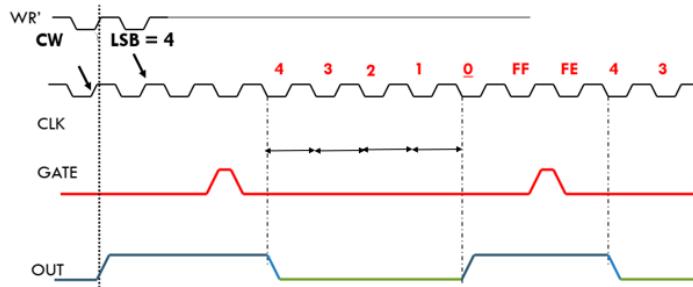
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
SC1	SC0	RW1	RW0	M2	M1	M0	BCD
Selects Counter		Read/Write Control		Timer Mode			
00	Counter 0	00	Latch Counter	000	Interrupt on T/C		0 – binary
01	Counter 1	01	R/W LSB	001	h/w re-Triggerable one shot		0000 _h
10	Counter 2	10	R/W MSB	010	rate generator		FFFF _h
11	Read Back Command	11	R/W LSB followed by MSB	011	Square wave generator		1 – BCD
				1x0	s/w triggered strobe		0000
				1x1	h/w triggered strobe		9999



P.T.O.



Mode-1 (Normal operation)

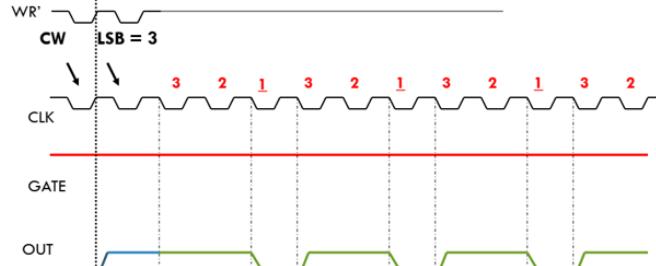


Note: Out goes high after writing the CW and goes zero after gate pulse till count reaches 0.

Note: Counter keeps rolling even after 0.



Mode-2 (Normal operation)

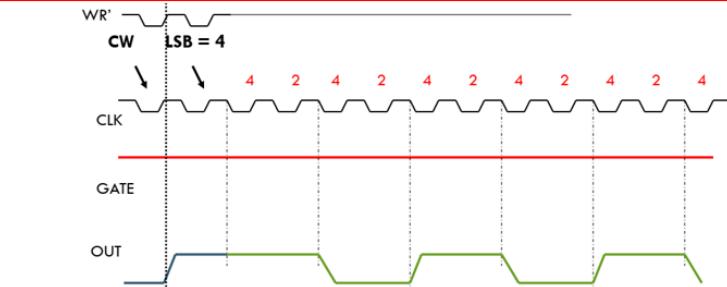


Note: Out goes high after writing the CW and goes zero when counter reaches '1'.

Note: Counter re-load the value and restart countdown.



Mode-3 (Normal operation, even value)



Note: Out goes high after writing the CW. Counter decrements by 2 and goes zero when counter reaches '1'.

Note: Counter reloads the value and restart countdown.

*****End of Part-C*****

*****Upload answers to this part under Part-C uP compre on google classroom*****

BITS Pilani, Dubai Campus
Dubai International Academic City, Dubai.

SECOND SEMESTER: 2020 – 2021
COMPREHENSIVE EXAM – Part-C

Course Code:	EEE F241	Date:	02.06.2021
Course Title:	Microprocessor and Its Interfacing	Maximum Marks:	20
Duration:	50 min.		

1. Answer all questions on A4 sheets with your name and ID No. entered at the top of each page
 2. For getting full credit, shows all steps in arriving at your final answer.
 3. You have a maximum of 5 minutes after the part-C to scan and upload the single PDF in the Google Classroom under corresponding Part-C. Late submissions will not be entertained.
-

Q1: Design a 8086 based circuit using 8255 IC for the following requirements. [10 Marks]

You need to design a 8x3 encoder with active high output. There are 8 switches to set the input of encoder and three LEDs as output. Only one switch at a time can be high. **Example:** If switch-0 is '1' and rest all are '0', then all three output LEDs should be OFF '000'. If switch-2 is '1' and rest all are '0', then LED should show '010'.

Draw the block level circuit diagram and write the 8086 snippet code for the same.

8255 Control Word:

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1 - I/O Mode	Port A Mode	Port A	Port C Upper	Port B Mode	Port B	Port C Lower	
0 0 - Mode 0	1 - i/p	0 - o/p	1 - i/p	0 - Mode0	1 - i/p	1 - i/p	
0 1 - Mode 1	0 - o/p		0 - o/p	1 - Mode1	0 - o/p	0 - o/p	
1 x - Mode2							

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0 -BSR	x	x	x	Bit ₂	Bit ₁	Bit ₀	Bit Set/Reset
	Don't Care Condition			PC	0 1 2 3 4 5 6 7	B ₀	1 - Set 0 - Reset
				B ₁	0 0 1 1 0 0 1 1	B ₂	
				B ₃	0 0 0 0 1 1 1 1		

Q2: Design a 8086 based circuit using 8253 IC for the following requirement.

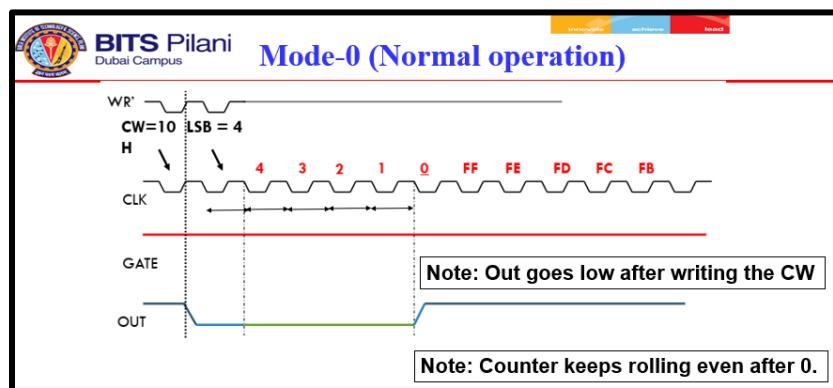
[10 Marks]

You need to generate the perfect square wave of 2 kHz from the Out pin of counter-0 of 8253 which is running in **Mode-1**. Clock input pin of counter zero is connected to 400 kHz signal. You can use other remaining counter(s) in any mode as per your requirement (to provide gate input to counter-0) with any frequency at their clock pin. You can use some minimum number of external logic gates if required. Ignore the time-period/frequency of out pins for initial few clock cycles.

Draw the block level circuit diagram and write the 8086 snippet code for the same.

8253 Control word

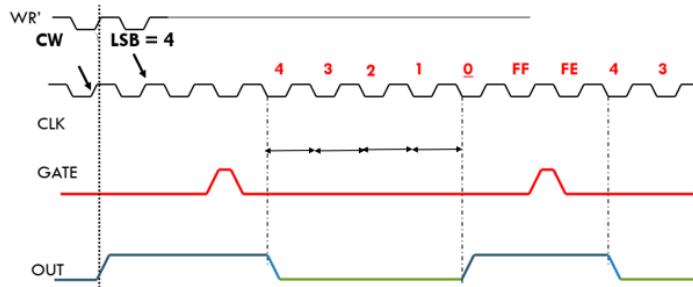
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
SC1	SC0	RW1	RW0	M2	M1	M0	BCD
Selects Counter		Read/Write Control		Timer Mode			
00	Counter 0	00	Latch Counter	000	Interrupt on T/C		0 – binary
01	Counter 1	01	R/W LSB	001	h/w re-Triggerable one shot		0000 _h FFFF _h
10	Counter 2	10	R/W MSB	010	rate generator		1 – BCD
11	Read Back Command	11	R/W LSB followed by MSB	011	Square wave generator		0000
				1x0	s/w triggered strobe		9999
				1x1	h/w triggered strobe		



P.T.O.



Mode-1 (Normal operation)

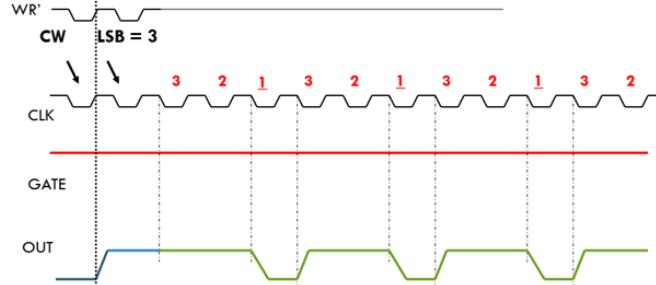


Note: Out goes high after writing the CW and goes zero after gate pulse till count reaches 0.

Note: Counter keeps rolling even after 0.



Mode-2 (Normal operation)

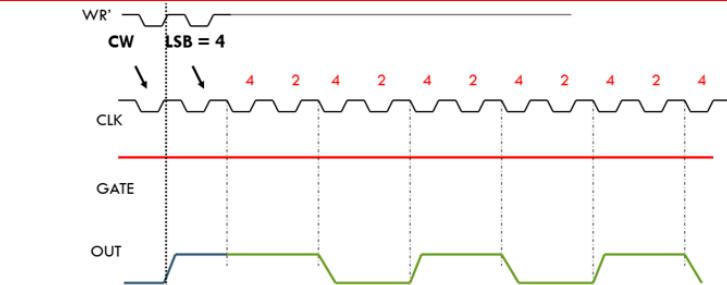


Note: Out goes high after writing the CW and goes zero when counter reaches '1'.

Note: Counter re-load the value and restart countdown.



Mode-3 (Normal operation, even value)



Note: Out goes high after writing the CW. Counter decrements by 2 and goes zero when counter reaches '1'.

Note: Counter reloads the value and restart countdown.

*****End of Part-C*****

*****Upload answers to this part under Part-C uP compre on google classroom*****



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DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI UAE

II SEM 2020-2021

Evaluation Component: TEST-1 (Closed Book)	Date/Time/Duration: 11-03-21 (2:30-3:20PM) 50 Minutes
Course No : EEE /ECE/INSTR / CSE F241	Course Name : Microprocessor and Interfacing
Maximum Marks : 30	Weightage : 15%

Note: Answer all the questions and any missing data can be assumed suitably

Q.1	<p>Q1 If ALU of a microprocessor can perform all the following operations then what is the minimum size of microprocessor:</p> <p>(a) 0BAh + 4Fh (b) 1FFAh + Aah</p>	[1]					
Q.2	<p>(a) If a microprocessor supports 32KB of memory. Then what is the size of address bus.</p> <p>(b) Find the physical address if base address is 123H and offset address is 1000H.</p>	[1+1]					
Q.3	<p>Answer the following:</p> <p>(a) If machine code is 66B178563412 then tell the Instruction format, addressing mode and whether processor is operating in 16 bit mode or 32 bit mode.</p> <p>(b) For instruction MOV [SI], BL, tell the machine code and addressing mode, if mode of operation is 32 bit.</p>	[6+3]					
Q.4	<p>(a) The following hypothetical program runs in 8086. What is the content of AX and CX register in hexadecimal, after execution.</p> <pre>MOV CX,05H CLC MOV AH,00H MOV AL,64H Up: RCR AL,01 JNC down INC AH Down: LOOP Up</pre> <p>Let X1 be an array of words, write a correct instruction to set the sixth element in X1 to FF.</p>	[4+1]					
Q.5	<p>(a) For the code section of the program. Write the content of the Register and Flags after the execution of the instruction. (You can assume that all status flags are cleared initially).</p> <table style="margin-left: 200px;"> <tr> <td>Register content</td> <td>OF,</td> <td>SF,</td> <td>CF,</td> <td>ZF , DF,</td> </tr> </table> <pre>LEA DI, 0000H MOV AX,0034H MOV BL,86H ROR AL,02 CMP AL,BL</pre> <p>(b) The following hypothetical program runs in 8086 with the machine code generated as given. For a short jump calculate the displacement generated by the assembler</p> <pre>X1: Mov AL,08 H MC:B008 Add AX, [SI]MC:0304 jmp X1</pre>	Register content	OF,	SF,	CF,	ZF , DF,	[2.5 +1.5]
Register content	OF,	SF,	CF,	ZF , DF,			
Q.6	<p>Write an 8086-assembly program code to store your registration ID in the memory location called as 'MYID' and find and store only the alphabets in ID number in a location called 'MYALPHA'</p> <p>For example, if your Registration ID is 2019AAPS1163U, then the memory location MYALPHA will have ASCII values of AAPSU.</p>	[9]					



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II SEM 2020-2021

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Course No : EEE /ECE/INSTR / CSE F241		Course Name : Microprocessor and Interfacing
Maximum Marks : 30		Weightage : 15%

Note: Answer all the questions and any missing data can be assumed suitably

MOD	00	01	10	11	
R/M					
000	[BX] + [SI]	[BX]+[SI]+d8	[BX]+[SI]+d16	W = 0	AL AX
001	[BX] + [DI]	[BX]+[DI]+d8	[BX]+[DI]+d16		CL CX
010	[BP] + [SI]	[BP]+[SI]+d8	[BP]+[SI]+d16		DL DX
011	[BP] + [DI]	[BP]+[DI]+d8	[BP]+[DI]+d16		BL BX
100	[SI]	[SI]+d8	[SI]+d16		AH SP
101	[DI]	[DI]+d8	[DI]+d16		CH BP
110	d16	[BP] + d8	[BP] + d16		DH SI
111	[BX]	[BX]+d8	[BX]+d16		BH DI

MOD	00	01	10	11	
R/M					
000	EAX	EAX+d8	EAX+d32	W = 0	AL EAX
001	ECX	ECX+d8	ECX+d32		CL ECX
010	EDX	EDX+d8	EDX+d32		DL EDX
011	EBX	EBX+d8	EBX+d32		BL EBX
100	Scaled Index	Scaled Index +d8	Scaled Index +d32		AH ESP
101	d32	EBP+d8	EBP+d32		CH EBP
110	ESI	ESI+d8	ESI+d32		DH ESI
111	EDI	EDI+d8	EDI+d32		BH EDI

EAX/AX/AL	000
EBX/BX/BL	011
ECX/CX/CL	001
EDX/DX/DL	010
ESP/SP/AH	100
EBP/BP/CH	101
ESI/SI/DH	110
EDI/DI/BH	111

REG

Segment	Prefix Value
ES	26H
CS	2EH
SS	36H
DS	3EH
FS	64H
GS	65H



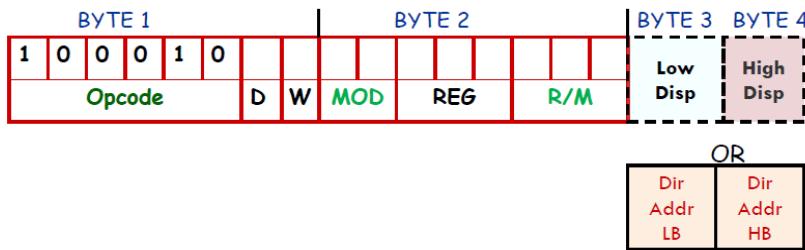
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Evaluation Component: TEST-1 (Closed Book)	Date/Time/Duration: 11-03-21 (2:30-3:20PM) 50 Minutes
Course No : EEE /ECE/INSTR / CSE F241	Course Name : Microprocessor and Interfacing
Maximum Marks : 30	Weightage : 15%

Note: Answer all the questions and any missing data can be assumed suitably



S S index base

ASCII - Hex - Binary Conversion Chart											
ASCII	Hex	Binary	ASCII	Hex	Binary	ASCII	Hex	Binary	ASCII	Hex	Binary
NUL	00	00000000	SP	20	00100000	@	40	01000000	`	60	01100000
SOH	01	00000001	!	21	00100001	A	41	01000001	a	61	01100001
STX	02	00000010	"	22	00100010	B	42	01000010	b	62	01100010
ETX	03	00000011	#	23	00100011	C	43	01000011	c	63	01100011
EOT	04	00000100	\$	24	00100100	D	44	01000100	d	64	01100100
ENQ	05	00000101	%	25	00100101	E	45	01000101	e	65	01100101
ACK	06	00000110	&	26	00100110	F	46	01000110	f	66	01100110
BEL	07	00000111	,	27	00100111	G	47	01000111	g	67	01100111
BS	08	00001000	(28	00101000	H	48	01001000	h	68	01101000
HT	09	00001001)	29	00101001	I	49	01001001	i	69	01101001
LF	0A	00001010	*	2A	00101010	J	4A	01001010	j	6A	01101010
VT	0B	00001011	+	2B	00101011	K	4B	01001011	k	6B	01101011
FF	0C	00001100	,	2C	00101100	L	4C	01001100	l	6C	01101100
CR	0D	00001101	-	2D	00101101	M	4D	01001101	m	6D	01101101
SO	0E	00001110	.	2E	00101110	N	4E	01001110	n	6E	01101110
SI	0F	00001111	/	2F	00101111	O	4F	01001111	o	6F	01101111
DLE	10	00010000	0	30	00110000	P	50	01010000	p	70	01110000
DC1	11	00010001	1	31	00110001	Q	51	01010001	q	71	01110001
DC2	12	00010010	2	32	00110010	R	52	01010010	r	72	01110010
DC3	13	00010011	3	33	00110011	S	53	01010011	s	73	01110011
DC4	14	00010100	4	34	00110100	T	54	01010100	t	74	01110100
NAK	15	00010101	5	35	00110101	U	55	01010101	u	75	01110101
SYN	16	00010110	6	36	00110110	V	56	01010110	v	76	01110110
ETB	17	00010111	7	37	00110111	W	57	01010111	w	77	01110111
CAN	18	00011000	8	38	00111000	X	58	01011000	x	78	01111000
EM	19	00011001	9	39	00111001	Y	59	01011001	y	79	01111001
SUB	1A	00011010	:	3A	00111010	Z	5A	01011010	z	7A	01111010
ESC	1B	00011011	;	3B	00111011	[5B	01011011	{	7B	01111011
FS	1C	00011100	<	3C	00111100	\	5C	01011100		7C	01111100
GS	1D	00011101	=	3D	00111101]	5D	01011101	}	7D	01111101
RS	1E	00011110	>	3E	00111110	^	5E	01011110	~	7E	01111110
US	1F	00011111	?	3F	00111111	_	5F	01011111	DEL	7F	01111111



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DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI UAE

II SEM 2020-2021

Evaluation Component: TEST-1 (Closed Book)	Date/Time/Duration: 11-03-21 (2:30-3:20PM) 50 Minutes
Course No : EEE /ECE/INSTR / CSE F241	Course Name : Microprocessor and Interfacing
Maximum Marks : 30	Weightage : 15%

Note: Answer all the questions and any missing data can be assumed suitably

Q.1	If ALU of a microprocessor can perform all the following operations then what is the minimum size of microprocessor: (a) 1Ah + 0ACh (b) 1FF4h * 5AD8h	[1]
Q.2	(a) If a microprocessor supports 32Kb of memory. Then what is the size of address bus. (b) Find the physical address if Offset address is 0100H and base address is 3015H.	[1+1]
Q.3	Answer the following: (a) If machine code is 66B967123456 then tell the Instruction format, addressing mode and whether processor is operating in 16 bit mode or 32 bit mode. (b) For instruction MOV [SI], BL, tell the machine code and addressing mode, if mode of operation is 16 bit	[6+3]
Q.4	(a) The following hypothetical program runs in 8086. Given that PUTC displays a character, the following code will display MOV AL, 'A' ADD AL, 22H AND AL, 1101 1111 CALL PUTC (b) Let X1 be an array of words, write a correct instruction to set the third element in X1 to FF.	[4+1]
Q.5	(a) For the code section of the program. Write the content of the Register and Flags after the execution of the instruction. (You can assume that all status flags are cleared initially). Register content OF, SF, CF, ZF , DF, LEA SI, 0000H MOV AX,0012H MOV BL,48H ROL AL,02 CMP AL,BL (b) Which of the following is an illegal 8086 instruction? a) mov DS, ES b) add ax, [di] c) mov ax, [bx] d) aDd bx, [bx]	[2.5 +1.5]
Q.6	Write an 8086 assembly program code to store your registration ID in the memory location called as 'MYID' and find the highest numeric number in that store the result in memory called 'MAXNUM' For example , if your Registration ID is 2019AAPS1163U, then highest numeric number is 9.	[9]



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II SEM 2020-2021

Evaluation Component: TEST-1 (Closed Book)		Date/Time/Duration: 11-03-21 (2:30-3:20PM) 50 Minutes
Course No : EEE /ECE/INSTR / CSE F241		Course Name : Microprocessor and Interfacing
Maximum Marks : 30		Weightage : 15%

Note: Answer all the questions and any missing data can be assumed suitably

MOD R/M	00	01	10	11	
				W = 0	W = 1
000	[BX] + [SI]	[BX]+[SI]+d8	[BX]+[SI]+d16	AL	AX
001	[BX] + [DI]	[BX]+[DI]+d8	[BX]+[DI]+d16	CL	CX
010	[BP] + [SI]	[BP]+[SI]+d8	[BP]+[SI]+d16	DL	DX
011	[BP] + [DI]	[BP]+[DI]+d8	[BP]+[DI]+d16	BL	BX
100	[SI]	[SI]+d8	[SI]+d16	AH	SP
101	[DI]	[DI]+d8	[DI]+d16	CH	BP
110	d16	[BP] + d8	[BP] + d16	DH	SI
111	[BX]	[BX]+d8	[BX]+d16	BH	DI

MOD R/M	00	01	10	11	
				W = 0	W = 1
000	EAX	EAX+d8	EAX+d32	AL	EAX
001	ECX	ECX+d8	ECX+d32	CL	ECX
010	EDX	EDX+d8	EDX+d32	DL	EDX
011	EBX	EBX+d8	EBX+d32	BL	EBX
100	Scaled Index	Scaled Index +d8	Scaled Index +d32	AH	ESP
101	d32	EBP+d8	EBP+d32	CH	EBP
110	ESI	ESI+d8	ESI+d32	DH	ESI
111	EDI	EDI+d8	EDI+d32	BH	EDI

EAX/AX/AL	000
EBX/BX/BL	011
ECX/CX/CL	001
EDX/DX/DL	010
ESP/SP/AH	100
EBP/BP/CH	101
ESI/SI/DH	110
EDI/DI/BH	111

REG

Segment	Prefix Value
ES	26 _H
CS	2E _H
SS	36 _H
DS	3E _H
FS	64 _H
GS	65 _H



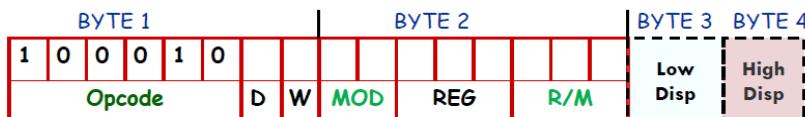
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S S In d x s as e

ASCII - Hex - Binary Conversion Chart											
ASCII	Hex	Binary	ASCII	Hex	Binary	ASCII	Hex	Binary	ASCII	Hex	Binary
NUL	00	00000000	SP	20	00100000	@	40	01000000	`	60	01100000
SOH	01	00000001	!	21	00100001	A	41	01000001	a	61	01100001
STX	02	00000010	"	22	00100010	B	42	01000010	b	62	01100010
ETX	03	00000011	#	23	00100011	C	43	01000011	c	63	01100011
EOT	04	00000100	\$	24	00100100	D	44	01000100	d	64	01100100
ENQ	05	00000101	%	25	00100101	E	45	01000101	e	65	01100101
ACK	06	00000110	&	26	00100110	F	46	01000110	f	66	01100110
BEL	07	00000111	'	27	00100111	G	47	01000111	g	67	01100111
BS	08	00001000	(28	00101000	H	48	01001000	h	68	01101000
HT	09	00001001)	29	00101001	I	49	01001001	i	69	01101001
LF	0A	00001010	*	2A	00101010	J	4A	01001010	j	6A	01101010
VT	0B	00001011	+	2B	00101011	K	4B	01001011	k	6B	01101011
FF	0C	00001100	,	2C	00101100	L	4C	01001100	l	6C	01101100
CR	0D	00001101	-	2D	00101101	M	4D	01001101	m	6D	01101101
SO	0E	00001110	.	2E	00101110	N	4E	01001110	n	6E	01101110
SI	0F	00001111	/	2F	00101111	O	4F	01001111	o	6F	01101111
DLE	10	00010000	0	30	00110000	P	50	01010000	p	70	01110000
DC1	11	00010001	1	31	00110001	Q	51	01010001	q	71	01110001
DC2	12	00010010	2	32	00110010	R	52	01010010	r	72	01110010
DC3	13	00010011	3	33	00110011	S	53	01010011	s	73	01110011
DC4	14	00010100	4	34	00110100	T	54	01010100	t	74	01110100
NAK	15	00010101	5	35	00110101	U	55	01010101	u	75	01110101
SYN	16	00010110	6	36	00110110	V	56	01010110	v	76	01110110
ETB	17	00010111	7	37	00110111	W	57	01010111	w	77	01110111
CAN	18	00011000	8	38	00111000	X	58	01011000	x	78	01111000
EM	19	00011001	9	39	00111001	Y	59	01011001	y	79	01111001
SUB	1A	00011010	:	3A	00111010	Z	5A	01011010	z	7A	01111010
ESC	1B	00011011	;	3B	00111011	[5B	01011011	{	7B	01111011
FS	1C	00011100	<	3C	00111100	\	5C	01011100		7C	01111100
GS	1D	00011101	=	3D	00111101]	5D	01011101	}	7D	01111101
RS	1E	00011110	>	3E	00111110	^	5E	01011110	~	7E	01111110
US	1F	00011111	?	3F	00111111	-	5F	01011111	DEL	7F	01111111



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Note: Answer all the questions and any missing data can be assumed suitably

Q.1	If ALU of a microprocessor can perform all the following operations then what is the minimum size of microprocessor: (a) 5Ah * 5Ch (b) 1234h + 5678h	[1]
Q.2	(a) If a microprocessor supports 20KB of memory. Then what is the size of address bus. (b) Find the physical address if Offset address is 1000H and base address is 1234F.	[1+1]
Q.3	Answer the following: (a) If machine code is 66B96712AABB then tell the Instruction format, addressing mode and whether processor is operating in 16 bit mode or 32 bit mode. (b) For instruction MOV AX, SI, tell the machine code and addressing mode, if mode of operation is 16 mode.	[6+3]
Q.4	(a) The following hypothetical program runs in 8086 .What will be the contents of registers AX, BX and SP after execution. Assume initially AX=0000, BX=0000, SP=FFFEH. Also show the Memory content of Stack segment. MOV AX, 2037H MOV BX, 0542H MOV SS, AX MOV SP, BX PUSH AX PUSH BX POP AX ADDBX,AX (b) Let X1 be an array of words, write a correct instruction to set the fifth element in X1 to FF.	[4+1]
Q.5	(a) Given that register BL contains the ASCII code of an uppercase letter, it can be converted to lowercase by (write logic required to do so). (b) Which of the following is an illegal 8086 instruction? a) add ax, [di] b) mov IP, num1 c) mov ax, [bx] d) aDd bx, [bx]	[2+2]
Q.6	Write an 8086 assembly program code to store your registration ID in the memory location called as 'MYID' and sum only the numeric values and store the sum in the memory location called 'tnum' For example , if your Registration ID is 2019AAPS1163U, then sum of the numeric value is 2+0+1+9+1+1+6+3=23.	[9]



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R/M					
000	[BX] + [SI]	[BX]+[SI]+d8	[BX]+[SI]+d16	W = 0	W = 1
001	[BX] + [DI]	[BX]+[DI]+d8	[BX]+[DI]+d16	AL	AX
010	[BP] + [SI]	[BP]+[SI]+d8	[BP]+[SI]+d16	CL	CX
011	[BP] + [DI]	[BP]+[DI]+d8	[BP]+[DI]+d16	DL	DX
100	[SI]	[SI]+d8	[SI]+d16	BL	BX
101	[DI]	[DI]+d8	[DI]+d16	AH	SP
110	d16	[BP] + d8	[BP] + d16	CH	BP
111	[BX]	[BX]+d8	[BX]+d16	DH	SI
				BH	DI

MOD	00	01	10	11	
R/M					
000	EAX	EAX+d8	EAX+d32	W = 0	W = 1
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011	EBX	EBX+d8	EBX+d32	DL	EDX
100	Scaled Index	Scaled Index	Scaled Index	BL	EBX
	+d8	+d32	+d32	AH	ESP
101	d32	EBP+d8	EBP+d32	CH	EBP
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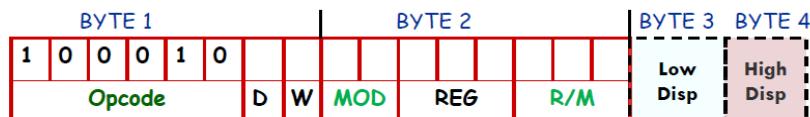
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Note: Answer all the questions and any missing data can be assumed suitably



S S Index s as e

ASCII - Hex - Binary Conversion Chart											
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SUB	1A	00011010	:	3A	00111010	Z	5A	01011010	z	7A	01111010
ESC	1B	00011011	;	3B	00111011	[5B	01011011	{	7B	01111011
FS	1C	00011100	<	3C	00111100	\	5C	01011100		7C	01111100
GS	1D	00011101	=	3D	00111101]	5D	01011101	}	7D	01111101
RS	1E	00011110	>	3E	00111110	^	5E	01011110	~	7E	01111110
US	1F	00011111	?	3F	00111111	_	5F	01011111	DEL	7F	01111111



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Evaluation Component: TEST-2 (OPEN BOOK)	Date/Time/Duration: 20-04-21 (1:30-2:20PM)50 Minutes
Course No : EEE /ECE/INSTR / CSE F241	Course Name : Microprocessor and Interfacing
Maximum Marks : 30	Weightage : 15%

Note: Answer all the questions and any missing data can be assumed suitably

Q.1	<p>The following lines of Assembly code is to be executed using 8086 Microprocessor running on frequency of 5kHz</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 5px;">Assembly Code</th><th style="text-align: center; padding: 5px;">Machine Code</th></tr> </thead> <tbody> <tr> <td style="padding: 5px;">up: mov CX,XXXXH</td><td style="padding: 5px;">B9XXXX</td></tr> <tr> <td style="padding: 5px;">MOV AX,[1000H]</td><td style="padding: 5px;">A10010</td></tr> <tr> <td style="padding: 5px;">ADD AX,BX</td><td style="padding: 5px;">03C3</td></tr> <tr> <td style="padding: 5px;">MOV [2000H],AX</td><td style="padding: 5px;">A30020</td></tr> <tr> <td style="padding: 5px;">DEC cx</td><td style="padding: 5px;">49</td></tr> <tr> <td style="padding: 5px;">JNZ up</td><td style="padding: 5px;">75F2</td></tr> </tbody> </table> <p>Note on Data XXXXH: XXXX is taken from last four digit of your Registration ID number. For example, if your ID is 2019A3PS1163H, then XXXX value is 1163.</p> <p>Calculate the following</p> <ul style="list-style-type: none"> a) Number of total machine cycles required b) Total number of T states required (Assume no wait states) <p style="margin-left: 20px;">Total time required in (milli seconds)</p>	Assembly Code	Machine Code	up: mov CX,XXXXH	B9XXXX	MOV AX,[1000H]	A10010	ADD AX,BX	03C3	MOV [2000H],AX	A30020	DEC cx	49	JNZ up	75F2	[5]				
Assembly Code	Machine Code																			
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DEC cx	49																			
JNZ up	75F2																			
Q.2	<p>Design a digital system required to send an interrupt request from eight sensors to the INTR pin of the 8086 microprocessors. The sensors can be identified by the microprocessor from the vector number during the interrupt generation.</p> <p>Following are the vector numbers</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 5px;">Sensor</th><th style="text-align: center; padding: 5px;">Vector Number</th></tr> </thead> <tbody> <tr> <td style="padding: 5px;">Sensor 0</td><td style="padding: 5px;">0A</td></tr> <tr> <td style="padding: 5px;">Sensor 1</td><td style="padding: 5px;">1A</td></tr> <tr> <td style="padding: 5px;">Sensor 2</td><td style="padding: 5px;">2A</td></tr> <tr> <td style="padding: 5px;">Sensor 3</td><td style="padding: 5px;">3A</td></tr> <tr> <td style="padding: 5px;">Sensor 4</td><td style="padding: 5px;">4A</td></tr> <tr> <td style="padding: 5px;">Sensor 5</td><td style="padding: 5px;">5A</td></tr> <tr> <td style="padding: 5px;">Sensor 6</td><td style="padding: 5px;">6A</td></tr> <tr> <td style="padding: 5px;">Sensor 7</td><td style="padding: 5px;">7A</td></tr> </tbody> </table>	Sensor	Vector Number	Sensor 0	0A	Sensor 1	1A	Sensor 2	2A	Sensor 3	3A	Sensor 4	4A	Sensor 5	5A	Sensor 6	6A	Sensor 7	7A	[5]
Sensor	Vector Number																			
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Note: Answer all the questions and any missing data can be assumed suitably

Q.3	Interface 8088 chip with 4KB of ROM using 2716 with start address of 00000H, 2KB of RAM using 6108 with start address of 08000H. You have one LS138 chip. Draw the partial circuit diagram showing the decoder connections only (all address line connections and outputs towards RAM and ROM chips). No need to draw the RAM and ROM chips.	[8]
Q.4	80286-based system is having a memory requirement of 8M. Out of this 3M of ROM and rest is RAM. The mapping is as follows 1M of ROM with starting address 000000H 1M of ROM with starting address 800000H 1M of ROM with starting address F00000H 3M of RAM with starting address 100000H 2M of RAM with starting address 900000H Chips available: 274096, 614096, LS138. Design the memory interfacing circuit. Use absolute addressing.	[12]



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Q.1	<p>The following lines of Assembly code is to be executed using 8086 Microprocessor running on frequency of 5MHz</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 5px;">Assembly Code</th><th style="text-align: center; padding: 5px;">Machine Code</th></tr> </thead> <tbody> <tr> <td style="padding: 5px;">up: mov CX,XXXXH</td><td style="padding: 5px;">B9XXXX</td></tr> <tr> <td style="padding: 5px;">MOV AX,[1000H]</td><td style="padding: 5px;">A10010</td></tr> <tr> <td style="padding: 5px;">ADD AX,BX</td><td style="padding: 5px;">03C3</td></tr> <tr> <td style="padding: 5px;">MOV [2000H],AX</td><td style="padding: 5px;">A30020</td></tr> <tr> <td style="padding: 5px;">DEC cx</td><td style="padding: 5px;">49</td></tr> <tr> <td style="padding: 5px;">JNZ up</td><td style="padding: 5px;">75F2</td></tr> </tbody> </table> <p>Note on Data XXXXH: XXXX is taken from last four digit of your Registration ID number. For example, if your ID is 2019A3PS1163H, then XXXX value is 1163.</p> <p>Calculate the following in decimals</p> <ul style="list-style-type: none"> a) Number of total machine cycles required b) Total number of T states required (Assume no wait states) <p>Total time required in (milli seconds)</p>	Assembly Code	Machine Code	up: mov CX,XXXXH	B9XXXX	MOV AX,[1000H]	A10010	ADD AX,BX	03C3	MOV [2000H],AX	A30020	DEC cx	49	JNZ up	75F2	[5]				
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Maximum Marks : 30	Weightage : 15%

Note: Answer all the questions and any missing data can be assumed suitably

Q.3	Interface 8088 chip with 3KB of ROM using 2708 with start address of 00000H, 2KB of RAM using 6116 with start address of 01000H. You have one LS138 chip. Draw the partial circuit diagram showing the decoder connections only (all address line connections and outputs towards RAM and ROM chips). No need to draw the RAM and ROM chips.	[8]
Q.4	80286-based system has a total of 448K of memory requirement out of which 256K of ROM with a starting address of 00000H and Rest is RAM with a starting address of 07000H. Chips available: 27512. 61256. LS138. Design the memory interfacing circuit. Use absolute addressing.	[12]



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DUBAI INTERNATIONAL ACADEMIC CITY, DUBAI UAE

II SEM 2020-2021

Evaluation Component: TEST-2 (OPEN BOOK)	Date/Time/Duration: 20-04-21 (1:30-2:20PM)50 Minutes
Course No : EEE /ECE/INSTR / CSE F241	Course Name : Microprocessor and Interfacing
Maximum Marks : 30	Weightage : 15%

Note: Answer all the questions and any missing data can be assumed suitably

Q.1	<p>The following lines of Assembly code is to be executed using 8086 Microprocessor running on frequency of 5kHz</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 5px;">Assembly Code</th><th style="text-align: center; padding: 5px;">Machine Code</th></tr> </thead> <tbody> <tr> <td style="padding: 5px;">up: mov CX,XXXXH</td><td style="padding: 5px;">B9XXXX</td></tr> <tr> <td style="padding: 5px;">MOV AX,[1000H]</td><td style="padding: 5px;">A10010</td></tr> <tr> <td style="padding: 5px;">ADD AX,BX</td><td style="padding: 5px;">03C3</td></tr> <tr> <td style="padding: 5px;">MOV [2000H],AX</td><td style="padding: 5px;">A30020</td></tr> <tr> <td style="padding: 5px;">DEC cx</td><td style="padding: 5px;">49</td></tr> <tr> <td style="padding: 5px;">JNZ up</td><td style="padding: 5px;">75F2</td></tr> </tbody> </table> <p>Note on Data XXXXH: XXXX is taken from last four digit of your Registration ID number. For example, if your ID is 2019A3PS1163H, then XXXX value is 1163.</p> <p>Calculate the following</p> <ul style="list-style-type: none"> a) Number of total machine cycles required b) Total number of T states required (Assume no wait states) <p style="margin-left: 20px;">Total time required in (milli seconds)</p>	Assembly Code	Machine Code	up: mov CX,XXXXH	B9XXXX	MOV AX,[1000H]	A10010	ADD AX,BX	03C3	MOV [2000H],AX	A30020	DEC cx	49	JNZ up	75F2	[5]				
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DEC cx	49																			
JNZ up	75F2																			
Q.2	<p>Design a digital system required to send an interrupt request from eight sensors to the INTR pin of the 8086 microprocessors. The sensors can be identified by the microprocessor from the vector number during the interrupt generation.</p> <p>Following are the vector numbers</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center; padding: 5px;">Sensor</th><th style="text-align: center; padding: 5px;">Vector Number</th></tr> </thead> <tbody> <tr> <td style="padding: 5px;">Sensor 0</td><td style="padding: 5px;">07</td></tr> <tr> <td style="padding: 5px;">Sensor 1</td><td style="padding: 5px;">17</td></tr> <tr> <td style="padding: 5px;">Sensor 2</td><td style="padding: 5px;">27</td></tr> <tr> <td style="padding: 5px;">Sensor 3</td><td style="padding: 5px;">37</td></tr> <tr> <td style="padding: 5px;">Sensor 4</td><td style="padding: 5px;">47</td></tr> <tr> <td style="padding: 5px;">Sensor 5</td><td style="padding: 5px;">57</td></tr> <tr> <td style="padding: 5px;">Sensor 6</td><td style="padding: 5px;">67</td></tr> <tr> <td style="padding: 5px;">Sensor 7</td><td style="padding: 5px;">77</td></tr> </tbody> </table>	Sensor	Vector Number	Sensor 0	07	Sensor 1	17	Sensor 2	27	Sensor 3	37	Sensor 4	47	Sensor 5	57	Sensor 6	67	Sensor 7	77	[5]
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Note: Answer all the questions and any missing data can be assumed suitably

Q.3	Interface 8088 chip with 8KB of ROM using 2732 with start address of 00000H, 4KB of RAM using 6116 with start address of 02000H. You have one LS138 chip. Draw the partial circuit diagram showing the decoder connections only (all address line connections and outputs towards RAM and ROM chips). No need to draw the RAM and ROM chips.	[8]
Q.4	80286-based system is having a memory requirement of 224K. Out of this 128K of RAM and rest is ROM. The mapping is as follows RAM with starting address 000000H ROM with starting address 0A0000H Chips available: 61256, 27128, LS138. Design the memory interfacing circuit. Use absolute addressing.	[12]