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# BE-256

100147

III Semester B.Tech. (CSE/ISE) Examination,
December - 2019/January - 2020

(CBCS Scheme)

## 18CIPC302 : DIGITAL SYSTEM DESIGN

Time : 3 Hours Max. Marks : 100

***Instructions :*** *(i) Question Q1 is **compulsory** and its MCQ.*
*(ii) Question Q2 and Q3 are **compulsory**.*
*(iii) Answer **any one** full question from Q4 and Q5.*
*(iv) Answer **any one** full question from Q6 and Q7.*
*(v) Answer **any one** full question from Q8 and Q9.*

**1.** Multiple choice questions. **15x1=15**

(i) Each "1" entry in a K-map square represents :

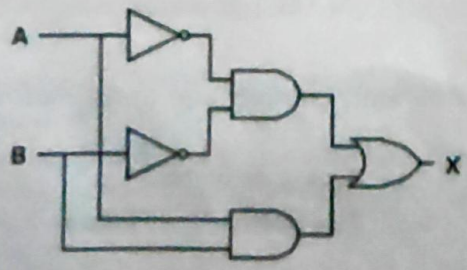
(a) A HIGH for each input truth table condition that produces a HIGH output

(b) A HIGH output on the truth table for all LOW input combinations

(c) A LOW output for all possible HIGH input conditions

(d) A DON'T CARE condition for all possible input truth table combinations

(ii) What type of logic circuit is represented by the figure shown below ?




(a) XOR (b) XNOR (c) AND (d) XAND

(iii) Odd parity of word can be conveniently tested by _____.

(a) OR gate (b) AND gate (c) NAND gate (d) XOR gate

**P.T.O.**

(iv) A Karnaugh map (K-map) is an abstract form of _____ organized as a matrix of squares.

(a) Venn Diagram (b) Cycle Diagram

(c) Block Diagram (d) Triangular Diagram

(v) Which of the following flip-flops is free from the race around the problem ?

(a) T flip-flop (b) SR flip-flop

(c) Master-Slave flip-flop (d) D flip-flop

(vi) Match the following write the correct match _____.

| | |
|---|---|
| (a) 7400 | (A) XOR Gate |
| (b) 74153 | (B) 4 inputs NAND Gate |
| (c) Parity generator and Checker | (C) Multiplexer |
| (d) 7420 | (D) 2-input NAND Gates |

(vii) One example of the use of an S-R flip-flop is as _____.

(a) Transition pulse generator (b) Racer

(c) Switch debouncer (d) Astable oscillator

(viii) In a positive edge triggered JK flip-flop, a low J and low K produces :

(a) High state (b) Low state

(c) Toggle state (d) No Change state

(ix) What is the difference between a ring shift counter and a Johnson shift counter ?

(a) There is no difference (b) A ring is faster

(c) The feedback is reversed (d) The Johnson is faster

(x) Internal propagation delay of asynchronous counter is removed by _____.

(a) Ripple counter (b) Ring counter

(c) Modulus counter (d) Synchronous counter

(xi) How many flip-flops are required to construct a decade counter ?
(a) 4 (b) 8 (c) 5 (d) 10

(xii) A 4-bit counter has a maximum modulus of _____.
(a) 3 (b) 6 (c) 8 (d) 16

(xiii) Which of the following is decade counter ?
(a) IC 7493 (b) IC 7490 (c) IC 7491 (d) IC 7492

(xiv) How is a J-K flip-flop made to toggle ?
(a) $J=0, K=0$
(b) $J=1, K=0$
(c) $J=0, K=1$
(d) $J=1, K=1$

(xv) The characteristic equation of S-R latch is _____.
(a) $Q(n+1)=(S+Q(n))R'$
(b) $Q(n+1)=SR+Q(n)R$
(c) $Q(n+1)=S'R+Q(n)R$
(d) $Q(n+1)=S'R+Q'(n)R$

2. (a) Simplify the given Boolean expression using McClusky method. 6
$Y=f(a, b, c, d)=\sum(0, 2, 6, 7, 9, 10, 12)$ verify the result using K-Map.
(b) Distinguish prime implicit and essential prime implicit. 3
(c) Simplify the Boolean functions using K-Map : 8
$F1=\sum m(0, 2, 6, 10, 11, 12, 13)+d(3, 4, 5, 14, 15)$
$F2=\sum m(1, 2, 6, 7, 8, 13, 14, 15)+d(3, 5, 12)$

3. (a) Design 4:1 MUX using NAND gates and realise Full adder using NAND gates. 7
(b) Design 3-of 8 Decoder using basic gates and specify decoder application. 5
(c) Design two-bit comparator circuit, represent truth table, K-maps and logic diagram. 5

4. (a) Demonstrate JK flip-flop working with the help of circuit diagram and Illustrate how to avoid the propagation delay in JK flip-flop. 10
(b) Summarise flip-flop. Design and explain SISO and SIPO shift register, draw the waveform for inputs 1010. 7

**OR**

5. (a) Design and explain SR flip-flop working, and its applications. 7
   (b) Differentiate between Latch and Flip-Flops. 4
   (c) Debate sequential and combinational logic circuits with examples. 6

6. (a) Design 3-bit ripple down counter using D flip-flop with circuit diagram. 9
   (b) Design mod-6 asynchronous counter using JK flip-flop. 8

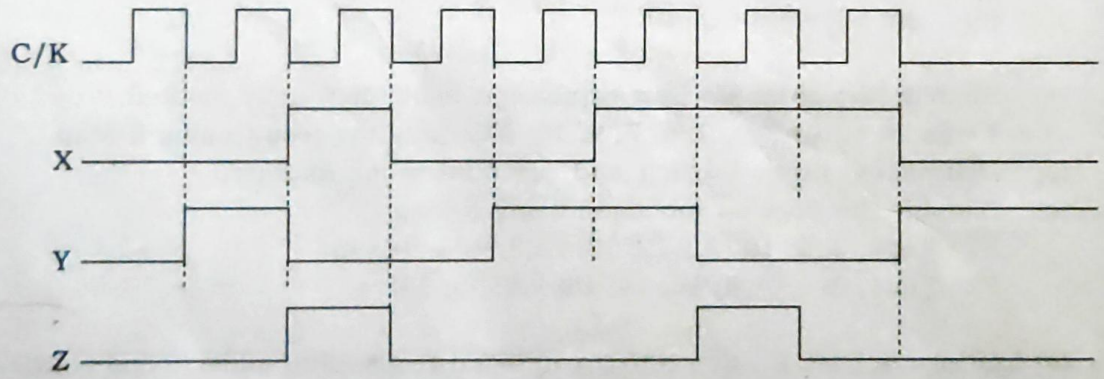
**OR**

7. (a) Design a decade counter using JK flip-flop, represent its truth table, K-maps and logic diagram. 9
   (b) Represent all four flip-flops using Finite State Machine. 8

8. (a) Design binary sequence detector that detect '011' using Moore and Mealy approach. 9
   (b) Summarise Moore and Mealay model and differentiate the same. 8

**OR**

9. (a) Timing diagram have 7 clock cycles. The X, Y are two inputs and Z is output. Z remain high for one clock period when Y goes from high to low and if at that time other input X remains at logic high. 11




Given synchronous sequential logic circuit timing diagram that has two inputs X, Y and Z as outputs. Draw state transition diagram, synthesis table and design equations for the timing diagram given above.

   (b) Discuss state reduction techniques with example. 6

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