

BE-258

III Semester B.Tech. (CSE/ISE) Examination, December - 2019/January - 2020 (CBCS Scheme)

COMPUTER SCIENCE AND ENGINEERING

18CIPC304: Computer Organization and Architecture

Time	: 3 F	Hours Max. Marks	: 100
		on: Answer Q1 compulsory, Q2 or Q3, Q4, Q5 compulsory, Q6 or Q7 and Q8 or Q9.	
		15x	1=15
Q1.	(i)	The Program counter is incremented	
		(a) After the instruction decoding	
		(b) After the IR instruction gets executed	
		(c) After the Fetch cycle	
		(d) None of the above	
	(ii)	While CPU is executing a program, If an interrupt occurs then	
		it	
		(a) It follows the next instruction in the program	
		(b) Jumps to instruction in other registers	
		(c) Breaks the normal sequence of execution of instructions	
		(d) Stops executing the program	
	(iii)	Cache memories are used for	
	(iv)	Virtual memories are used for	
	(v)	RAM stands for	
	(vi)	PROM stands for	
	(vii)	DMA is used for	
	(viii)	ROM is used for	
	(ix)	ISP stands for	



	(x)	Which Register can interact with the secondary storage? (a) MAR (b) PC (c) IR (d) R ₀	
	(xi)	When generating physical address from a logical address, the offset is stored in	
	(xii)	Any condition that causes a processor to stall is called as (a) Hazard (b) Page fault (c) System error (d) None	
	(xiii	The addressing mode, where user/programmer directly specify the Operand value is	
	19	(a) Immediate (b) Direct (c) Definite (d) Relative	
	(xiv)	Pipelining increases (a) Throughput (b) Time (c) Space (d) All of the mentioned	
	(xv)	RISC stands for	
Q2.	(a) (b)		8
		OR	
Q3.	(a) (b)		8
24.	(a) (b)		9
25.		Define the following: (i) Access time (ii) Cycle time (iii) Block size (iv) Bandwidth (v) Latency (vi) Block access time Write a note on virtual memories.	
	(D)	write a note on virtual memories.	
6.		What is Pipelining? Explain. 6 6 6 6 6 6 6 6 6 6 6 6 6	
		Explain superscalar processor with its operations. What is Data hazard? Explain. OR	

Q9. (a) List various types of printers.

(b) Explain the key concepts of visual displays.

(c) Write a note on input devices.

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