# Evaluation of Extra High Voltage (XHV) Power Module for Gen3 10 kV SiC MOSFETs in a Mobile Utility Support Equipment based Solid State Transformer (MUSE-SST)

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***Abstract*—MV solid state transformers enabled by SiC semiconductor devices is a promising replacement to conventional low frequency transformers. However, when MV SiC devices are used in converter applications, they are exposed to a high peak stress (5 kV to 10 kV) and a very high $dv/dt$ (10 kV/µs to 100 kV/µs). Operating these semiconductor devices at these high peak stresses require careful designing from the packaging point of view, as well as designing the auxiliary systems such as the gate drivers and busbars, to handle the peak stress conditions. Recently, an extra high voltage (XHV) power module has been developed by Wolfspeed to package the 10 kV SiC MOSFETs for continuous and reliable operation. This paper aims at testing these modules in continuous operation for qualifying their operation in a MV solid state transformer. Reliable operation of these modules require the development of reliable auxiliary parts including gate drivers, bus bars and inductors. Design and development of the auxiliary system is also carried out. Successful tests demonstrating operation at MV levels are also shown. These tests serve as a qualification method for using these devices in a MV solid state transformer. It is envisaged that successful operation of these devices would accelerate the growth and deployment of MV SiC devices for field operation.**

***Keywords*—*10 kV Gen3 SiC devices, gate driver, medium voltage, solid-state transformer, transformer isolation, XHV-6 modules, XHV-9 modules***

## I. Introduction

Extensive research in the semiconductor industry combined with superior material properties of SiC over Silicon (Si) have propelled the development of MV SiC power devices [1], [2]. Lower switching and conduction losses in SiC devices as compared to Si devices have enabled medium voltage, medium frequency applications without the use of complicated/multilevel converter topologies [3]. The application of high voltage power modules in medium voltage converters is demonstrated [3]–[7]. A MV Mobile Utility Support Equipment based Solid State Transformer (MUSE-SST) concept is introduced in [8]. The MUSE-SST is used for inter-connecting a MV 4160 V - 60 Hz grid to a LV 480 V - 60 Hz grid. The voltage transformation is handled by three stages - Front-End Converter: MV (MV:AFEC), Dual Active Bridge (DAB) and the Front-End Converter: LV (LV:AFEC). The system consists of $LCL$ with $R_d - C_d$ filters on both the grid-connected converters. The MV side of the MUSE-SST is realized using latest generation 10 kV SiC MOSFET packaged in a Extra High Voltage (XHV) module, and the LV side is realized using high performance CAS325M12HM2 Wolfspeed modules.

In order to realize the MUSE-SST, reliable operation of all the components should be ensured. Since, the low-voltage converters are realized using commercially available and more matured 1200 V SiC technology, this paper focuses on the design and development of the relatively new 10 kV SiC technology based converter system with the XHV based module as the basic building block. The basic electrical and thermal parameters of the module is reported in [9]. A detailed characterization of the XHV module is carried out in [10]. In addition, continuous heat run tests is also demonstrated in [3] for voltages less than 3 kV. In this paper, the evaluation of the XHV power module is carried out taking into account the high stress (peak voltage and high $dv/dt$) experienced by it. Testing at voltages around 5 kV is carried out. The design and development of the auxiliary system (gate driver, busbar, and inductor) is also provided.

## II. Issues in MV converter systems

MV converters are generally plagued with common mode (CM) current issues which needs to be accounted for while designing and running the system. Due to the high $dv/dt$ exhibited by the MV devices, a current through the parasitic capacitances' path is observed. The parasitic capacitive current is mainly observed through two different paths: through the gate driver, and through the heatsink. These common mode currents flow through the ground and might lead to disruptions in the control ground [8].

### *A. Common mode current through the gate driver and the heatsink*

In the gate driver, the major path for the common mode current (due to the high $dv/dt$) is through the isolation transformer and the signal path (optical fiber in most cases). The optical fiber offers very low isolation capacitance, and most of the common mode current flows through the isolation transformer.

The magnitude of the common mode (CM) current ($I_{cm}$) is directly affected by the $dv/dt$ and parasitic capacitance ($C_p$)

$$i_{cm} = C_p \frac{dv}{dt} \tag{1}$$

This necessitates a gate driver isolation with ultra low capacitive coupling, to minimize the common mode current flow through the isolation transformer, along with having a high voltage isolation across the transformer. A gate driver is designed according to the requirements and extensive testing is carried out to validate its operation in converters [11].

Due to the capacitance of the baseplate isolation material, a common mode current path is present through the heatsink if the heatsink is grounded. In MUSE-SST, the heatsink grounded through the fan connected to it. Common mode chokes are connected to the input of the fan to impede the flow of common mode current through it. Fig. 1 shows the common mode current path in a MV converter system in MUSE-SST.

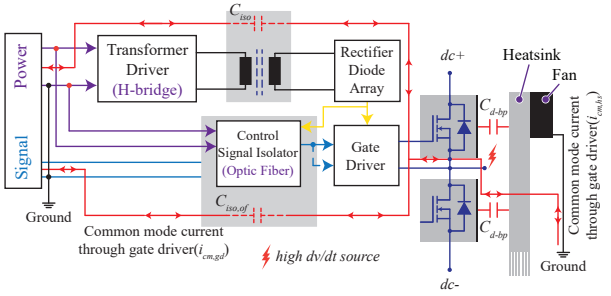



Fig. 1: Schematic representation of the common mode current path for the high side gate driver, and the heatsink in a half-bridge configuration.

### B. Differential mode current through inductor

The parasitic capacitances across the inductors lead to an additional current through these inductors. The differential mode current flows through the devices and causes additional switching losses. It is therefore necessary to minimize these parasitic capacitances. Fig. 2 shows the differential mode current path through the inductors. Several techniques such as $dv/dt$ filters ($RL$ dampeners connected in series with the inductor) or magnetic coupling in parallel with the inductor can be used to bypass the effect of these capacitive currents on the switching devices. A method is proposed in [12] to reduce the effect of these additional currents where a small inductor is connected in series with the $LCL$ filter inductor (which helps in changing the resonant frequency of the system).

## III. Design of the MV Converter System

The realization of a MV converter system not only requires the MV SiC devices to operate reliably, but also requires a reliable auxiliary system. Individual parts should be designed accordingly to ensure proper operation of a MV converter system.

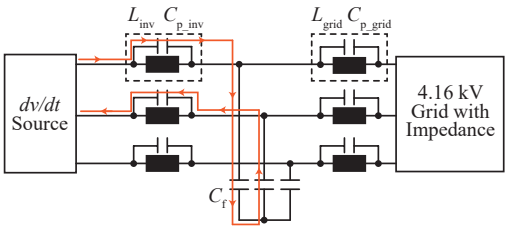



Fig. 2: Differential mode current flowing through the $LCL$ filter due to the parasitic capacitance across the $LCL$ filter inductors.

### A. XHV power modules

The building block for the MV side of the MUSE-SST is the 10 kV SiC MOSFET packaged in a XHV power module as shown in Fig. Two XHV packages are available namely XHV-6 and XHV-9 which is a three-phase two-level package and a half-bridge package respectively (Fig. 3). However, the dies can be populated in a custom manner. The internal structure of the module is shown in Fig. 3c. The MUSE-SST employs XHV-6 modules with un-populated submodule 2 and submodule 3 (due to the unavailability of XHV-9 modules during the time of commencement of the work). Each switch position is populated with six dies (total current rating of 90 A).

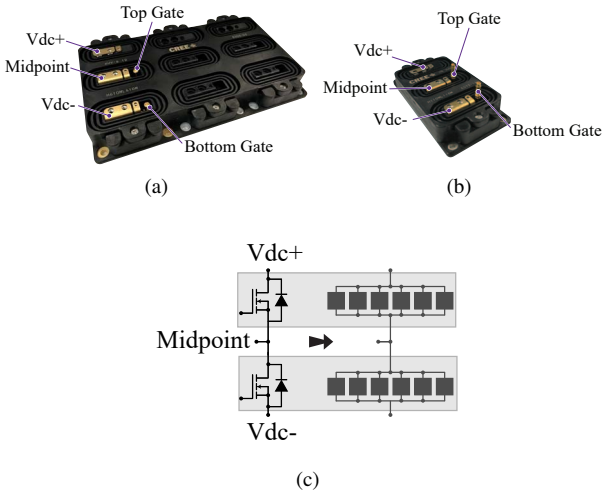
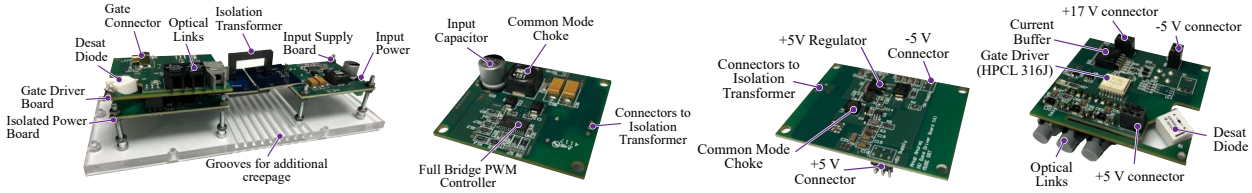



Fig. 3: (a) 10 kV SiC MOSFET packed in a XHV-6 module from Wolfspeed. Only, the first sub-module is populated and the other two sub-modules are kept un-populated (b) 10 kV SiC MOSFET packed in a XHV-9 module from Wolfspeed (c) Six 10 kV SiC MOSFET dies in parallel packaged in the form of a half-bridge in a XHV module.

### B. MV gate driver

In MUSE-SST, the MV SiC devices are exposed to a high peak stress (5 kV to 10 kV) and a very high $dv/dt$ (10 kV/µs to 100 kV/µs). This necessitates a gate driver with a dc-dc isolation stage having a ultra-low coupling capacitance in addition to be able to withstand the high isolation voltage. Fig. 4 shows the custom made gate driver for MUSE-SST [11], [13]. The gate driver is designed with three major objectives: high isolation voltage between primary and secondary, low coupling



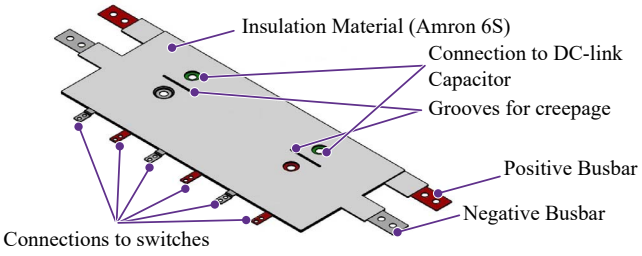

(a) (b) (c) (d)

Fig. 4: (a) Designed gate driver for driving 10 kV SiC MOSFETs which includes inherent short circuit protection and provides low capacitive isolation. Photograph of the (b) Input power board, (c) Isolated power board, and (d) Gate Driver Board.

capacitance between primary and secondary, and design for a small/optimized footprint. The gate driver transformer is designed to have a minimal parasitic capacitance for driving the 10 kV SiC MOSFETs with such high $dv/dt$.

### C. Busbar design

Insulation requirements in MV converters requires careful design considerations for avoiding short circuits or breakdown during operation. In addition, loop inductance of the busbar should be minimized to avoid voltage overshoots across the switching devices. A sandwiched structure with an insulating material between them solves both the issues. Care should be taken to ensure the effective insulation strength of the material, as well as clearance and creepage requirements for the operating voltage. In MUSE-SST, a sandwiched busbar structure is employed (manufactured by Mersen [14]) to enable reliable operation of the 10 kV SiC MOSFETs. Fig 5 shows the busbar structure along with the placement of the dc-link capacitors on the busbars.

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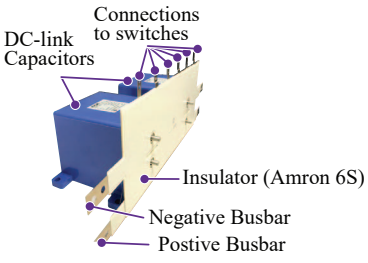
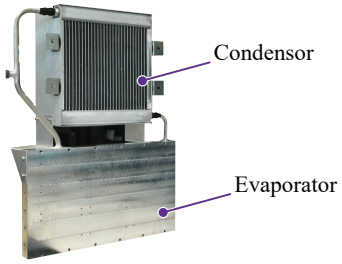



(b)

Fig. 5: (a) CAD diagram of the busbar used for testing the XHV modules. A sandwiched structure is used with proper clearance and creepage, and (b) Placement of the DC-link capacitors along with the busbar.

### D. Heatsink design

The MUSE-SST system employs an efficient thermal solution which uses a loop thermosyphon based heatsink (Fig. 6(a)) manufactured by Advanced Cooling Technologies (ACT) [15]. Heat generated by the power semiconductor devices during operation causes the liquid inside the evaporator to change its phase. This, combined with the condensation of liquid in the condenser, generates a gravitational pressure imbalance which maintains the fluid circulation between the condenser and evaporator. Fig. 6(b) shows an FEM simulation of the evaporator block. An ambient temperature of 50°C is assumed and instead of individual dies, it is assumed that the baseplate is the heat source. The temperature distribution is therefore estimated.

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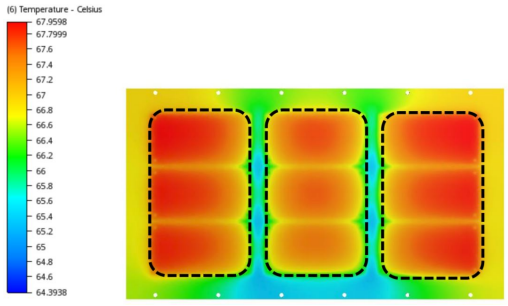


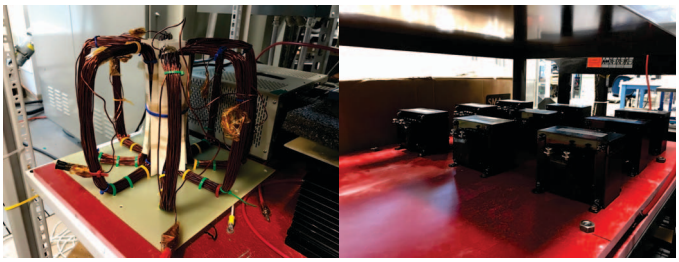

(b)

Fig. 6: (a) Loop thermosyphon solution for heat dissipation in the MV converter system (b) FEM simulation of the loop thermosyphon solution.

### E. Medium Voltage Inductors

The design of a MV inductor needs careful considerations due to the presence of a high $dv/dt$ across them during

switching transitions [12]. For initial testing purposes, an air core inductor with a value of 6.2 mH, is used in the system. The air core inductor do not have the turn-to-core capacitance, which makes them suitable for driving MV SiC converters. Also the absence of a core eliminates the insulation between core and winding, thus making it suitable for laboratory testing purposes. Fig. 7(a) shows the air-core inductor used for testing purposes. In practical situations, the air-core inductor is not feasible, and hence a series connected low voltage inductor chain can also be used as the medium voltage inductor. Fig. 7(b) shows a series connected low voltage inductor chain designed in the laboratory. Commercially available inductors with a blocking capacity of 600 V dc are connected in series depending on the voltage, current and inductance requirements. An optimum design of these inductors is necessary to minimize switching losses due to the additional differential mode current which flows through the parasitic capacitance of the inductors.



(a) (b)

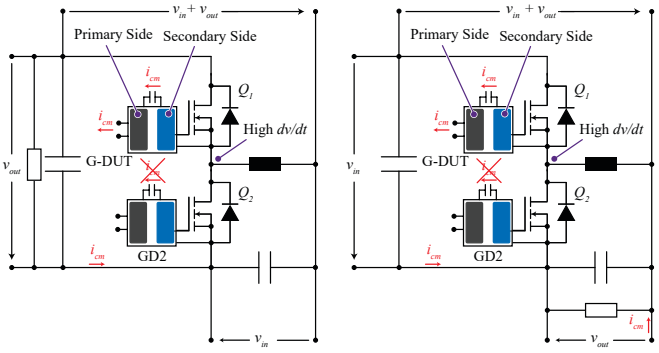
Fig. 7: (a) Air core inductor used for testing in the laboratory (b) Series-connected low voltage (600 V) inductors to enable medium voltage operation (The wire connection in the series connected inductor is not shown).

## IV. Test Methodology

With the final use of the 10 kV SiC MOSFETs aimed at designing and testing the MUSE-SST converter system, a series of tests is conducted to qualify the XHV modules. The dc-link of the medium voltage converter is designed with two series connected capacitors having a total 10 kV blocking voltage capacity (individual values of 50 µF and 5 kV blocking capacity). Additional snubber capacitors, which are mounted close to the modules are also used. A 3 kV - 50 A dc power supply from Magna Power is used for initial testing purposes. High voltage probes from CIC research (DP20 series) are used to monitor the individual high voltage signals. The low voltage signals are monitored using Tektronix differential probes (THDP0200). Current monitoring is carried out by Pearson current monitors. A number of converters are implemented to validate the operation of the 10 kV SiC MOSFETs. The gate drivers are tested for high voltage insulation, as well as continuous operation, and hence double pulse tests are not carried out for this study [11]. Continuous operation modes are emulated to stress the 10 kV SiC MOSFET in the XHV module.

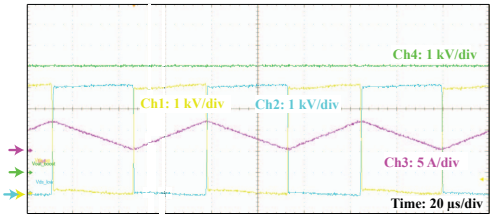
### A. Buck Converter and Boost Converter Tests

The initial testing of the XHV packaging along with the 10 kV SiC MOSFET is carried out in a buck converter topology. A buck converter topology is employed to validate the gate driver operation rather than stressing the device. A boost converter topology is thereafter employed to stress the device by providing a higher voltage across it. Fig. 8 shows the schematic of the test setups. Experimental test results are also shown in Fig. 9 and Fig. 10.




(a) (b)

Fig. 8: (a) Boost converter topology, and (b) Buck converter topology to test continuous converter operation.

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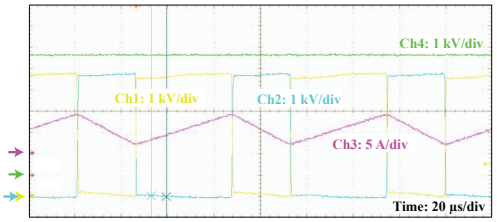
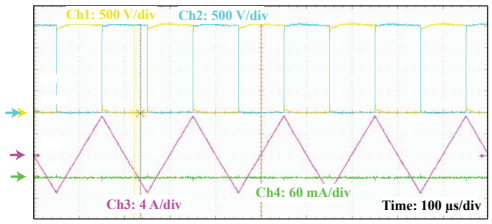



(b)

Fig. 9: Experimental results of boost converter for an output voltage of (a) 5000 V, and (b) 5500 V. (Ch1: Voltage across MOSFET $Q_2$; Ch2: Voltage across diode (body diode of $Q_1$; Ch3: Inductor current; Ch4: Output voltage).

### B. Buck-boost Converter Tests

The buck-boost converter tests is carried out since the device blocks the sum of the input and output voltage ($v_{in} + v_{out}$). This serves as a major advantage since high voltage tests can be carried out with lower voltage input power supplies. In

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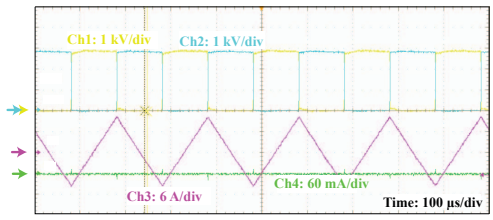
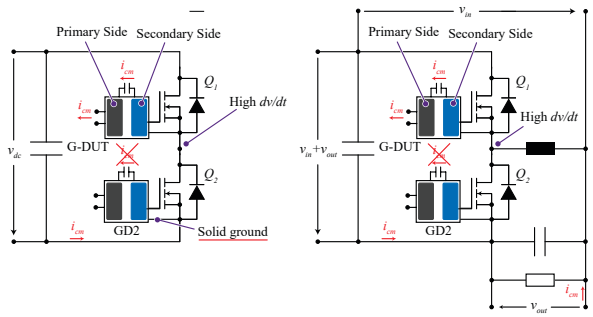



(b)

Fig. 10: Experimental results of buck converter for an input voltage of (a) 2000 V, and (b) 2800 V. (Ch1: Voltage across MOSFET $Q_1$; Ch2: Voltage across MOSFET $Q_2$; Ch3: Inductor current; Ch4: Common mode current through the gate driver for $Q_2$).

this paper, a 3 kV - 50 A DC power supply to impress 6 kV across the switching device. For the MUSE-SST, a half-bridge with dc-link capacitors serve as a building block (as shown in Fig. 11(a)). To keep the building block unchanged, a modified buck-boost converter is used as shown in Fig. 11(b), where the dc-link capacitors are connected across the switches.

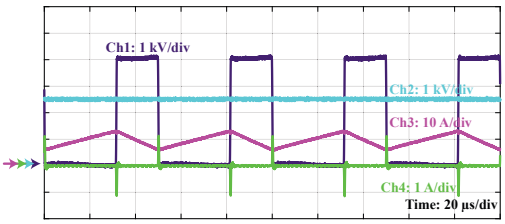



(a) (b)

Fig. 11: (a) Building block for MUSE-SST system (dc-link capacitors with busbars and switching devices), and (b) Modified buck-boost converter topology to test continuous converter operation.

### C. Full Bridge Converter Tests

The full-bridge converter tests are carried out to ensure the operation of two modules working together on the same heatsink. In addition, the gate drivers are also tested since the effective common mode current increases. With the aim of validating the MUSE-SST system, the full bridge tests of the device proves to be the next step in qualifying the devices, and therefore the entire system. In this setup, an inductor is connected across the midpoint of both the half bridges to

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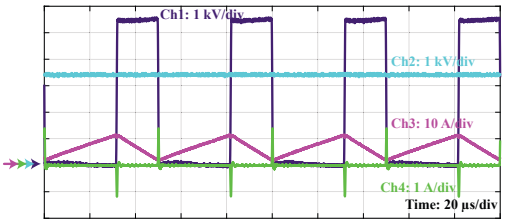
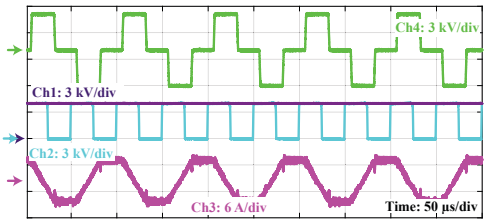



(b)

Fig. 12: Experimental results of buck boost converter for an output voltage of (a) 4000 V, and (b) 5500 V. (Ch1: Voltage across DUT; Ch2: Output voltage ($v_{out}$); Ch3: Inductor current; Ch4: Gate driver circuit CM current).

allow a current flow through the inductor and thus the devices. Experimental tests are carried out to validate the operation of the devices. Fig. 13 shows the operation of a full-bridge inverter in a complementary fashion, where a voltage of 5 kV is applied. A boost converter is used to generate the input voltage of 5 kV due to non-availability of power supply more than 3 kV in the laboratory. Due to the non-availability of high power load, a sinusoidal modulation technique is used to validate the operation of the XHV devices at higher currents (but lower voltages), and is shown in Fig. 14.

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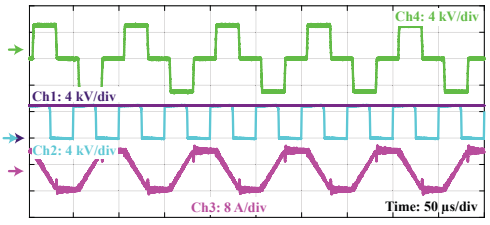


(b)

Fig. 13: Experimental results of full bridge converter for an output voltage of (a) 4000 V, and (b) 5000 V. (Ch1: Input Voltage; Ch2: Voltage across the MOSFET of the boost converter; Ch3: Current through the full bridge converter inductor; Ch4: Voltage across the mid-points of the full bridge inductor).

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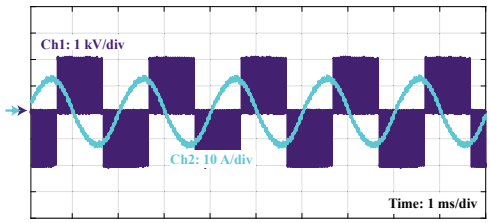


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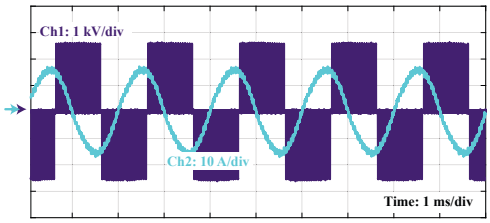
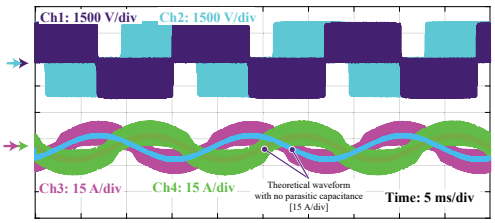



(b)

Fig. 14: Experimental results of full bridge converter with sinusoidal modulation for an output voltage of 2500 V with a peak current of (a) 14 A, and (b) 17 A. (Ch1: Voltage across the mid-points of the full bridge inductor; Ch2: Current through the full bridge converter inductor).

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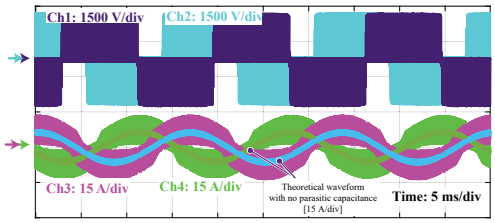


(b)

Fig. 15: Experimental results of three-phase inverter with a $RL$ load with a resistance of 100 Ω per phase and and inductance of 20 mH per phase with an input voltage of (a) 2000 V, and (b) 2500 V. (Ch1: Line-to-line voltage across R-phase; Ch2: Line-to-line voltage across R-phase; Ch3: R-phase current; Ch4: Y-phase current).

### *D. Three-phase Inverter Tests*

With the device operating in the full-bridge mode, the final setup for qualifying the converter system (including devices and gate drivers) includes operating a three-phase inverter. A dc input of 2500 V is applied and the three-phase inverter is operated in open loop. A three-phase $RL$ load with a resistance of 100 Ω per phase and and inductance of 20 mH per phase is used. This emulates the operation of the XHV devices in the MUSE-SST system and more importantly evaluates the device performance under real operating conditions. The ability of the control circuitry to handle the common mode currents originating from the converter system is also tested. Experimental results demonstrating the operation of the three-phase inverter system is shown in Fig. 15. It can be seen that the current through the inductor is not a pure sinusoidal waveform. This is due to the presence of parasitic capacitance across the inductor [12]. A zoomed-in version of Fig. 15 is provided in Fig. 16 where a current spike is observed at every switching instant. This is attributed to the high $dv/dt$ across the device combined with the parasitic capacitance of the inductor, which forces a differential mode current through the inductor.

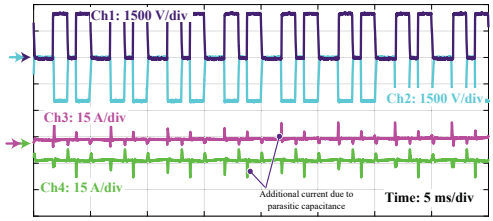


Fig. 16: Zoomed in version of Fig. 15 where a spike is observed in the current due to the high $dv/dt$ across the 10 kV SiC MOSFET and the parasitic capacitance across the filter inductors. (Ch1: Line-to-line voltage across R-phase; Ch2: Line-to-line voltage across R-phase; Ch3: R-phase current; Ch4: Y-phase current).

## V. Conclusions

This paper presents an evaluation of the XHV power module is carried out taking into account the high stress (peak voltage and high $dv/dt$) experienced by it. Testing at voltage levels up to 5 kV is carried out. The design and development of the auxiliary system (gate driver, busbar, and inductor) is also provided in brief. The testing includes the test for the intrinsic body diode (used in boost, buck and buck-boost topology) which proves that an additional JBS diode is not required for continuous operation up to 5 kV voltage levels. Testing beyond 5 kV has not been carried out. From the three-phase inverter tests, a high frequency current spike is observed in the inductor current which is the effect of the high switching $dv/dt$ and the parasitic capacitance across the filter inductor. Improvement in the design of the filter inductors is necessary to avoid the additional switching current (current spike). In future, testing the converters at 7 kV dc bus will be attempted and the design issues needs to be identified. The testing of these XHV packaged 10 kV SiC MOSFET can accelerate the growth and deployment of these devices for field operation thus replacing conventional Si IGBTs and also these devices can help in reducing the complexity of converters in various applications.

## References

[1] A. Huang, L. Cheng, J. W. Palmour, and C. Scozzie, "Ultra High Voltage SiC Power Devices and Its Impact on Future Power Delivery System," in *PCIM Europe 2014; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, May 2014.

• • •

[2] J. W. Palmour, "Silicon carbide power device development for industrial markets," in *2014 IEEE International Electron Devices Meeting*, Dec 2014.

[3] A. Kumar, S. Parashar, and S. Bhtattacharya, "Continuous Heat Run Test of Latest Generation Power Modules for 10 kV 4H-SiC MOSFETs in Medium Voltage Power Converters," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 1949–1955.

[4] M. K. Das, C. Capell, D. E. Grider, S. Leslie, J. Ostop, R. Raju, M. Schutten, J. Nasadoski, and A. Hefner, "10 kV, 120 A SiC half H-bridge power MOSFET modules suitable for high frequency, medium voltage applications," in *2011 IEEE Energy Conversion Congress and Exposition*, Sep. 2011, pp. 2689–2692.

[5] K. Mainali, A. Tripathi, S. Madhusoodhanan, A. Kadavelugu, D. Patel, S. Hazra, K. Hatua, and S. Bhattacharya, "A Transformerless Intelligent Power Substation: A three-phase SST enabled by a 15-kV SiC IGBT," *IEEE Power Electronics Magazine*, vol. 2, no. 3, pp. 31–43, Sep. 2015.

[6] D. Rothmund, T. Guillod, D. Bortis, and J. W. Kolar, "99 % Efficient 10 kV SiC-Based 7 kV/400 V DC-Transformer for Future Data Centers," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2018.

[7] ——, "99.1 % Efficient 10 kV SiC-Based Medium Voltage ZVS Bidirectional Single-Phase PFC AC/DC Stage," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, pp. 1–1, 2018.

[8] A. Anurag, S. Acharya, Y. Prabowo, V. Jakka, and S. Bhattacharya, "Design of a Medium Voltage Mobile Utilities Support Equipment based Solid State Transformer (MUSE-SST) with 10 kV SiC MOSFETs for Grid Interconnection," in *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, June 2018, pp. 1–8.

[9] B. Passmore et. al, "The next generation of high voltage (10 kV) silicon carbide power modules," in *2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Nov 2016, pp. 1–4.

[10] D. Johannesson, M. Nawaz, and K. Ilves, "Assessment of 10 kV, 100 A Silicon Carbide MOSFET Power Modules," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 5215–5225, June 2018.

[11] A. Anurag, S. Acharya, Y. Prabowo, G. Gohil, and S. Bhattacharya, "Design Considerations and Development of an Innovative Gate Driver for Medium Voltage Power Devices with High dv/dt," *IEEE Transactions on Power Electronics*, 2018.

[12] S. Acharya, A. Anurag, Y. Prabowo, and S. Bhattacharya, "Practical Design Considerations for MV LCL Filter Under High dv/dt Conditions Considering the Effects of Parasitic Elements," in *2018 9th IEEE International Symposium on Power Electronics for Distributed Generation Systems (PEDG)*, June 2018, pp. 1–7.

[13] A. Anurag, S. Acharya, G. Gohil, and S. Bhattacharya, "A Gate Driver Design for Medium Voltage Silicon Carbide Power Devices with High dv / dt," in *IECON 2018 - 44th Annual Conference of the IEEE Industrial Electronics Society*, Oct 2018, pp. 877–882.

[14] "Mersen Electrical Power," http://ep-us.mersen.com/, accessed: 2018-03-25.

[15] "High Performance Power Electronics Coolers," www.1-act.com/, accessed: 2018-03-25.

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