

# Assessment of 10 kV, 100 A Silicon Carbide MOSFET Power Modules

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**Abstract**—This paper presents a thorough characterization of 10 kV SiC MOSFET power modules, equipped with third-generation MOSFET chips and without external free-wheeling diodes, using the inherent SiC MOSFET body-diode instead. The static performance (e.g.,  $I_{DS}-V_{DS}$ ,  $I_{DS}-V_{GS}$ , C-V characteristics, leakage current, body-diode characteristics) is addressed by measurements at various temperatures. Moreover, the power module is tested in a simple chopper circuit with inductive load to assess the dynamic characteristics up to 7 kV and 120 A. The SiC MOSFET power module exhibits an on-state resistance of 40 mΩ at room-temperature and leakage current in the range of 100 nA, approximately one order of magnitude lower than that of a 6.5 kV Si-IGBT. The power module shows fast switching characteristics with the turn-on (turn-on loss) and turn-off (turn-off loss) times of 130 ns (89 mJ) and 145 ns (33 mJ), respectively, at 6.0 kV supply voltage and 100 A current. Furthermore, a peak short-circuit current of 900 A and a short-circuit survivability time of 3.5 μs were observed. The extracted characterization results could serve as input for power electronic converter design and may support topology evaluation with realistic system performance predictability, using SiC MOSFET power modules in the energy transmission and distribution networks.

**Index Terms**—Device characterization, power modules, short-circuit robustness, SiC mosfets, wide bandgap devices.

## I. INTRODUCTION

THE general market and technology trends in the electric power system research field are striving towards compact and high-efficiency conversion for transmission and distribution of electrical energy. The main objectives are for instance increased power transfer capability, more system compactness, reduced energy loss and with lower environmental impact, enabled by high-voltage direct current transmission (HVDC) systems and flexible ac transmission systems (FACTS). In general, the performance of power electronic converter systems is mainly determined by the active semiconductor components inside. With these considerations in mind, the basic research focus within

the power electronics research field has partly shifted from traditional silicon (Si) material to wide-bandgap-based semiconductor material systems [e.g., silicon carbide (SiC) and gallium nitride (GaN)]; thanks to superior physical properties of wide-bandgap materials in comparison to that of Si counterpart [1]. The SiC semiconductor material is predicted to enable semiconductor devices with higher blocking voltage capabilities, which can operate at higher temperatures and operate with higher switching frequencies than that of Si devices [1]. For example, the electric breakdown field strength in SiC is about one order of magnitude larger than that of Si counterpart that allows devices with thinner drift regions but with sustained blocking voltage capabilities. Several high-voltage SiC devices have recently been developed such as 15 kV metal-oxide semiconductor field-effect transistor (MOSFET) [2], 22 kV emitter turn-off (ETO) thyristor [3] and 27 kV insulated-gate bipolar transistor (IGBT) [4]. Furthermore, a SiC PIN diode using a 268-μm-thick n-layer doped to  $(1-2) \times 10^{14} \text{ cm}^{-3}$ , treated with carrier lifetime enhancement process and coupled with improved junction termination extension (JTE) structure, achieved a blocking voltage over 26.9 kV and low differential on-resistance of 9.7 mΩ · cm<sup>2</sup> [5]. In contrast to bipolar power devices (e.g., IGBTs and gate turn-off (GTO) thyristor), unipolar devices (e.g., MOSFETs and junction field-effect transistors (JFETs)) offers faster switching capabilities as a result of absence of charge carrier plasma extraction from the drift region. The main technological challenges in front of high-voltage SiC device development before their realization in the field are growth of high quality thick epitaxial process, reduction of extended defects, stable carrier life times, robust JTE step, and mature surface passivation process. Although few packages are just introduced for high-voltage SiC devices, development of reliable, and qualified ultra-high voltage package with low parasitics, excellent insulation material inside, and with robust thermal management is not ready yet to accommodate such high-voltage devices. Simultaneously, reliability of bipolar devices is still limited by the expansion of stacking faults that nucleate from the basal plane dislocations that poses another challenging threat to bipolar device development.

A variety of 10 kV class discrete SiC MOSFET chips and power modules have been demonstrated in the literature [6]–[18]. Ryu *et al.* [6] have developed a multizone junction termination process for 4H-SiC DMOSFETs. With a drift layer thickness of 115 μm (*n*-type doped to  $6 \times 10^{14} \text{ cm}^{-3}$ ), a blocking voltage of 10 kV, on-resistance of 236 mΩ·cm<sup>2</sup>, and a channel mobility of 14.5 cm<sup>2</sup>/Vs was achieved at room temperature [6]. Ryu *et al.* [8] have further scaled up the device area to higher current rating of 5 A and obtained a specific on-resistance of 111 mΩ·cm<sup>2</sup>. The

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same device was then used by Wang *et al.* [7] in a 370 W dc/dc boost-converter at 20 kHz. The short-circuit performance of the 10 kV chip has been investigated by Eni *et al.* with a dc-link voltage of 6 kV and a short-circuit survivability time of 8.6  $\mu$ s [10]. A 10 kV/120 A prototype SiC power module using 24 MOSFET dies and with 12 free-wheeling Schottky diodes was demonstrated by Das *et al.* [11] and Grider *et al.* [12] in a 1 MVA solid state power substation circuit. More recently, in-depth static and dynamic characterization of 10 kV/120 A power modules was presented by Lemmon *et al.* [16], [17] under various gate driving conditions. Parasitic elements, such as stray inductances of the power module, were extracted from the high-frequency impedance measurements [17]. Unfortunately, the static characteristics showed a large performance discrepancy between the upper and lower MOSFET switch in the half-bridge phase leg configuration, which indicates an unstable manufacturing process. Note that previously reported prototype modules based on 10 kV SiC MOSFETs [11]–[17] have used first-generation SiC MOSFET chips with separate free-wheeling diodes across the switch.

Recent development of the 10 kV SiC MOSFET chip has led to a new generation (a so-called third generation) of 10 kV SiC MOSFET dies with better performance as a result of improved material quality and stable manufacturing process control [18]. Commercial prototype samples of 10 kV SiC MOSFET power module based on the third generation MOSFET chips, were recently announced by CREE [19]. Compared to earlier generation of 10.0 kV SiC power modules [11]–[17], the new generation SiC MOSFET power module lacks external free-wheeling diodes (i.e., possess only inherent MOSFET body diode). Overall, this leads to a more compact layout design with smaller physical footprint of the package and with higher current rating capability. Moreover, these modules are in three parallel half-bridge phase leg configuration.

This paper addresses the thorough characterization work of the 10 kV, 100 A SiC MOSFET power modules based on the third-generation MOSFET dies using the inherent MOSFET body diode as a free-wheeling diode. The characterization results of the static performance, die/package process maturity, transient characteristics from the point of view of switching transients, switching energy losses, and also the power module short-circuit capability are presented in this paper. The main objective is to provide quantitative inputs for modeling parameters required to develop an accurate model for topology evaluation of realistic high-power converters in energy transmission systems and distribution networks [20], [21].

## II. EXPERIMENTAL SETUP

### A. Power Module Configuration

The investigated 10 kV SiC MOSFET power modules and gate drive unit were supplied from third party [19], [22] (i.e., prototype engineering samples) under collaborative agreement, however these are not visible in the commercial market yet. The power modules are assembled with a total of nine SiC MOSFET chips (i.e., three per switch position) placed in parallel to increase the current rating. The power modules are manufactured in three parallel half-bridge phase leg configuration (i.e., total of 18 SiC MOSFET dies), without separate free-wheeling diodes. The free-wheeling current is instead conducted by the MOSFET inherent body-diode, saving thus physical space in the module.

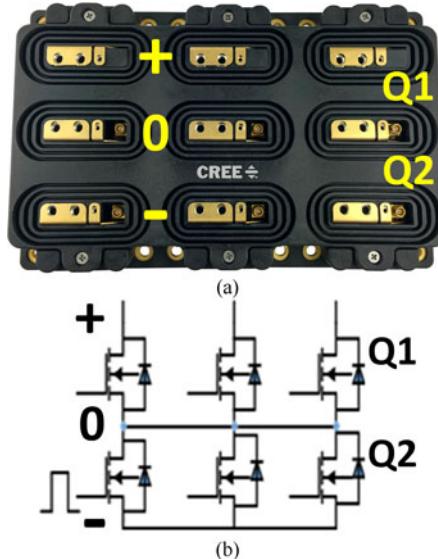


Fig. 1. Physical footprint (a) and electrical schematic (b) of the 10 kV 100 A SiC MOSFET power module [19].

TABLE I  
SiC MOSFET GATE DRIVER PARAMETERS [22]

Symbol	Parameter name	Value and Unit
$V_{\text{Drive}}$	Output voltage	+20 / -5 V
$V_{\text{DC}}$	Maximum supply voltage	32 V
$I_{\text{O}}$	Output peak current	$\pm 50$ A
$V_{\text{IOWM}}$	Working isolation voltage	8 kV
$R_{\text{G}}$	Output resistance	2 $\Omega$
$t_{\text{on}}$	Output rise time	250 ns
$t_{\text{off}}$	Output fall time	250 ns
$T_{\text{OP}}$	Operating temperature	-35 to 85 $^{\circ}\text{C}$

The electrical configuration of the power module is illustrated in the schematic diagram presented in Fig. 1, along with the physical footprint of the device ( $195 \times 125 \times 24$  mm).

A detailed view of the similar SiC MOSFET dies is presented in [18] where the SiC MOSFET die has a size of  $8.1 \times 8.1$  mm<sup>2</sup>, rated for 15 A and 10 kV blocking voltage capability. The total current capability of the power module is 100 A and the maximum junction temperature is 150  $^{\circ}\text{C}$ . The gate-source voltage is specified in the range of -10 to 20 V and the thermal resistance,  $R_{\text{TH},J-C}$ , is typically about 0.13  $^{\circ}\text{C}/\text{W}$  per switch position. The power module is designed for applications such as solid-state transformers, medium voltage drives, energy storage systems, and smart grid interconnections [19].

A gate driver unit for the inductive load switching test and short-circuit evaluation was used. The gate driver is primarily optimized for 10 kV SiC MOSFET power modules and well suited for high frequency and ultra-fast switching operations using a nominal gate resistance of 2.0  $\Omega$  [22]. Moreover, the gate driver has fiber optic control signals and overcurrent protection features. Table I summarizes the main properties of the gate driver.

### B. Test Setup

The SiC MOSFET static performance was measured with a Keysight B1505A power device analyzer/curve tracer, which is capable of measurements up to 10 kV and 1500 A. The

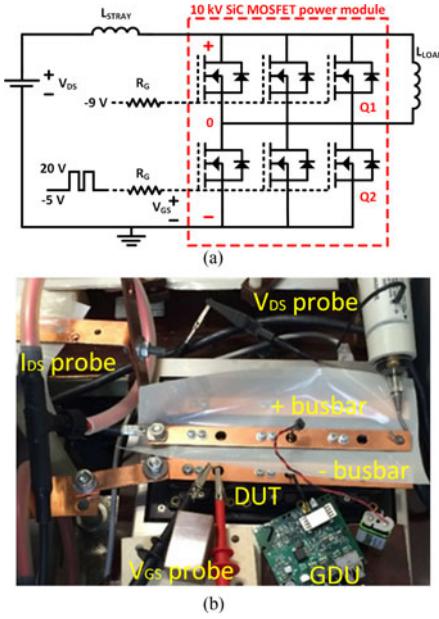


Fig. 2. (a) Electrical schematic of the chopper circuit with inductive load. (b) Experimental test setup for the SiC MOSFET dynamic characterization.

power module was heated with a Weller WHP 3000 hotplate. The dynamic characterization measurements were performed in a simple chopper circuit with inductive load, according to the electrical schematic in Fig. 2(a). The device under test were placed onto the Weller hotplate and connected to the test circuit terminals (i.e., dc+ busbar, dc- busbar, and midpoint), as presented in Fig. 2(b). The copper busbars were separated with a high insulation level mylar sheet between the busbars. The gate driver units were connected with shortest possible cable length. Since SiC devices switch faster, accurate considerations of metrology equipment (e.g., Rogowski coil, voltage probe, oscilloscope, etc.) and its calibration, are critical for accurately predicting the device transients as has been reported in [23]. In this circuit, the supply voltage was measured with a Tektronix's high-voltage probe (i.e., P6015A, 75 MHz, and 20 kV) and the gate voltage signal was measured with a Yokogawa 701926 differential voltage probe. The current conducted by the +/- busbar was measured with PEM Rogowski coils, CWT 15R. The measurements were recorded with a LeCroy LC564A 1 GHz oscilloscope. The test setup has variable power supply, inductive load, and a programmable sequence controller which gives thorough testing possibilities (i.e., generate arbitrary pulse sequence for a given inductive load to get required load current or vice versa, etc.).

### III. STATIC CHARACTERISTICS

#### A. I-V Characteristics

The extracted temperature dependent current-voltage characteristics ( $I_{DS} - V_{DS}$ ), transfer characteristics ( $I_{DS} - V_{GS}$ ), on-resistance ( $R_{on}$ ), and extracted threshold voltage are presented in Figs. 3–5, respectively. The power module on-state resistance is approximately 40 mΩ for a gate bias of 20 V at room temperature and shows a positive temperature coefficient.

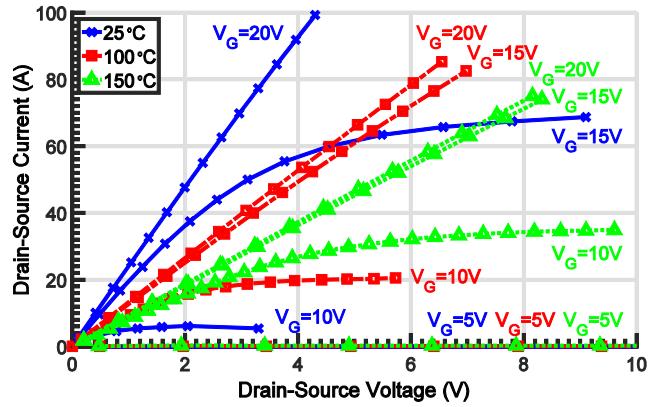


Fig. 3. SiC MOSFET drain-source current and drain-source voltage characteristics for different gate voltages at different temperatures.

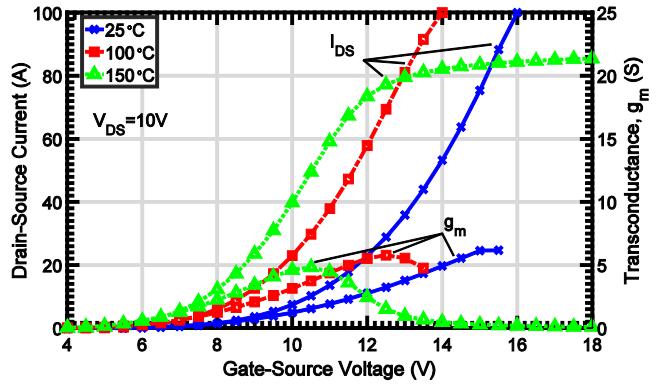


Fig. 4. Temperature-dependent transfer characteristics (e.g.,  $I_{DS}-V_{GS}$ ) and transconductance.

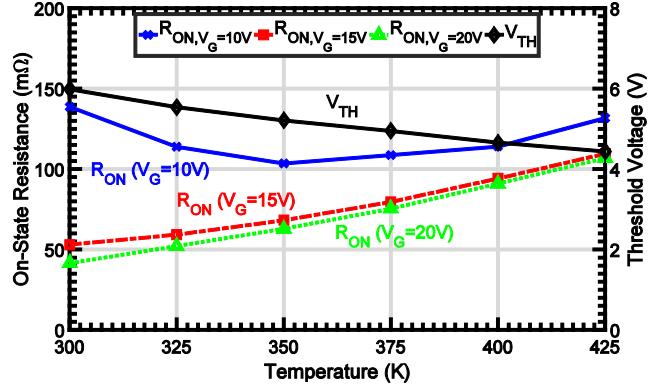


Fig. 5. SiC MOSFET threshold voltage and on-state resistance as function of temperature.

The threshold voltage, defined as the gate-source voltage required to obtain a 100 mA drain-source current at 20 V drain-source bias, decays with a slope of  $-12 \text{ mV}/\text{C}$  with temperature variation from 25 to 150 °C. Note that for a given oxide thickness and dielectric constant, the temperature coefficient of threshold voltage is primarily influenced by the presence of surface charge, surface potential, and trapped inversion electrons in the interface trap states at the SiC/SiO<sub>2</sub> interface [7], [24]. The drift region resistance is increasing for rising temperatures mainly because of more active lattice vibrations leads to increased phonon

scattering, which thereby decreases the bulk electron mobility [25], [26]. At lower gate voltages (e.g., 10 V), on-resistance first decreases with temperature and then increases at higher temperature similar to earlier observations for low voltage SiC MOSFETs [25], [27]. It is primarily due to limited amount of inversion channel charges at lower gate bias (i.e., channel is not fully open) and where the channel mobility increases with temperature due to reduced Coulomb scattering. At higher gate voltage (say 15 V, 20 V), the channel is fully open and the bulk mobility of carriers in the drift layer plays a dominant role that decreases with temperature and, hence, increase in the overall on-resistance is noticed.

The peak transconductance is in the range of 30 S at room temperature and shows a decreasing trend with increasing temperature as a result of bulk mobility drop in the drift part of the device structure.

### B. Third-Quadrant Characteristics

The SiC MOSFET power module lacks external free-wheeling diodes, which is typically used for Si IGBT power modules. The free-wheeling current is, therefore, instead managed by the MOSFET inherent body diode. Generally speaking, the most significant issue of body-diode utilization is associated to its reverse recovery behavior, which is linked to the presence of high concentrations of injected carriers stored in the drift part of the device. When the switch turns OFF, some carriers are swept away from the drift part of the device, resulting in a significant reverse recovery current that leads to additional switching loss in the complementary power switch of the half-bridge cell.

In third-quadrant operation and with varying gate bias from 0 to 5 V, the current flow is mostly through the body diode and where the knee voltage [e.g., -2.0 V at  $V_{GS} = 0.0$  V, see Fig. 6(a)] of the diode gradually decreases with increasing gate bias. On the other hand, when the gate of the power module is forward biased with 10 to 20 V, the inherent body-diode conduction is supported with a reverse conduction mostly through the MOSFET channel. In this reverse conduction case, the slope of the drain-source current (i.e., on-state resistance) is similar to the on-state resistance in the forward conduction state. Instead, with zero or negative bias at the gate terminal, the MOSFET channel is completely shut and the inherent body-diode conducts fully, Fig. 6(b). In the case of  $V_G = 0$  V, the extracted differential on-state resistance,  $R_{on,DIFF}$  is 45.0, 77.3, 89.4, and 101.7 mΩ for 25, 100, 125, and 150 °C, respectively, at the drain-source current of  $I_{DS} = 20$  A. Similarly for  $V_G = -5$  V, the measured  $R_{on,DIFF}$  is 44.3, 55.0, and 57.3 mΩ for 25, 100, and 125 °C, respectively. The positive temperature coefficient of the on-state resistance of the body diode is mainly governed by the reduction of bulk mobility for increased temperatures, similar to that of the on-resistance when the device is forward biased [26], [28]. On the other side, the built-in potential of the body diode is decreasing with increasing temperature at constant source-drain bias as a result of strong increase of the intrinsic carrier concentration with temperature [28]. For a fixed temperature, an increase of the knee voltage (i.e., source-drain voltage drop) for increasing reverse gate bias is observed consistent to earlier demonstration [28] meaning that the voltage required to overcome the internal junction barrier increases due to the increasing

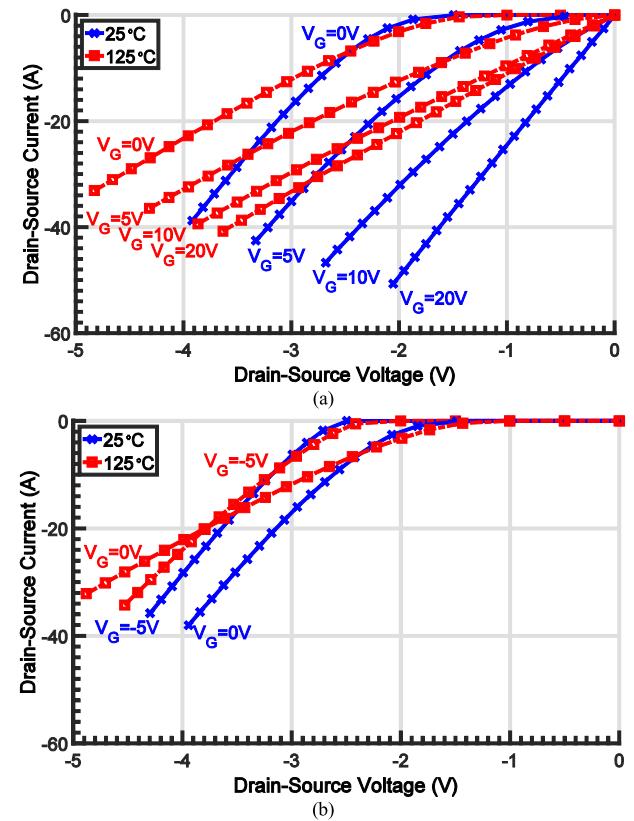


Fig. 6. SiC MOSFET power module reverse characteristics at different temperatures, (a) positive applied gate bias, (b) negative applied gate bias.

negative gate bias, as expected. In the case of 125 °C, note that after the crossover point of around  $V_{DS} = -4$  V and 20 A, the negatively biased ( $V_G = -5$  V) body diode shows less voltage drop than for the zero bias case ( $V_G = -0$  V). Furthermore, a larger negative gate voltage enables faster charge extraction process from the gate during turn-off, which reduces the turn-off time and, thereby, also the turn-off switching energy losses.

### C. Leakage Current Characteristics

As earlier said, the Keysight curve tracer (i.e., B1505A) was used to measure the SiC MOSFET leakage current and the blocking voltage characteristics. Without any bias at the gate terminal, the SiC MOSFET is capable of supporting a high drain voltage through the reverse-biased  $p$ -body and low doped  $n^-$  epitaxial layer junction. For high-voltage devices, most of the applied voltage is supported by the lightly doped  $n^-$ -drift layer where thicker and more lightly doped epitaxial layer supports higher breakdown voltage but with the cost of increased on-resistance. Thus, a low leakage current is a good indicator for the epitaxial growth and device process quality.

A comparative assessment of the off-state leakage current of the 10 kV SiC MOSFET power module with a 6.5 kV Si IGBT power module (ABB, 5SMX12M6501) [29] is illustrated in Fig. 7. Here, the SiC MOSFET is only stressed up to 9 kV due to precautionary reasons. The leakage current of the SiC MOSFET shows about one order of magnitude lower leakage current value than that of the Si IGBT counterpart. Note that the leakage current is strongly temperature dependent and presents

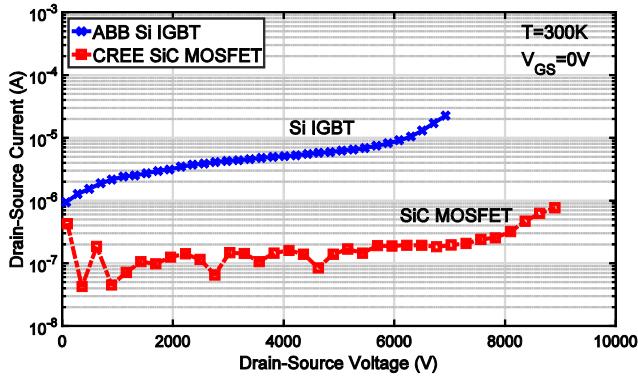


Fig. 7. Leakage current and blocking voltage characteristics of the 10 kV SiC MOSFET power module, compared to a 6.5 kV Si IGBT power module, [29].

one limiting factor for the maximum operating temperature usage of Si power modules [30]. The wide bandgap properties of the SiC material ensures minimal leakage current at reverse voltages, even at elevated temperatures. Hence, it offers good prerequisites to be used in high-temperature applications and under harsh environment conditions [31]–[33].

#### D. C–V Characteristics

The capacitive characteristics of the SiC MOSFET power module influences the switching performance. Primarily, the three parasitic capacitances associated to the three terminals of the device are gate-to-drain ( $C_{GD}$ ), drain-to-source ( $C_{DS}$ ) and gate-to-source ( $C_{GS}$ ) capacitances where device structure, package geometry, and their nonlinear dependence on the bias condition in fact define the switching transients. Note that the gate-drain capacitance comes from a series combination of a bias independent gate oxide capacitance ( $C_{OX}$ ) and a bias dependent depletion region capacitance. The decrease in capacitances with  $V_{DS}$  comes from the decrease in depletion capacitance as a result of widening of the depletion region with the increase of the drain-source voltage. Similarly, the drain-source capacitance is related to the drain-source depletion region width and the gate-source capacitance is merely constant with respect to  $V_{DS}$ .

During turn-on and turn-off switching transients, the drain-source capacitance,  $C_{DS}$ , and gate-drain capacitance,  $C_{GD}$ , are charged and discharged under the influence of the gate drive current. The extracted capacitance–voltage characteristics (e.g.,  $C_{DS} - V_{DS}$ ,  $C_{GD} - V_{DS}$ ,  $C_{GS} - V_{DS}$ ) at room temperature are presented in Fig. 8. The measurements were performed by using a measurement stimulus signal with a frequency of 100 kHz to avoid resonance interference which could arise between parasitic elements in the package and intrinsic capacitances within the semiconductor chip, which could occur in the MHz frequency range [17]. The gate-source capacitance,  $C_{GS}$ , is in principle constant at about 40 nF for increasing drain-source voltage, as expected. The  $C_{GD}$  and  $C_{DS}$  is in principle constant for drain-source voltages below 1 V and decreases for higher drain-source voltages. Furthermore, the basic bias dependent device capacitances such as  $C_{DS}$ ,  $C_{GD}$  and  $C_{GS}$  determine the input capacitance,  $C_{ISS}$ , the output capacitance,  $C_{OSS}$ , and the transfer capacitance,  $C_{RSS}$ , of the SiC MOSFET power module, as shown in Fig. 8(b) [34].

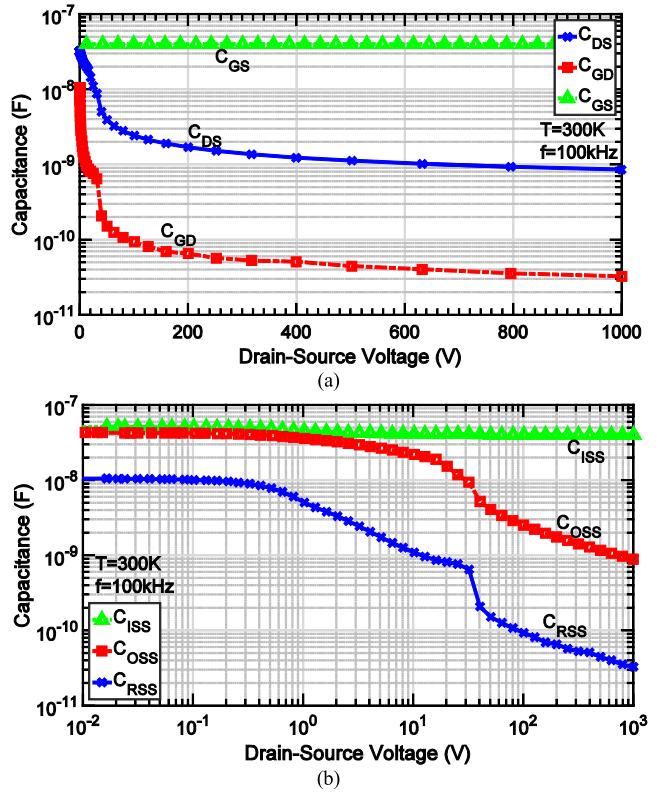


Fig. 8. Capacitance–voltage characteristics of the SiC MOSFET power module (a)  $C_{DS}-V_{DS}$ ,  $C_{GD}-V_{DS}$ ,  $C_{GS}-V_{DS}$  and (b)  $C_{ISS}-V_{DS}$ ,  $C_{OSS}-V_{DS}$ ,  $C_{RSS}-V_{DS}$ .

#### E. Process Control Evaluation

Since commercial SiC power modules are relatively new to the market, the spread in basic technological parameters, such as threshold voltage, peak transconductance, and on-state resistance may induce unwanted current unbalance when several power modules are placed in parallel for increased power rating. The major ingredients in the spread of these parameters are variations in the oxide thickness, variations in the doping concentration in different parts of the layer structure, and variations in the thickness of the layer structure besides geometrical spread of the metallic contacts. The current unbalance among several modules may further be enhanced due to variations in the parasitic elements (e.g., stray inductance) as a result of unsymmetrical placement of the dies in the package. As earlier said, previously reported static characterization (e.g.,  $I_{DS} - V_{DS}$ ,  $C-V$ ) [17], shows large discrepancies between the upper and lower SiC MOSFET switch, which may arise from the infancy manufacturing process of the first generation of the SiC MOSFET chip and the quality of the assembly process for the power module package.

The  $I_{DS} - V_{DS}$  and  $I_{DS} - V_{GS}$  characteristics of five power modules, equipped with a total of ten SiC MOSFET switches (i.e., third generation) were studied here to evaluate the SiC chip manufacturing process control. The  $I_{DS} - V_{DS}$  characteristics of three randomly selected power modules are presented in Fig. 9. At a gate bias of 15 V, a maximum spread of 6 A in the saturation region was observed from the same power module. Similarly, an overall difference of 20 A in the saturation

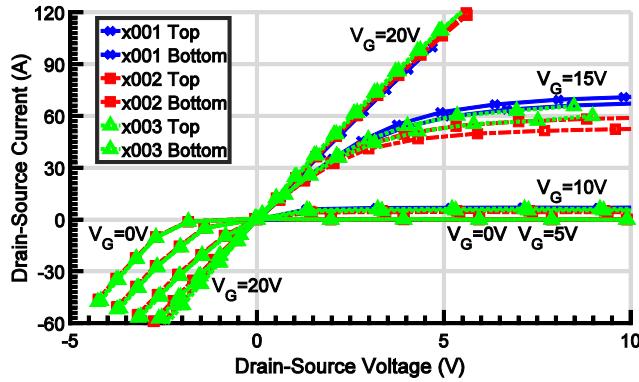


Fig. 9. Comparison of the forward and reverse  $I_{DS}$ - $V_{DS}$  characteristics of three SiC MOSFET power modules (six switches in total).

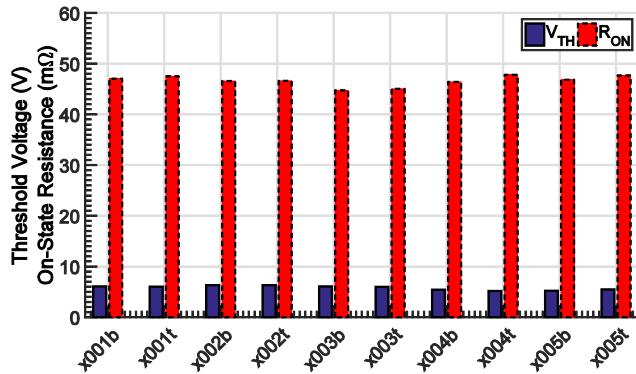


Fig. 10. Comparison of on-state resistance and threshold voltage of five SiC MOSFET power modules (ten switches in total).

region has been observed from all tested modules at 15 V gate bias, which is a significant improvement compared to the first-generation SiC MOSFET power module evaluated by Lemmon *et al.* [17]. Two important technological parameters (i.e.,  $V_{TH}$ ,  $R_{on}$ ) are extracted from the static characteristics of the power modules as illustrated in Fig. 10. An average on-resistance value of 46.6 mΩ with a standard deviation of  $\pm 0.98$  mΩ (i.e., 2.1%) is obtained from all tested power switches. Similarly, average value of the threshold voltage lies at 5.80 V with a standard deviation of  $\pm 0.42$  V (i.e., 7.2%). This implies that the manufacturing process of the third generation SiC MOSFET chip is rather mature and offers fair repeatability with minor deviations in these parameters. Similarly, the  $C$ - $V$  characteristics for two power modules is compared in Fig. 11. Here, very small differences in the  $C$ - $V$  characteristics indicates a rather mature semiconductor power module assembly process, in contrast to previously presented results [17].

#### IV. SWITCHING CHARACTERISTICS

##### A. Switching Waveforms

The SiC MOSFET dynamic characteristics were measured by using a simple chopper circuit with inductive load switching conditions. The oscilloscope view of the switching transients at 7 kV supply voltage and 2.8 mH inductive load is shown in Fig. 12. The top switch was negative biased with -9.0 V in order to always keep the top SiC MOSFET switch in the off-state and

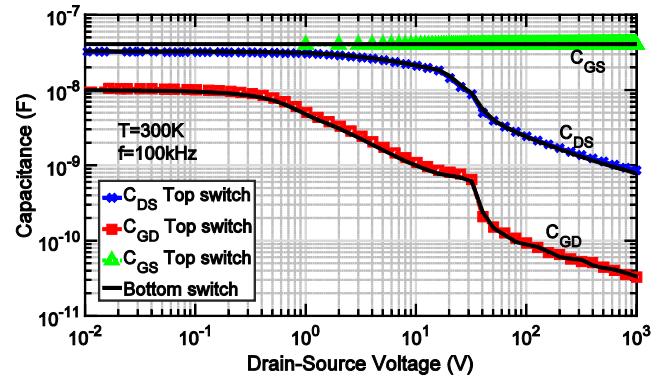


Fig. 11. Comparison of  $C$ - $V$  characteristics of the upper and lower switch in one SiC MOSFET power module.

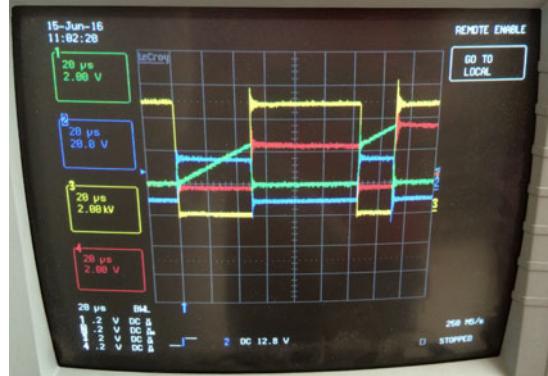


Fig. 12. Oscilloscope view of 7 kV switching transients.

simultaneously reduce the oscillations in the gate signal of the bottom switch (DUT). Note that the load inductance has been changed to vary the load current at a fixed supply voltage and for given pulse sequence. The full double pulse switching transient is presented in Fig. 13 along with zoomed in view of turn-on and turn-off waveforms. The power module gate bias was switched from -5 to 20 V with a constant external gate resistance of 2.0 Ω [22]. During turn ON, the drain-source current ( $di/dt$ ) with a slope of 1.07 kA/μs and gives a current overshoot transient of about 60 A, approximately 50%, before the current stabilizes at about 120 A. During turn-off, the drain-source current decreases with a slope of -0.71 kA/μs, while the drain-source voltage increases with a slope of 70.1 kV/μs which results in a 10–11% voltage overshoot before the voltage stabilizes at 7.0 kV. The SiC MOSFET turn-on and turn-off times and current/voltage slopes are compared to Si IGBT [29] values in Table II with varying drain-source current and supply voltages. First of all, the current slopes ( $di/dt$ ) are slightly steeper than that of previous reported 10 kV SiC MOSFET power modules [15]. For a given overall stray inductance in the loop, the current slopes are mainly governed by the gate resistance,  $R_G$  and the input capacitance,  $C_{ISS}$ . The tested power module is based on a later generation of SiC MOSFET chips and is using the inherent body-diode, which allows a more compact power module design. By that, the stray elements within the package are probably reduced, which allows the use of a lower gate resistance without significant overshoots, which enables switching with steeper slopes than before [15]. The SiC MOSFET current and voltage slopes are significantly steeper than

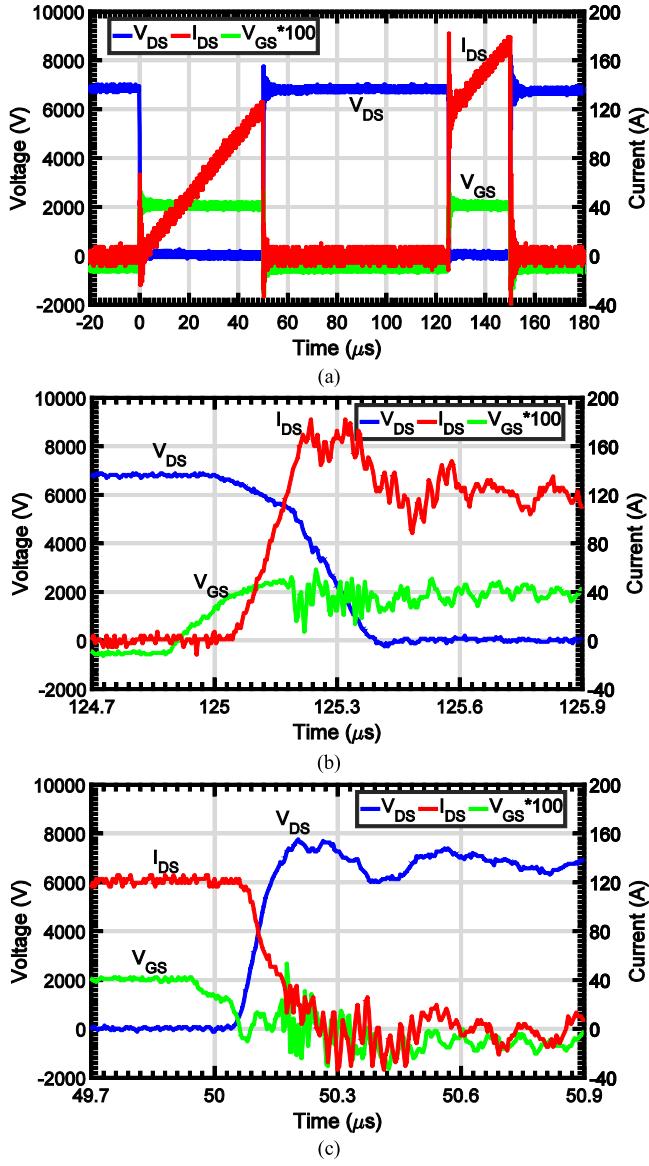


Fig. 13. SiC MOSFET switching transients at 7 kV supply voltage and room temperature, (a) full-double pulse cycle, zoomed-in view of (b) turn-on, and (c) turn-off switching transients.

TABLE II  
DRAIN-SOURCE CURRENT AND VOLTAGE RISE TIME AND FALL TIME  
COMPARISON, SiC MOSFET VERSUS Si IGBT

Operation conditions	Turn-on			Turn-off		
	$dI_{DS}/dt$ (kA/ $\mu$ s)	$dV_{DS}/dt$ (kV/ $\mu$ s)	$\tau_{on}$ ( $\mu$ s)	$dI_{DS}/dt$ (kA/ $\mu$ s)	$dV_{DS}/dt$ (kV/ $\mu$ s)	$\tau_{off}$ ( $\mu$ s)
<b>SiC MOSFET</b>						
7 kV, 121 A	1.07	-28.2	0.141	-0.71	70.1	0.148
6 kV, 104 A	1.02	-26.6	0.130	-0.66	60.5	0.145
5 kV, 87 A	0.99	-25.8	0.123	-0.56	43.4	0.140
4 kV, 69 A	0.93	-23.9	0.113	-0.48	35.0	0.128
3 kV, 53 A	0.80	-20.4	0.101	-0.39	24.8	0.118
<b>Si IGBT</b>						
3.5 kV, 60 A	0.48	-6.11	1.70	-0.34	1.24	3.83
3 kV, 40 A	0.24	-4.53	1.50	-0.05	0.95	4.57

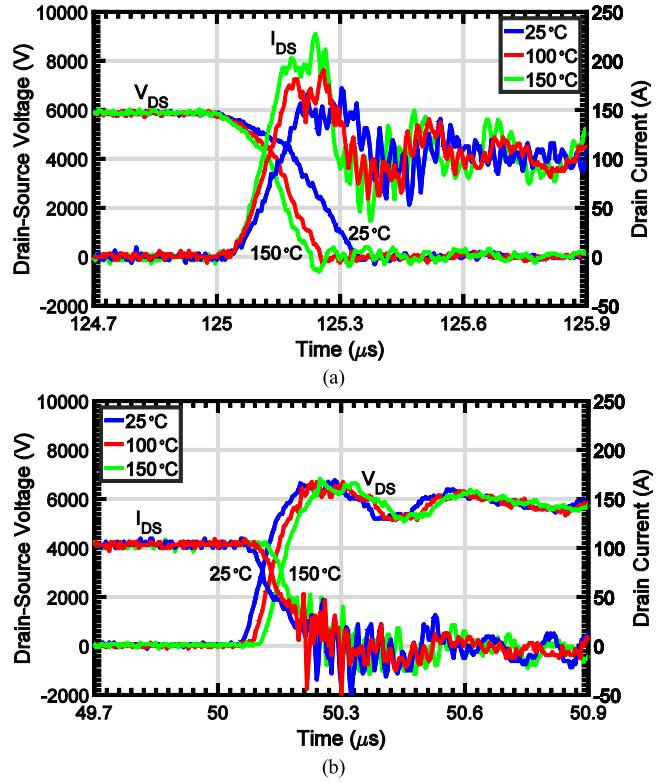


Fig. 14. (a) Turn-on and (b) turn-off switching transients for different temperatures.

that of the Si IGBT, consistent to previous measurements [35], [36]. This is primarily due to the lack of IGBT tail current that are observed in Si devices (i.e., unipolar SiC MOSFET versus bipolar Si IGBT) besides two times higher electron saturation velocity for SiC devices, leading to fast switching capabilities [1].

#### B. Switching Waveform Temperature Dependence

The temperature dependence of the SiC MOSFET switching transients are studied at the supply voltage of 6 kV, as shown in Fig. 14. In general, the SiC MOSFET turn-on current and voltage slopes are increasing with temperature, leading to shorter turn-on switching times. On the other hand, the turn-off current and voltage slopes are in principle constant but the turn-off characteristics demonstrates instead an increase of turn-off delay time with increasing temperature. In this case, there is mainly two parameters that governs the temperature dependency of the current and voltage slopes and delay times, namely the SiC MOSFET threshold voltage and transconductance parameter which in turn adjusts the Miller plateau voltage and the gate charge current and discharge current [34], [37], [38]. As observed in Fig. 14(b), the turn-off  $di/dt$  and  $dv/dt$  slopes are basically the same in this temperature range and the main change are only in the delay time, therefore the turn-off switching time and energy loss is only weakly temperature dependent.

The temperature dependency of the SiC MOSFET inherent body-diode reverse recovery is presented in Fig. 15. When the tested MOSFET switch (lower device) is in its off-state, the load current is free-wheeled in the inherent body-diode of the upper device. During the switching transition, the load current

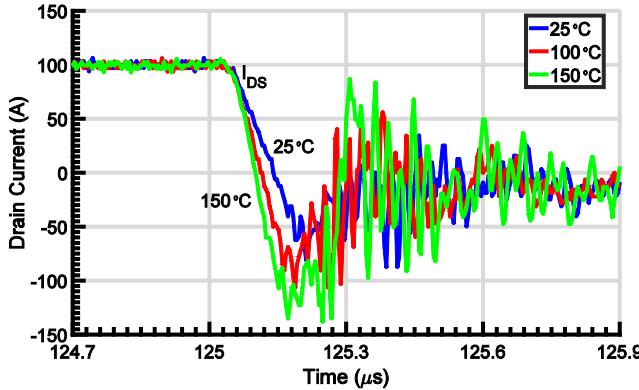


Fig. 15. Reverse recovery of the inherent body diode for different temperatures.

commutes to the lower device and the body-diode turns OFF. Since the body-diode is a bipolar charge carrier device, the minority carriers must be extracted or recombined before the device is completely turned-OFF. The removal of minority carriers causes the reverse recovery of the body diode. The amplitude of the reverse recovery current is increasing with temperature due to accumulated impact of temperature on intrinsic carrier concentration, more dopant ionization, and finally with increasing carrier lifetime, as expected.

## V. ENERGY LOSS EVALUATION

The energy losses are extracted from the switching transient characteristics during turn-on and turn-off phase of the double pulse sequence. With fixed load inductance of 2.8 mH, the switching energy loss for different supply voltages are presented in Fig. 16(a). The turn-on and turn-off losses at 7 kV and 121 A is 136 mJ and 42 mJ, respectively, at room temperature. The switching energy loss at constant supply voltage and for different drain-source currents are presented in Fig. 16(b). Here, the drain-source voltage is kept constant at 5 and 7 kV, and the load inductance is varied with constant double pulse sequence to get different drain-source currents, ranging from approximately 35 to 120 A. The turn-on and turn-off switching energy loss increases with increasing drain-source current, as expected. A larger drain-source current will require longer turn-on time and, therefore, more energy is dissipated during that period. The turn-off energy loss is increasing with a slower pace. The increasing energy loss is counteracted by the decrease of turn-off time which is caused by a higher Miller plateau that increases the gate discharge current and second a faster discharge of the free-wheeling diode capacitance, both caused by the increased drain-source current [38]. On the other hand, the switching energy loss for different temperatures follows a different trend, as presented in Fig. 16(c). Here, the turn-on losses decreases with temperature due to reduction in turn-on switching time. The turn-off switching energy losses are relatively unchanged and are approximately temperature independent.

Finally, the switching energy loss for the SiC MOSFET power module is compared to a 6.5 kV Si IGBT power module [29]. The two power modules are tested in the same test setup and under similar test conditions. The energy losses of the two power modules are compared in Table III. Here, the SiC MOSFET

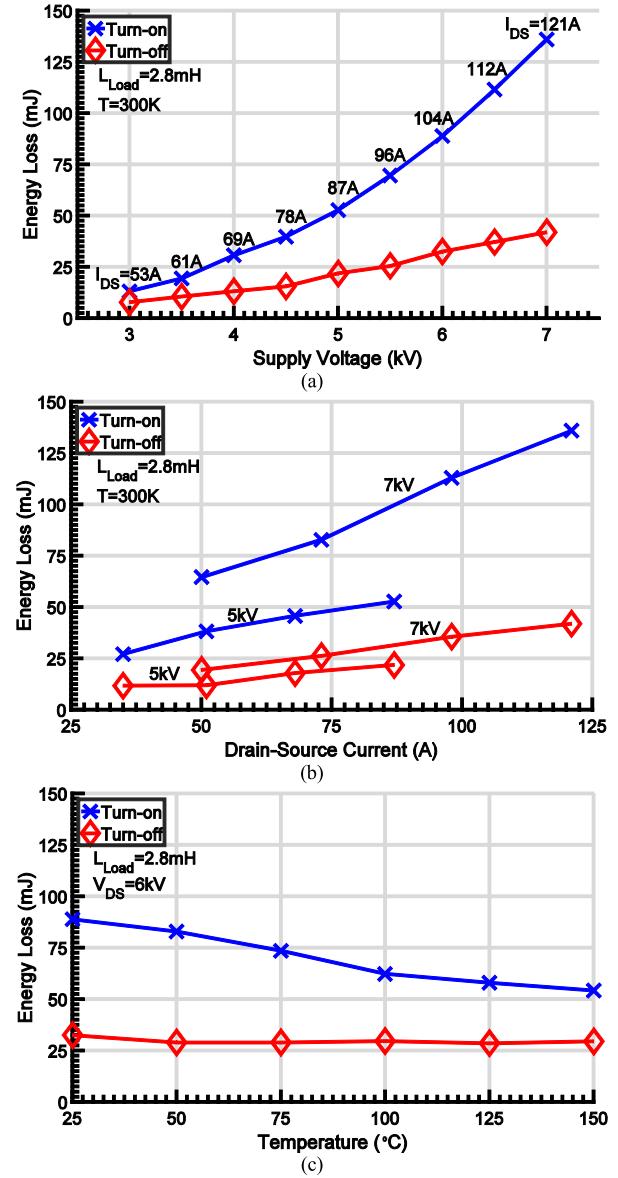


Fig. 16. SiC MOSFET power module switching energy losses under different operation conditions; (a) Supply voltage; (b) Drain-source current, and (c) Temperature.

TABLE III  
SWITCHING ENERGY LOSS COMPARISON, SiC MOSFET VERSUS Si IGBT

Operation conditions	$E_{\text{on}}$ (mJ)	$E_{\text{off}}$ (mJ)	$E_{\text{TOTAL}}$ (mJ)
SiC MOSFET 7 kV, 121 A	136	42	178
SiC MOSFET 3.5 kV, 61 A	19	11	30
SiC MOSFET 3.0 kV, 53 A	13	8	21
Si IGBT 3.5 kV, 60 A	279	335	614
Si IGBT 3.0 kV, 40 A	190	135	325

modules offer turn-on and turn-off energy loss of approximately 15 and 30 times lower than that of Si-IGBT counterpart, respectively at 3.5 kV indicating superior switching performance. Similarly, turn-on and turn-off energy loss were 15 and 17 times lower than that of Si-IGBT modules at 3.0 kV, respectively.

## VI. SHORT-CIRCUIT CAPABILITY

For power electronic converters, the short-circuit survivability time of power module provides important input for the design of short-circuit fault protection features. Here, the current slope ( $di/dt$ ) during short-circuit condition, short-circuit time, and the critical short-circuit energy are important parameters that determine the requirements of the protection circuit. Note that an undesirable short-circuit event can occur in a variety of ways in industrial environment prior to the intervention of the protection circuitry. Generally speaking short-circuit time under hard switching fault condition is provided by the device manufacturer and this stays mostly at  $10 \mu\text{s}$  for Si-based IGBTs [34]. As earlier said, SiC-based devices offer thinner drift region and, hence, reduced total volume (i.e., lower thermal mass) compared to Si-based devices with same ratings. For a given circuit parasitic condition and gate drivability, SiC-based devices, therefore, suffer from extremely fast temperature increase in a shorter time as a result of faster switching. This drastically reduces the device short-circuit capability of SiC MOSFETs [39]–[41]. Interestingly, for SiC-based devices, short-circuit time is still not visible in the datasheet for 1.2–1.7 kV commercial SiC MOSFETs.

The SiC MOSFET short-circuit failure phenomena are mainly temperature related, governed by the operating conditions (i.e., supply voltage, short-circuit current, and pulse time [39]). The dissipated energy rises device temperature. Due to this temperature rise, the total on-resistance increases, which leads to a reduction of the current magnitude after the current peak has been reached. If the applied pulse duration is long enough to reach the critical energy, the device will then enter into the failure mode. Different temperature related failure mechanisms have previously been addressed, such as significant increase of gate-source leakage current and, hence, reduction of gate-source voltage just before failure [42]–[44], significant increase of drain-source leakage current leading to thermal runaway [39], [41], [42] and sufficiently high surface temperature melting the aluminum bond wires [41], [43], [45]. A thorough investigation of short-circuit capability and avalanche roughness behavior of different commercial low power modules (i.e., 1.2–1.7 kV, 100–800 A) have been addressed in our recent work [41]. Short-circuit failure mechanism has been found out to be consistent to previous short-circuit measurements of discrete SiC MOSFETs and with physical analysis using technology computer-aided design (TCAD) software [42]. Furthermore, several short-circuit capability studies has previously been performed on 1.2–1.7 kV class discrete chips and power modules [40]–[42], [45]–[47] but only few short-circuit investigations has been observed for discrete devices in the 10 kV class. For example, Eni *et al.* recently evaluated the short-circuit robustness of a 10 kV discrete MOSFET chip, which resulted in a short circuit survivability time of  $8.6 \mu\text{s}$ , where the peak current reached to 266 A (26 times the rated current), with a gate bias switched to 18 V [10], [39]. Note that the situation is completely different where multiple chips are connected in parallel with varying stray inductance that induces different amount of stress inside the power module. The short circuit capability of the 10 kV SiC MOSFET power module was, therefore, investigated here.

The test was performed by excluding the load inductance from the test setup and shorting the top switch with a copper busbar. This test setup provides an overall parasitic inductance

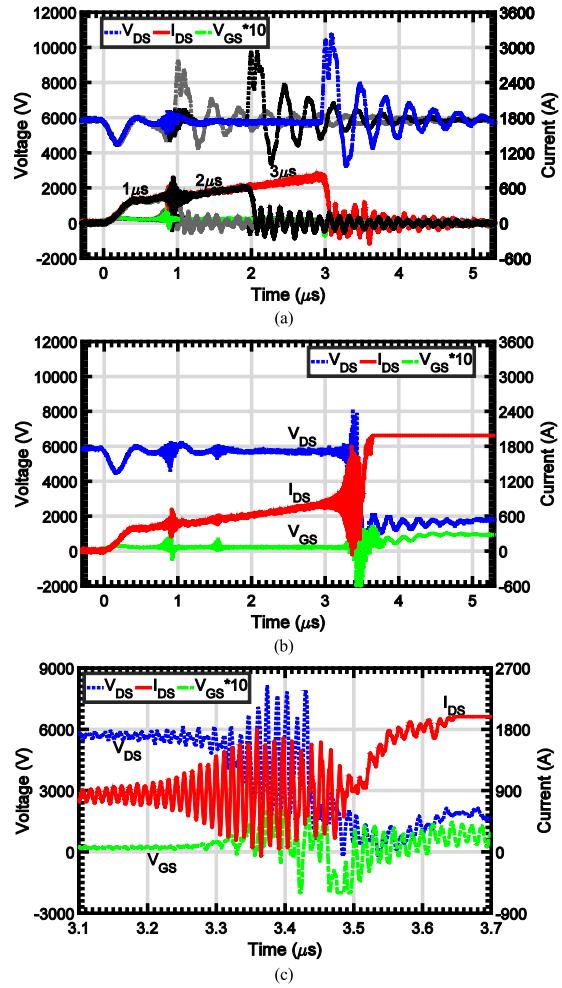


Fig. 17. Short-circuit performance of the SiC MOSFET power module; (a) Stepwise increase of the short-circuit pulse; (b) Short-circuit failure transient; (c) Zoomed-in view of the short-circuit failure transient.

of  $140 \text{ nH}$ , which is extracted from the drain-source current slope and the drain-source voltage overshoot at the short-circuit turn-off transition. For a given supply voltage in a short-circuit test, lower parasitic inductance induces higher current slope, whereas the junction temperature is still low [39], [40]. In our case, the parasitic inductance results in an initial short-circuit current slope ( $di/dt$ ) that is about four times higher than that of a 10 kV 10 A discrete chip tested at the same supply voltage of 6 kV [39]. In this test setup, the gate pulse duration was increased stepwise and the short-circuit current was monitored accordingly at a supply voltage of 6.0 kV, as seen in Fig. 17(a). The peak short-circuit current is limited by the maximum junction temperature rise and the parasitic elements in the test circuit and is determined by the slope of  $di/dt$  during the turn-on phase [39], [41]. Here, two current slopes are observed namely,  $4.4 \text{ kA}/\mu\text{s}$  during the first  $0.4 \mu\text{s}$  and, thereafter, with a lower rate of  $0.6 \text{ kA}/\mu\text{s}$ . The sharp transition between the two slopes is somewhat different from previous studies [39], [40], [45], [46]. This is primarily due to an inherent difference of short-circuit analysis of discrete chip (i.e., TO-247 type package) and present power module which is composed of three parallel half-bridge phase legs. This leads to a short-circuit phenomenon which is

rather difficult to explain in stand-alone format, since it presents a combination of several competing effects (i.e., module and circuit parasitics and several parallel dies). Initially, the short-circuit current rises with a steep slope, limited by the parasitic inductive elements in the circuit, whereas the temperature of the SiC MOSFET chip is increased due to the dissipated energy. Note that this temperature increase will result in reduction of the threshold voltage and increase of the channel mobility of electrons, which allows the drain-source current to increase even further, showing characteristics of a potentially thermally unstable device behavior [10]. Meanwhile, the short-circuit current continues to heat up the chip further after  $0.4 \mu\text{s}$  due to the transient temperature increase in the device and, thereby, the drain-source current will show a reduced current slope (i.e., significant increase of  $R_{\text{on}}$  with temperature rise due to decrease in the overall bulk mobility of the carrier once the channel is fully opened at higher gate biases [39], [41]).

This effect may be unified with unsymmetrical stray inductance in the current path within the power module where the same gate signal is used to turn-on the whole power module with three parallel half-bridge phase legs. Here, the devices that are farther away from the gate input terminal have larger stray inductance and, hence, induces lower current slope. Probably, the influence of variation of  $R_{\text{on}}$  with temperature is rather dominant than the variation of different stray inductances in the current path. This overall two slope behavior is similar to earlier experimental short-circuit observation of a 10 kV, 10 A discrete MOSFET [10], [39] as well as consistent to our recent device model of 10 kV SiC MOSFET power modules [48].

The SiC MOSFET reached a peak short-circuit current of approximately 900 A that is 9 times more than the rated current, as shown in Fig. 17(b). A zoomed-in view of the short-circuit failure transient is presented in Fig. 17(c). In this particular case, the module failed at  $3.5 \mu\text{s}$  as a result of thermal run away, where the maximum dissipated energy generated during the short-circuit pulse reached to approximately 11.0 J. Here, significant oscillations of the gate-source voltage, drain-source voltage, and current are visible before device failure. This leads to the apparently drop in the drain-source voltage with significant increase in the drain-source current (i.e., drain-source shorted). A turn-off of the short-circuit current generates a voltage across the parasitic components in the circuit, which in turn affects the device parasitic capacitances (e.g., Miller capacitance and  $C_{\text{GS}}$ ) and the gate voltage. In the case of large circuit parasitic components or fast switching, the generated gate voltage may reach the threshold and switch on the device, resulting in an oscillatory behavior [49]. The observed oscillatory phenomena (due to several dies in parallel that are under different amount of stress condition as a result of varying stray elements) is consistent to our previous short-circuit tests performed for 1.2 kV, 300 A SiC MOSFET power modules [47]. Similar oscillatory phenomena has also been noticed in Si-based IGBT modules with several dies in parallel [50].

## VII. CONCLUSION

In this paper, 10 kV 100 A SiC MOSFET power modules have been characterized. The SiC MOSFET power modules and the inherent body diodes have been assessed through several

experiments to extract the static and dynamic performance. The SiC MOSFET power module offers an on-state resistance of  $40 \text{ m}\Omega$ , with turn-on and turn-off energy losses of 89 mJ and 33 mJ, respectively, at 6.0 kV and 100 A. The SiC MOSFET performance, e.g., leakage current characteristics and switching energy losses have been compared to a 6.5 kV Si IGBT module. The SiC MOSFET shows superior performance compared to Si IGBT with one order of magnitude lower leakage current and with significantly lower switching energy losses, at room temperature. The short-circuit capability of the power modules have been investigated. The power modules withstood a  $3.5 \mu\text{s}$  short-circuit pulse duration with dissipated critical energy of 11 J before the device failure. The characterization results of this study provide valuable input for power electronic converter design and circuit level modeling of the 10 kV 100 A SiC MOSFET power module.

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