Instructions for Lab – 3

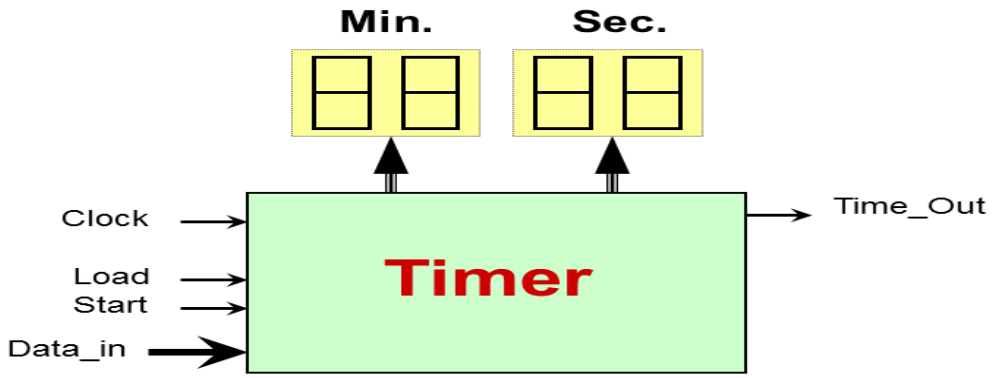
Wed. 25 March and Fri. 27 March (2-4 pm)

[3 Marks]

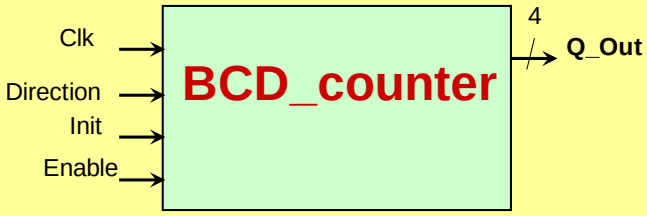
(This lab can be done by 2 students in one group).

The aim is to design a programmable timer, which can display minutes and seconds to record up to one hour (59 minutes and 59 seconds). The output of this timer is connected to 7-segment displays as shown below. Output signal ***Time_Out*** will change from '0' to '1' when the specified time elapsed (or in other words when the timer times out). The timer is initialized through ***Data_In*** input (which is 16 bits, representing 4 BCD digits and is used to indicate the amount of time in minutes using two BCD digits and seconds using the other two BCD digits). This value is used to indicate the specified amount of time when input ***Load*** is '1' (which is used to initialize the timer with the required time-out value). The timer starts working after the timeout value was initialized and when input ***Start*** changed from '0' to'1' (which should remain '1' until ***Time_Out*** changes from '0' to '1'). It counts every second from 0 until it reaches the **time out** initialized value and then output signal ***Time_Out*** will change from '0' to '1' (and remains '1' until next time the timer starts working using input ***Start***).

(For example, if you want to set the timer to time out after 36 minutes and 13 seconds, ***Data_In*** should have **0011 0110 0001 0011** when ***Load*** is '1' to initialize the timer. Then activate input ***Start*** to '1' to start the timer. After 36 minutes and 13 seconds output signal ***Time_Out*** will change from '0' to '1'. The count value is displayed on 7 segment displays).



The following Figure indicates a one-digit up/down BCD counter, which works when input ***Enable*** is '1' (otherwise the output is frozen at its current value). Input ***Init*** initializes the counter to 0 or 9 depending on the value of ***Direction*** input. (When ***Direction*** is '0', it is an up counter). (***Init***, ***Enable*** and ***Direction*** are **synchronous** inputs).



(a) Use the above one-digit BCD counter (which you designed in part 2 of lab2) **as a component** to design the **timer** (**without any changes to the VHDL code of the above one-digit BCD counter**). Note that the code for one-digit BCD counter should be **synthesizable**. You may make the connections in this system through using "schematic diagram design entry" in Quartus II (or write the required VHDL code for structural description of the system). The BCD to Seven Segment display converter code may be used from lecture notes if needed.

Input clock frequency of the timer (for Clock input) is 1 MHz.

(b) Write a testbench to test your code for the timer system and test it using ModelSim. (**Your design must be for the Clock input of 1 MHz** but you may use a faster clock in your testbench if it can be more convenient for testing and make the simulation time shorter).

(c) Use Quartus II tool to synthesize your code for different target devices: **CycloneVI** (EP4CE115) and **Stratix III** (let Quartus II automatically select the device for **Stratix III** families).

- How many logic elements (LE) are used for each target device?
- Can you determine the maximum clock frequency for each target device?

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The teaching assistants will help you in the lab to use Quartus II if you need help. (You may start in Quartus II with *creating a new project* and …)