Instructions for Lab – 2

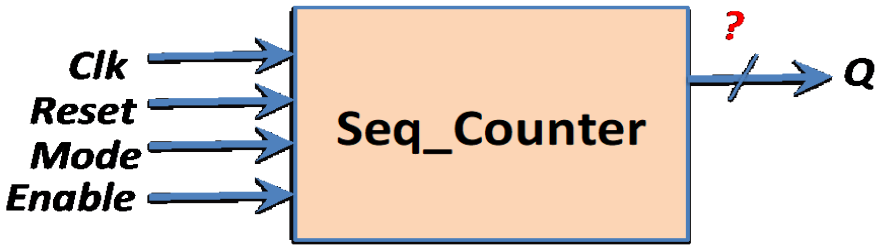
Wed. 18 March and Fri. 20 March (2 – 4 pm)

[3 Marks]

The aim of this lab is to practice behavioural and structural modelling of a digital system in VHDL, and use Intel (Altera) Quartus II tool.

1. Design a digital circuit as shown below, which has four *modes* of operation based on the value of the input signal ***Mode***. It generates sequence of numbers **periodically** on output ***Q*** depending on the value of the input signal ***Mode*** as shown below:

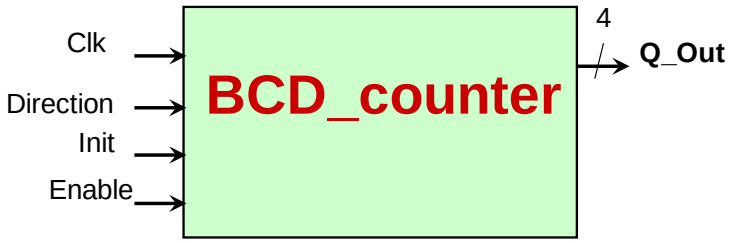
   Mode: "00" a down counter for odd numbers from 27 to 11
   Mode: "01" (3, -2, 8, 15, -1, 7, -14, 10, 1)
   Mode: "10" an up counter for numbers from 0 to 8
   Mode: "11" all bits of Q will be '1'



This circuit has ***asynchronous Reset*** input, which initializes it to the first counter value depending on the current value of ***Mode*** (except for ***Mode*** = "11"). When the ***Mode*** is changed, the counter starts counting in the new ***Mode*** in the next clock cycle, which counts from the first counter value (i.e from 3 if the ***Mode*** is changed to "01" from any other ***Mode***).
Input ***Enable*** is used to control the counter (and it is a ***synchronous*** input). When it is '1' the counter works otherwise its current value is unchanged.

(a) How many bits should be used for output ***Q***?
(b) Write the VHDL code to model this digital system.
(c) Write a proper testbench to test this system. The clock frequency of this system is 100 MHz. (Note that you may reuse the testbench given in part 1 of lab 1 and modify it where necessary).

2. (a) Write a **synthesizable** VHDL code for a one-digit up/down BCD counter, which works when input ***Enable*** is '1' (otherwise the output is frozen at its current value). Input ***Init*** initializes the counter to 0 or 9 depending on the value of ***Direction*** input. (When ***Direction*** is '0', it is an up counter). (***Init***, ***Enable*** and ***Direction*** are **synchronous** inputs).



(b) Write a test bench to test the functionality of your BCD counter.
(c) Use Quartus II tool to synthesize your code for target device Cyclone IV EP4CE115 and determine how many logic elements (LE) are used for your design.

3. Design a down counter, which counts either from 99 to 00 periodically *using the BCD counter designed in question 2 as component(s)*. The counter has **synchronous** inputs: active-high ***Reset***, which initializes the counter to 99 and the counter works when input ***Enable*** is '1'.

(a) Write the VHDL code for this counter ***using the one-digit BCD counter designed in question 2 as component(s) without any changes.***
Note: ***You may use the Quartus schematic diagram to make your system or simply write your VHDL code for the structural description.***
(b) Write a proper test bench to test this two-digit counter.

Reminder: **Summary of Simulation Steps (in ModelSim)**:

1. Change to the directory where your VHDL files are located.
2. Create a working library.
3. Compile your VHDL files.
4. Start Simulation (load the top level entity)
5. Add signals to the waveform viewer.
6. Perform the simulation for the required amount of time to test the circuit.