AW2028H 3 channel LED Driver with Audio Synchronization

FEATURES

- 3-channel constant current LED driver
  - 4- level I_{MAX} selections: 9/18/37/75mA
  - 256 current levels setting for each LED
  - Supports 256*256*256 color-mixing
- 256-level PWM dimming, 12-bit PWM resolution
- Audio synchronization, both brightness and color change with audio input
  - Analog audio input range: 0~2.8Vpp
  - Pre-amplifier with AGC gain adjustable from -12dB to +26dB
  - 8bit ADC and digital processing
  - Multiple audio-sync effects selectable
- Automatic breathing light with flexible pattern configuration and running mode
  - three independent pattern controllers
  - pulses repeating, multiple colors alternative
  - multiple patterns running successively or cyclically
- 400kHz fast I^2C interface , 1.8V ~ 3.3V
- Single power supply, 2.4V~5.5V
- Low power consumption
- FC-QFN8L 1.2mmx1.2mmx0.37mm package

GENERAL DESCRIPTION

AW2028H is three channels constant current LED driver with audio synchronization. The max output current is 4-level selectable among 9mA, 18mA, 37mA and 75mA. Each LED is 256 current levels configurable so as to achieve 256*256*256 color mixing. The 256-level dimming and 12 bits PWM resolution create fine and smooth dimming effect even in low brightness.

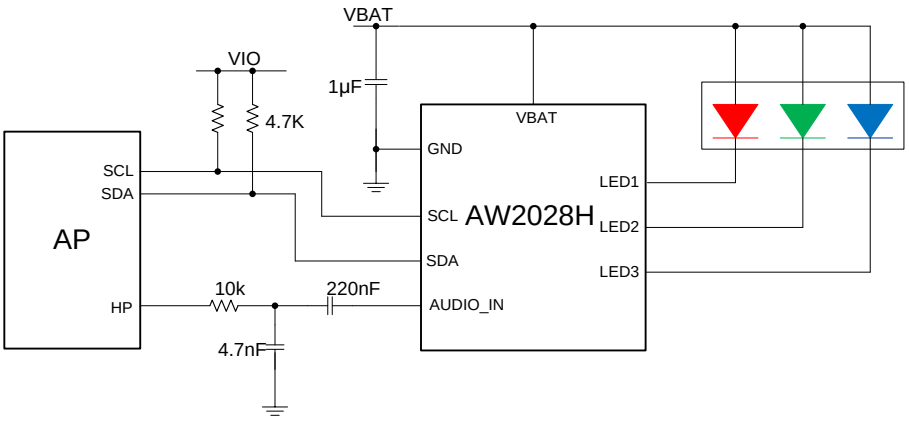
AW2028H integrates AGC preamplifier, ADC and digital filter to implement the audio synchronization, which allow user to synchronize the color LED with the audio input. The LED color can be programmed to switch periodically or vary directly with audio input signal. Multiple audio synchronization effects are configurable.

In shut down mode, AW2028H turn off all internal circuit and the consumption is less than 1μA. In standby mode, I^2C interface works and the consumption is less than 10μA.

The device requires only 2.4V~5.5V single power supply. An I^2C compatible interface in 400kHz fast mode is provided, the device address is 65h.

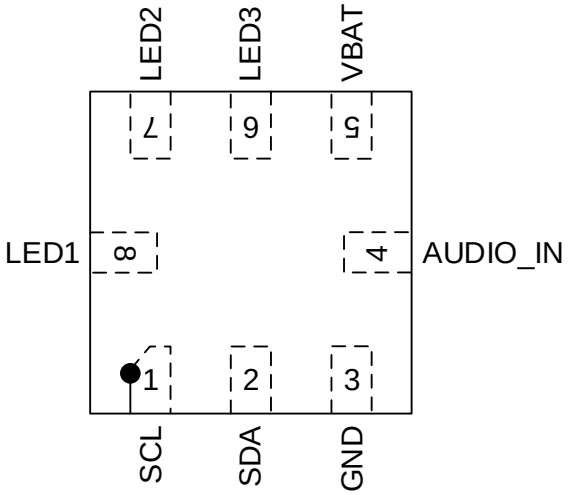
AW2028H is available in a ultra-thin 8 pin FC-QFN 1.2mmx1.2mmx0.37mm package.

TYPICAL APPLICATION CIRCUIT

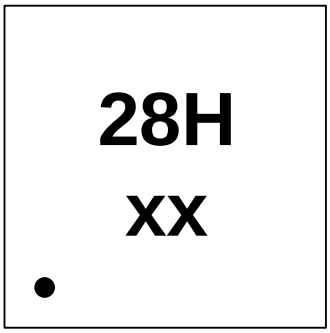


PIN CONFIGURATION AND TOP MARK

AW2028HFCR TOP VIEW



AW2028HFCR MARKING

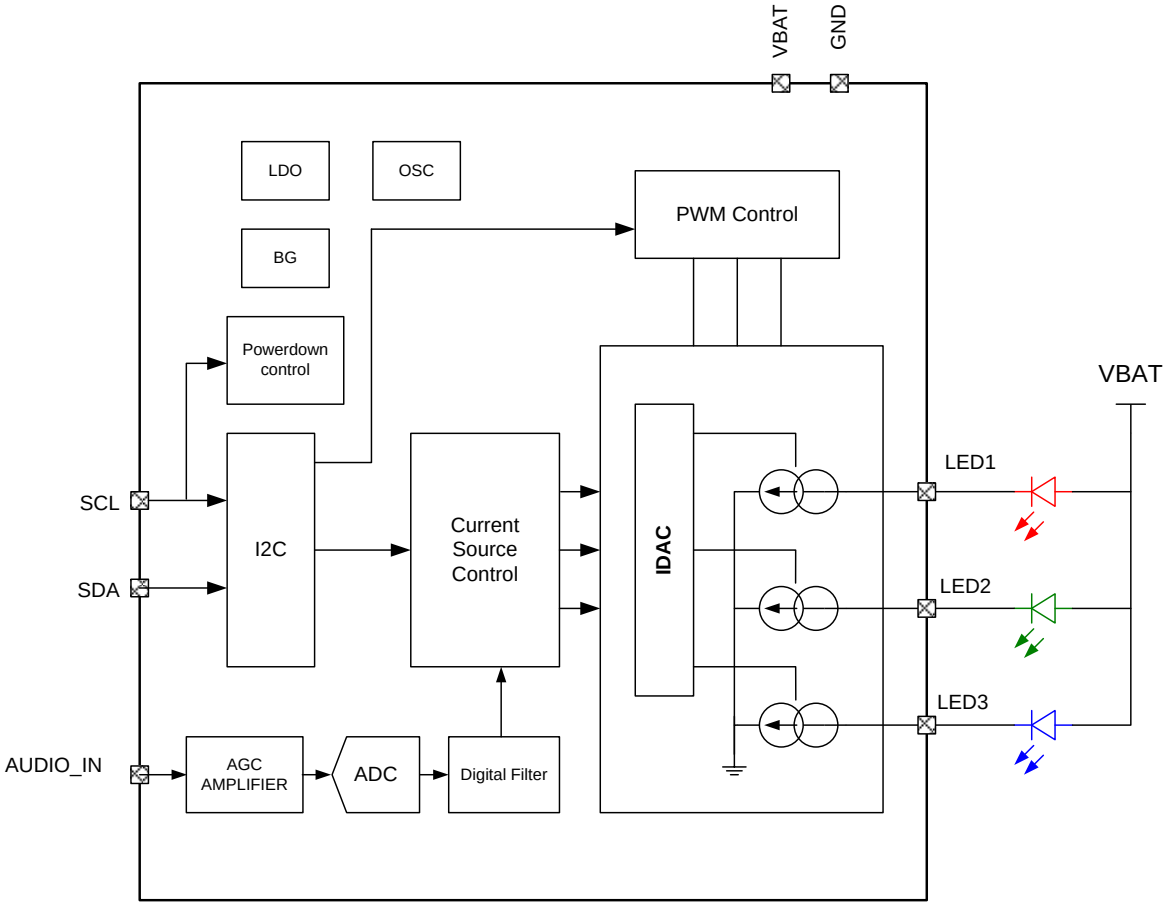


28H-AW2028HFCR
XX-Manufacture Data Code

PIN DEFINITION

No.	NAME	DESCRIPTION
1	SCL	Serial Clock Input for I^2C Interface
2	SDA	Serial Data I/O for I^2C Interface
3	GND	GND
4	AUDIO_IN	Analog Audio Signal Input
5	VBAT	Power Supply (2.4V-5.5V)
6	LED3	LED3 Cathode Driver, anode connected to VBAT
7	LED2	LED2 Cathode Driver, anode connected to VBAT
8	LED1	LED1 Cathode Driver, anode connected to VBAT

FUNCTIONAL BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUITS

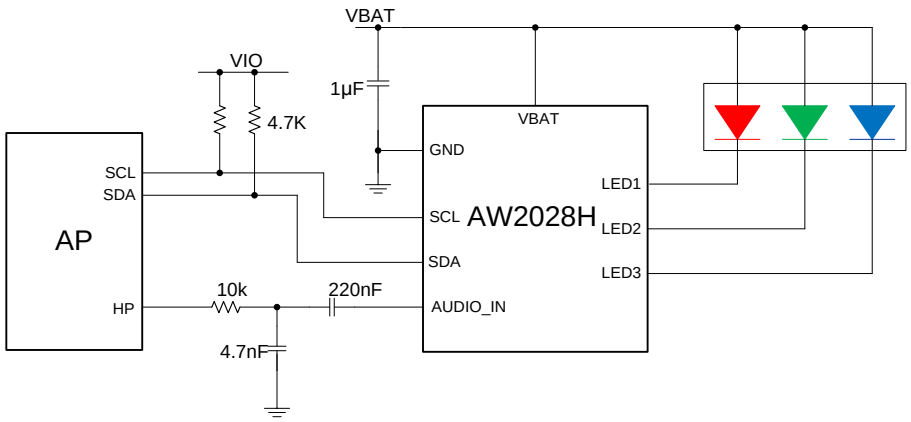


Figure 1. Typical Application Circuits

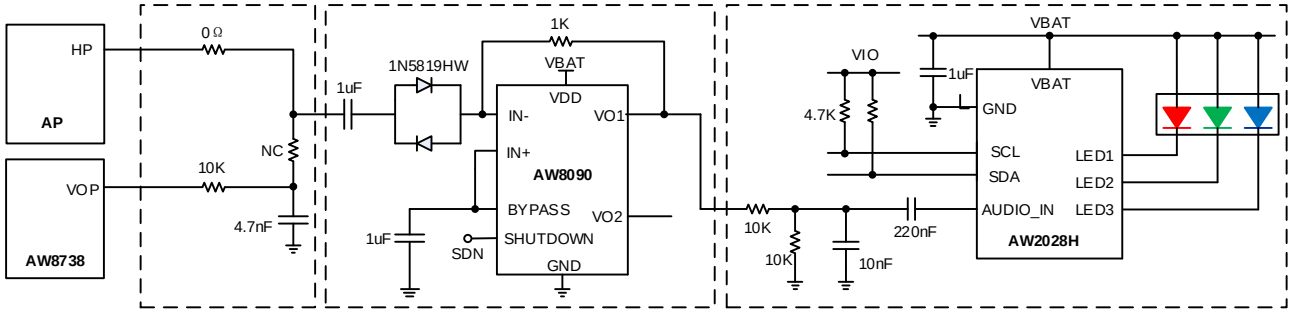
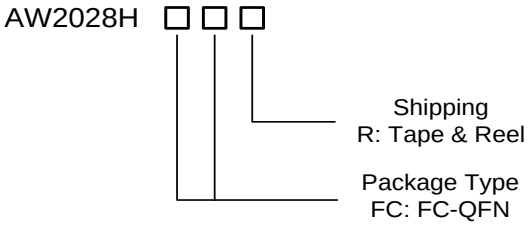


Figure 2. High Contrast Application Circuits

AW2028H has 2 kinds of application circuits. Figure 1 shows the typical application and the audio signal is from the headphone with RC low pass filter. Figure 2 shows the high contrast application. The audio signal is from audio power amplifier AW8738 or headphone with AW8090 exponential enlarging circuit. The LED light has higher contrast with level of audio amplitude.

ORDERING INFORMATION

Part Number	Temperature	Package	Marking	MSL Level	ROHS	Delivery Form
AW2028HFCR	-40℃～85℃	FC-QFN-8L 1.2mm×1.2mm ×0.37mm	28H XX	MSL3	ROHS+HF	3000 units/ Tape and Reel



ABSOLUTE MAXIMUM RATING(NOTE 1)

PARAMETERS		RANGE
Supply voltage range V_{BAT}		-0.3V to 6.0V
Input voltage range	SCL, SDA,	-0.3V to 6.0V
	AUDIO_IN	-0.3V to 6.0V
	LED1~LED3	-0.3V to 6.0V
Junction-to-ambient thermal resistance θ_{JA}		122℃/W
Operating free-air temperature range		-40℃ to 85℃
Maximum Junction temperature T_{JMAX}		150℃
Storage temperature T_{STG}		-55℃ to 125℃
Lead Temperature (Soldering 10 Seconds)		260℃
ESD(NOTE 2)		
HBM (human body model)		8000V
Latch-up		
Test Condition: JEDEC STANDARD NO.78B DECEMBER 2008		500mA

NOTE1: Conditions out of those ranges listed in "absolute maximum ratings" may cause permanent damages to the device. In spite of the limits above, functional operation conditions of the device should within the ranges listed in "recommended operating conditions". Exposure to absolute-maximum-rated conditions for prolonged periods may affect device reliability.

NOTE2: The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin. Test method: MIL-STD-883G Method 3015.7

ELECTRICAL CHARACTERISTICS

V_{BAT}=3.8V, T_A=25℃ for typical values (unless otherwise noted)

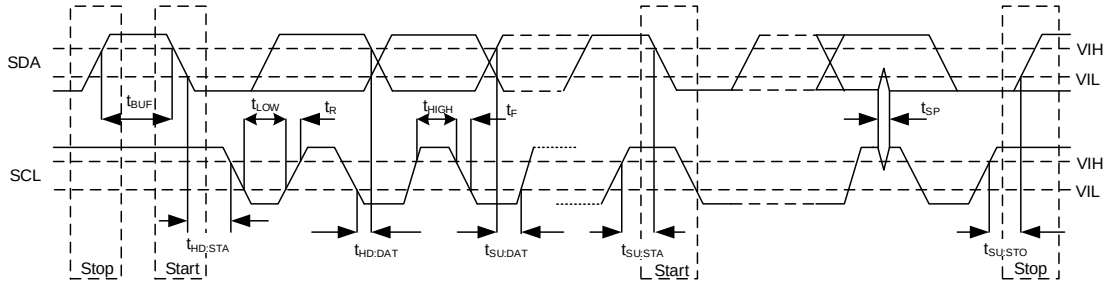
Symbol	Description	Test Conditions	Min	Typ	Max	Units
Power supply						
V_{BAT}	Input operating voltage	-	2.4		5.5	V
$I_{SHUTDOWN}$	Current in Shutdown mode	SCL/ SDA =0V (over 130ms)		0.1	1	μA
$I_{STANDBY}$	Current in Standby mode	SCL/SDA=1.8V		5	10	μA
I_Q	Quiescent Current in Active mode	register CHIPEN=1 all LED off		80	100	μA
I_{ACTIVE}	Current in Active mode	All channel set to 18mA		415		μA
		LED1 set to 18mA LED2,LED3 off		228		
		All channel set to 18mA T_{RISE}=2.1s,T_{ON}=0.04s T_{FALL}=2.1s, T_{OFF}=1s		150		
		LED1 set to 18mA LED2,LED3 off T_{RISE}=2.1s,T_{ON}=0.04s T_{FALL}=2.1s, T_{OFF}=1s		111		
Digital Logical Interface						
V_{IL}	Logic input low level	SDA,SCL			0.4	V
V_{IH}	Logic input high level	SDA,SCL	1.3			V
I_{IL}	Low level input current	SDA,SCL		5		nA
I_{IH}	High level input current	SDA,SCL		5		nA
V_{OL}	Logic output low level	SDA, I_{OUT}=3mA			0.4	V
I_L	Output leakage current	SDA open drain			1	nA
I^2C Interface						
F_{SCL}	I^2C-BUS clock frequency				400	kHz
$T_{Deglitch}$	SCL deglitch time			200		ns
	SDA deglitch time			250		ns
LED Driver						
I_{ACC}	Current accuracy	I_{LED}=37.3mA	-5%		+5%	mA
I_{MATCH}	Matching accuracy	I_{LED}=37.3mA	-5%		+5%	mA
V_{drop}	Dropout voltage	I_{LED}=37.3mA		60		mV

F_{PWM}	PWM frequency	Register PWM_F=0	115	122	128	Hz
		Register PWM_F=1	230	244	256	Hz

NOTE5：The value is tested in default configuration.

I²C INTERFACE TIMING

Parameter Name			Min	Typ	Max	Units
F_{SCL}	Interface Clock frequency				400	kHz
$T_{DEGLITCH}$	Deglitch time	SCL		200		ns
		SDA		250		ns
$T_{HD:STA}$	(Repeat-start) Start condition hold time		0.6			μs
T_{LOW}	Low level width of SCL		1.3			μs
T_{HIGH}	High level width of SCL		0.6			μs
$T_{SU:STA}$	(Repeat-start) Start condition setup time		0.6			μs
$T_{HD:DAT}$	Data hold time		0			μs
$T_{SU:DAT}$	Data setup time		0.1			μs
T_R	Rising time of SDA and SCL				0.3	μs
T_F	Falling time of SDA and SCL				0.3	μs
$T_{SU:STO}$	Stop condition setup time		0.6			μs
T_{BUF}	Time between start and stop condition		1.3			μs



FUNCTIONAL DESCRIPTION

POWER_ON RESET

AW2028H provides a power-on reset feature that is controlled by VBAT supply voltage. When the VBAT supply voltage rises from 0V to 2.4V, the internal LDO starts to work. The reset signal will be generated to perform a power-on reset operation, which will reset all control circuits and configuration register until the internal power voltage become stable.
The status bit STATUS.PUIS (register: 0x02 bit4) will be set to 1 when power-on reset operation occurs, which will be cleared by a read operation of STATUS register. Usually the STATUS.PUIS bit can be used to check whether a unexpected power-on event has taken place.

OPERATING MODE

In AW2028H, pin SCL provides power down control. There are three work modes available: Shut-down, Standby and Active mode.

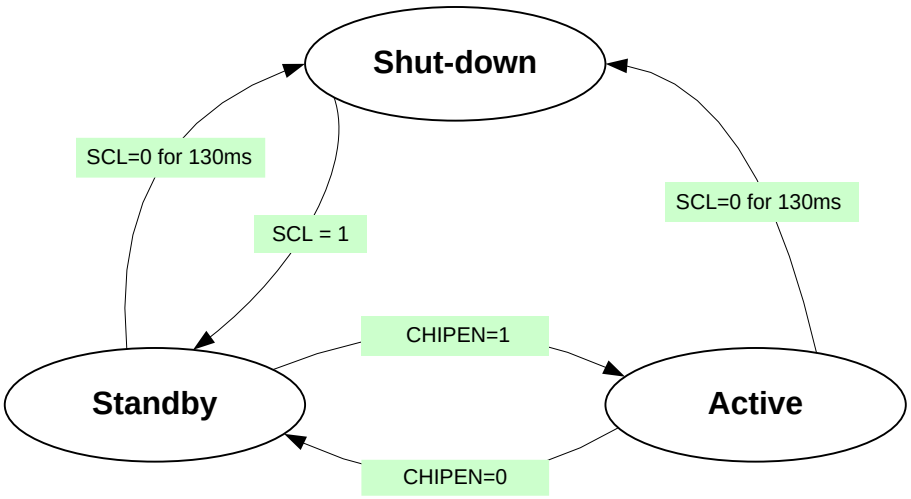


Figure 3. AW2028H operating mode transition

Shut-down Mode

AW2028H enters into the shut-down mode when SCL level is pulled to low for over 130ms (prevents system against wrong resets caused by electromagnetically influences)
In shut-down mode, AW2028H will reset all internal circuits and configuration register, all blocks inside AW2028H are basically switched off except the power on reset circuit and the SCL level detect circuit, and the current consumption is very low (< 1μA).

Standby Mode

AW2028H enters into standby mode when SCL level is pulled high from shut-down mode. In standby mode, only part of internal circuit can work, the OSC still keep closed so that there is not internal clock, the LDO operates in low power state, and the current consumption is less than 10μA.
In stand-by mode, the I^2C interface is accessible, but only registers RSTIDR and GCR can be operated.

Active mode

When bit CHIPEN of GCR register is set to 1, AW2028H enters into active mode.
In active mode, the internal OSC starts to work to provide clock signal. User can configure the device to produce the pre-defined pattern lighting effects in pattern mode, output the audio-related lighting effect in audio synchronization mode, or turn each LED on or off directly.
When PWM level is low in active mode, only the timer module works and the consumption is about 80uA(I_Q). So

the average consumption of active mode is every low.

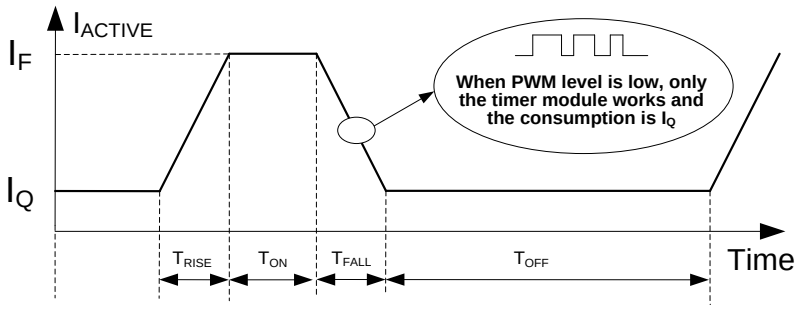


Figure 4. AW2028H consumption in active mode

Refer the following detailed formula (LED1/LED2/LED3 on)

$$I_{ACTIVE} = (I_F - I_Q) * \frac{(T_{RISE} + T_{FALL}) * 25\% + T_{ON}}{T_{RISE} + T_{ON} + T_{FALL} + T_{OFF}} + I_Q$$

IMAX	9mA	18mA	37mA	75mA
I_F	295μA	415μA	655μA	1140μA
I_Q	80μA	80μA	80μA	80μA

SOFTWARE RESET

Writing 0x55 to register RSTIDR (register: 0x00) via I²C interface will reset the AW2028H internal circuits and all configuration registers.

I²C INTERFACE

AW2028H supports the I²C serial bus and data transmission protocol in fast mode at 400 KHz. AW2028H operates as a slave on the I²C bus. Connections to the bus are made via the open-drain I/O pins SCL and SDA. The pull-up resistor can be selected in the range of 1k~10kΩ and the typical value is 4.7kΩ. AW2028H can support different high level (1.8V~3.3V) of this I²C interface.

Device Address

The I²C device address (7-bit) of AW2028H is 0x65, followed by the R/W bit (Read=1/Write=0).

Data Validation

When SCL is high level, SDA level must be constant. SDA can be changed only when SCL is low level.

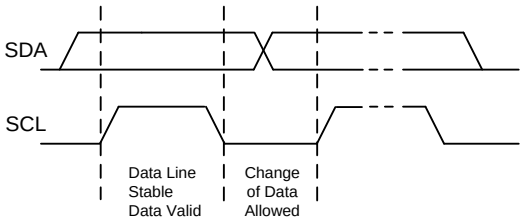


Figure 5. Data Validation Diagram

I2C Start/Stop

I²C start: SDA changes form high level to low level when SCL is high level.

I²C stop: SDA changes form low level to high level when SCL is high level.

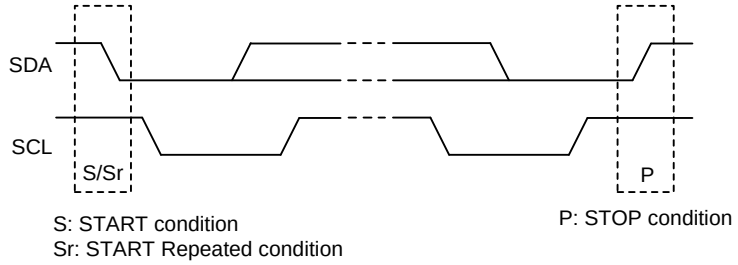


Figure 6. I²C Start/Stop Condition Timing

ACK (Acknowledgement)

ACK means the successful transfer of I²C bus data. After master sends 8bits data, SDA must be released; SDA is pulled to GND by slave device when slave acknowledges.

When master reads, slave device sends 8bit data, releases the SDA and waits for ACK from master. If ACK is send and I²C stop is not send by master, slave device sends the next data. If ACK is not send by master, slave device stops to send data and waits for I²C stop.

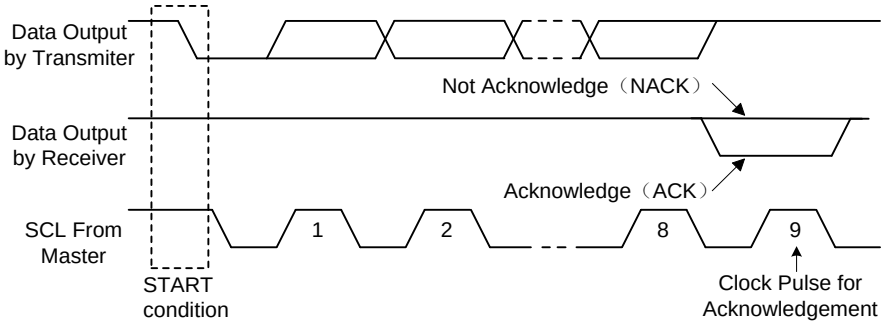


Figure 7. I²C ACK Timing

Write Cycle

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high state of the SCL and in the middle of a transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol allows a single data line to transfer both command/control information and data using the synchronous serial clock.

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow.

In a write process, the following steps should be followed:

a) Master device generates START condition. The "START" signal is generated by lowering the SDA signal while the SCL signal is high.

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master sends data byte to be written to the addressed register

g) Slave sends acknowledge signal

h) If master will send further data bytes the control register address will be incremented by one after acknowledge signal (repeat step 6, 7)

i) Master generates STOP condition to indicate write cycle end

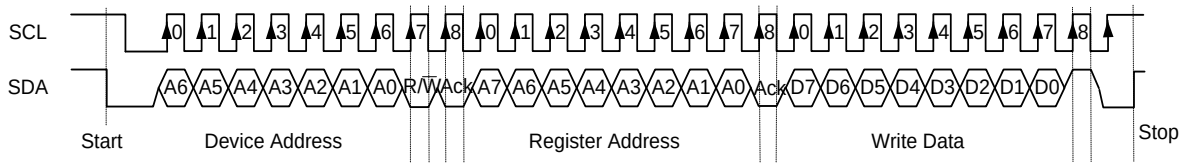


Figure 8. I²C Write Byte Cycle

Read Cycle

In a read cycle, the following steps should be followed:

a) Master device generates START condition

b) Master device sends slave address (7-bit) and the data direction bit (r/w = 0).

c) Slave device sends acknowledge signal if the slave address is correct.

d) Master sends control register address (8-bit)

e) Slave sends acknowledge signal

f) Master generates STOP condition followed with START condition or REPEAT START condition

g) Master device sends slave address (7-bit) and the data direction bit (r/w = 1).

h) Slave device sends acknowledge signal if the slave address is correct.

i) Slave sends data byte from addressed register.

j) If the master device sends acknowledge signal, the slave device will increase the control register address by one, then send the next data from the new addressed register.

k) If the master device generates STOP condition, the read cycle is ended.

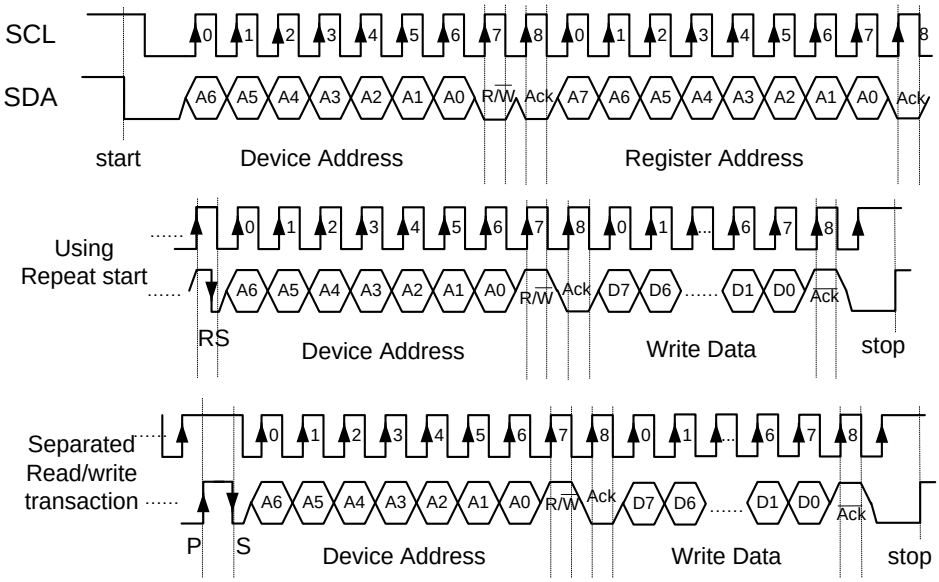


Figure 9. I²C Read Byte Cycle

LED DRIVER

AW2028H has three LED drivers to drive one RGB LED or three single-color LEDs. Each LED is driven by common-anode mode constant current source with duty cycle controlled by PWM. Both current and PWM can be configured via I²C interface.

LED Current

Globally, the maximum output current for three LEDs is 4-level selectable among 9mA, 18mA, 37mA and 75mA via register IMAX (register: 0x03). In general, IMAX is used to set the max brightness of LED output.
For each LED, there is 256 current levels configurable via 8-bit register groups ILEDx_y (x=1~3, y=1~4). So in RGB application it is possible to combine into 256x256x256 color-mixing schemes totally to achieve so-called true-color effect.
Generally the current level register is used to form specified LED color for RGB application. AW2028H has 4 groups pre-defined current registers capable of forming 4 dedicated colors in true-color pattern scheme, in which up to 4 pre-defined colors can be configured to represent 4 kinds of message, more than one color can flash one by one successively in the same pattern when it's necessary to transmit more than one messages.

PWM Dimming Control

In AW2028H, each LED current source is gated by a 256-level, 12bit resolution PWM signal to create fine dimming effect.
Each LED has a 8 bit PWM register PWMx (register: 0x1c, 0x1d, 0x1e) to control the duty cycle of constant current source. The ramp up and down are automatically implemented by PWM duty continuously adjusted to form a smooth LED current transition between ON and OFF state. The ramp slope, for rise and fall, are separately set via configuring the bit4~bit7 in pattern registers PATx_1 and PATx_2.
The ramping can be configured as linear and logarithmic curve by setting bit0~1 (PWMEXP) in register LEDCTR (register 0x08).

LED Control

Each LED of AW2028H can be independently configured to work or not via control bit LEDxEN.

- LEDxEN = 0, LEDx channel is disabled and no current output.
- LEDxEN = 1, LEDx channel is enabled to output lighting effect in different work mode.

By register configuration, AW2028H provides three types of LED control modes:

- *Audio synchronization*

The LED lighting effect is synchronized with the analog audio input on pin AUDIO_IN, there are several audio synchronization mode available for selection.

- *Pattern control mode.*
  AW2028H contains three independent pattern controller and three groups of pattern parameter register to generate user-defined breathing lighting effect. In RGB application, one pattern controller control 3 LED simultaneously to produce true-color breathing lighting, and three groups of pattern parameter can be executed successively or cyclically. For LED-independent application, three pattern controller are allocated to three different LEDs respectively, each operates with individual pattern parameter, user can start or stop each pattern independently.
- *Manual control mode.*
  User directly sets the brightness level of each LED by configuring relative current level register and PWM level register via I^2C interface. Usually it's recommended to modify the PWM level to set on or off. For each variation of PWM level register, the smoothly ramping effect is supported by setting FADE_IN bit and/or FADE_OUT bit in register LCFGx (x=1~3).

Audio Synchronization Mode

When AUDCTR.AUDEN (register: 0x40 bit0) is 1, the integrated audio synchronization block is enabled, which creates lighting effect depending on the audio signal amplitude connected to pin AUDIO_IN. The AS1, AS2, AS3 in AUDSEL (register:0x41, bit2~bit0) decide whether LEDx output the audio synchronous lighting, and AUDSEL must be set to 0x07 for color RGB LED application.

The block diagram of audio signal path is shown in the Figure below.

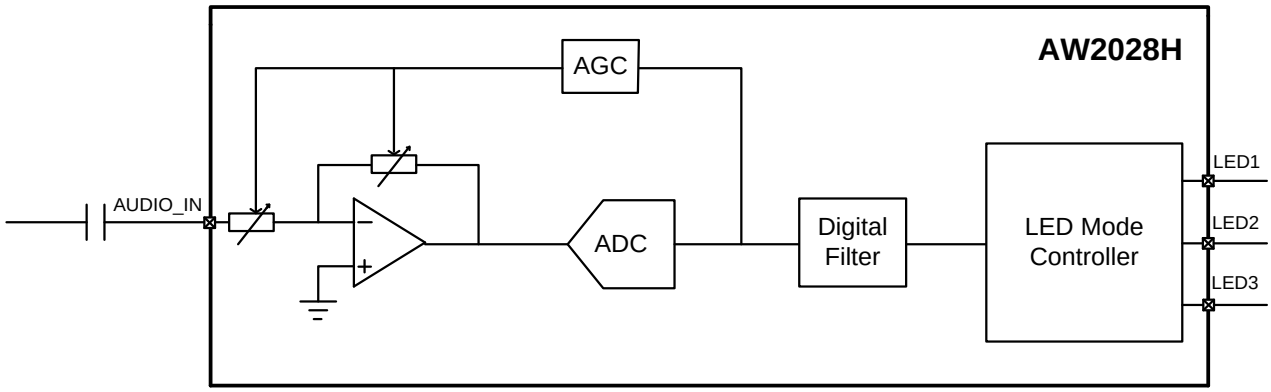


Figure 10. AW2028H Audio Synchronization Block

The analogue audio signal is coupled into the pin AUDIO_IN with an external DC blocking capacitor. The integrated audio pre-amplifier with automatic gain control (AGC) attenuates or amplifies the input signal to avoid clipping inside the signal processing path and furthermore increases the dynamic range of the signal when audio input signal is very small.

When AUDCTR.AGCEN (register: 0x40 bit1) is 0, AGC function is disable, the gain of pre-amplifier is defined by AGCGAIN (register: 0x43) register, and no auto gain adjustment involved. When bit AGCEN is set to 1, AGCGAIN register only determine the initial gain of pre-amplifier, and the actual gain will be dynamically adjusted in terms of the amplitude of analogue audio input signal. The AGC gain adjustment range is -12dB ~ +26dB, the GAINMAX register limits the maximum gain level that AGC can achieve, by default the value of GAIN_MAX is 31, corresponds to +26dB.

The integrated ADC transforms the buffered analogue audio signal into 8bit digital signal, which then is sent to digital filter for peak detection. The parameter of digital filter can be configured by register AUDFILT (register: 0x45), the attack time and release time of peak filter can be set independently.

The filtered data is finally sent to LED mode controller unit to create lighting effect. Various settings for the controller unit allow user to define different fancy blinking effect, the output of the controller directly links to the constant current sources of 3 LED output so as to implement brightness synchronized with audio.

In audio synchronization mode, the PWM level is used to specify the color output of RGB LED, which may be fixed, or varying periodically, or auto switching when input audio signal cross zero.

There are six types of audio synchronization effect can be selected by AUDCTR.SYNC_MD (register: 0x40, bit5~3).

1. SYNC_MD = 000, parallel mode with single color
   The brightness of all LED is controlled by audio signal amplitude simultaneously. The color is defined by register PWM1/PWM2/PWM3, 256*256*256 mixed colors is available via different register setting.
2. SYNC_MD = 001, parallel mode with color switch periodically
   The brightness of all LED is controlled by audio signal amplitude simultaneously. Six pre-defined colors (red – green – blue – yellow – cyan – purple) switch regularly and the switching period is configured by AUDTIM (register: 0x49).
3. SYNC_MD = 010, parallel mode with color switch on signal cross-zero
   The brightness of all LED is controlled by audio signal amplitude simultaneously. Six pre-defined colors switching occurs only when the audio input signal is cross zero.
4. SYNC_MD = 011, parallel mode with color switch both on timing and signal cross-zero
   The brightness of all LED is controlled by audio signal amplitude simultaneously. Six pre-defined colors switch when the audio signal is cross zero or the time defined by register AU_TIMER has passed by.
5. SYNC_MD = 100, Bar mode
   Three LEDs turn on successively and turn off reversely according to the audio signal amplitude.

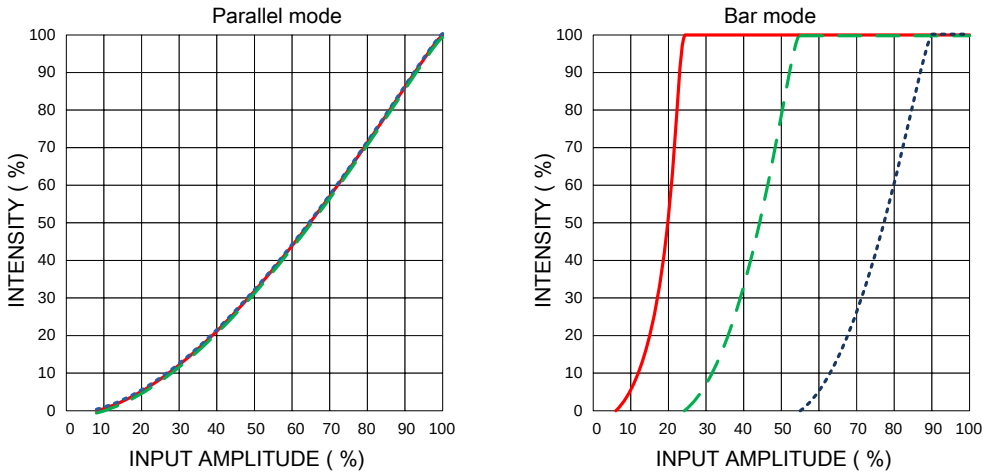


Figure 11. Parallel mode and Bar Mode of Audio synchronization

6. SYNC_MD = 101, RGB switch mode
   The color and brightness are both controlled by audio signal amplitude.

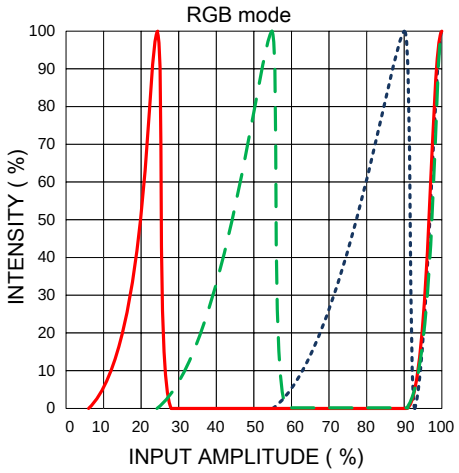


Figure 12. RGB Switch Mode of Audio synchronization

Pattern Control Mode

Breathing Lighting Control

When register bit LCFGx.LEDMD (register: 0x04, 0x05, 0x06 bit0) is set to 1, the corresponding LEDx operates in pattern mode.
User should configure the related pattern parameter registers according to actual timing requirements via I²C interface before starting pattern. The repeating times of pattern is configurable also, which may be 1~ 2048 or infinite according to setting of register PATx_T5 (x=1~4).

Single Pulse mode

Basically one pattern contains only one blink, it's called as single pulse mode. In single pulse mode, the pattern parameters includes delay time, rise time, on time, fall time, off time and repeat times can be set by corresponding configuration registers (PATx_T1~T5), The meanings of basic single-pulse pattern parameters are shown in Figure and table below.

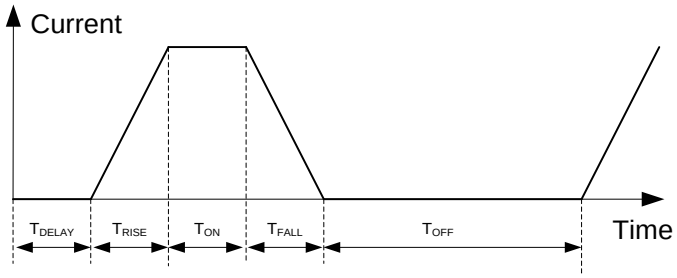


Figure 13. Basic single-pulse pattern parameter definition

Symbol	Parameters	Min	Typ	Max	Unit
T_{DELAY}	Delay time until pattern start	0		8	s
T_{RISE}	Rise time for dimming up	0		8	s
T_{ON}	On time	0.04		8	s
T_{FALL}	Fall time for dimming down	0		8	s
T_{OFF}	Off time	0.04		8	s

Multi-pulse mode

A serial fast pulse blinking can be used to transmit message different from that carried by single pulse. In multi-pulse mode, up to 4 pulses are allowed during one color blinking. Besides the basic timing parameter defined in single-pulse mode, there are 2 additional parameter need to be set:
The number of multi-pulse is defined by setting bit4~5 (MPULSE) in register PATx_T4 (register: 0x33/0x38/ 0x3D) , the actual blinking times is MPULSE+1.
The interval time between two adjacent pulses is defined by T_{SLOT}, bit5~7 in PATx_T4 (register: 0x32/0x37/0x3C).

Symbol	Parameter	Min	Typ	Max	Unit
T_{SLOT}	Pause time between multiple pulses	0		1.024	s

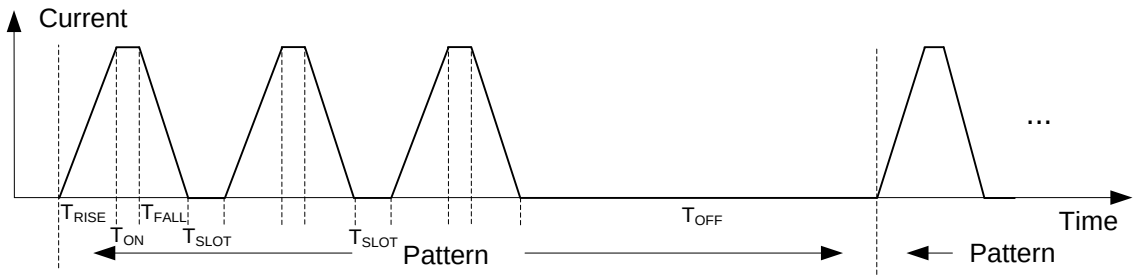


Figure 14. Multi-pulse pattern parameter definition

An example of multi-pulse pattern is shown below:

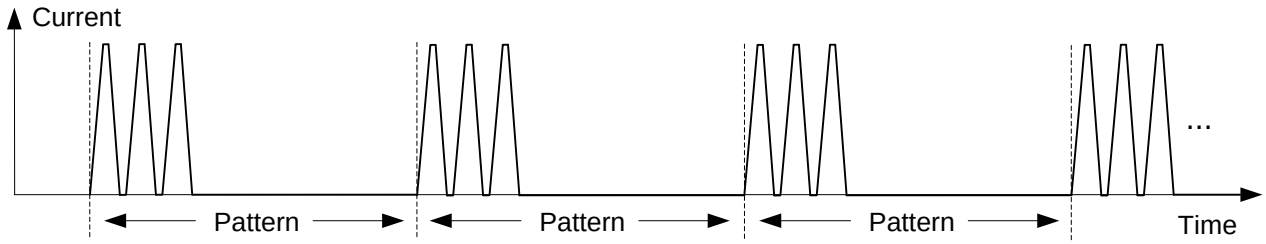


Figure 15. Multi-pulse pattern parameter definition

Multi-color mode

Blinking with multiple different colors is allowed in one pattern period in RGB LED application, if different color is expected to carry different message.

In AW2028H, the LED color is defined by LED current configure register ILEDx_y (x=1~3, y=1~4), there are 4 RGB current combination to generate 4 pre-defined colors for display. More than one of the 4 pre-defined colors can be chosen by setting CE1~CE4, bit0~bit3 in PATx_T4 (register:x32/0x37/0x3C), when CEx is set to 1, the color #x is allow to be displayed in current pattern.

If the color setting on CE1~CE4 is modified during current pattern is running, the updating of new color setting will not occur until present pattern period is over.

If both multi-pulse and multi-color is enabled simultaneously, every selected color will blink specified times before switching to another color, and the display order of color is always from color #1 to color #4.

An example of 4-color /single-pulse pattern is shown below, in which the CE1~CE4 are changed twice during pattern is running.

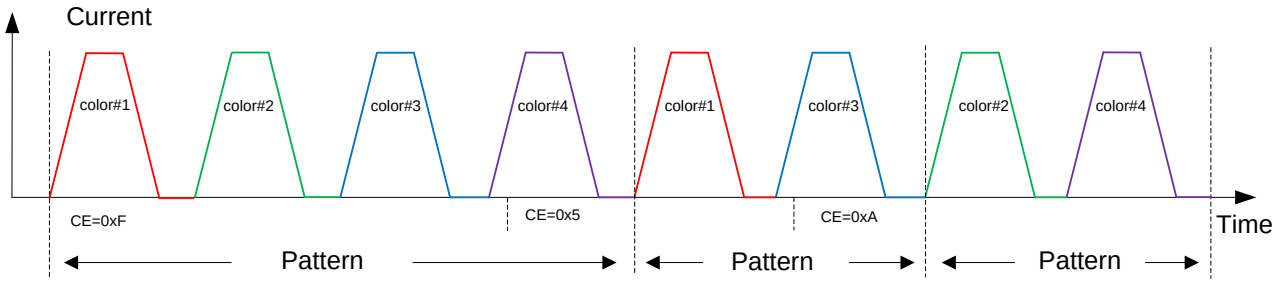


Figure 16. Example of multi-color mode and color scheme modification

True -color Breathing Lighting

In true-color breathing lighting application, the LEDMD, bit0 in LCFGx (register: 0x04, 0x05, 0x06), and the SYNC, bit3 in LEDCTR (register: 0x08 bit3) should be set to 1, three LED output share the same pattern controller to generate PWM dimming simultaneously. Multi-pulse, multi-color and multi-pattern modes are supported fully in this mode.

The RGB color is defined by LED current setting register ILEDx_y (x=1~3, y=1~4), there are 4 RGB current combination to generate 4 pre-defined color for display.

In true-color mode (SYNC=1), 3 groups of pattern timer parameters could be applied to defined 3 different breathing lighting effects, which can be executed successively or keep looping forever, without external processor involved to control every pattern switching. For each pattern, if PATx_T4.SW (register: 0x33, 0x38, 0x3E) is set to 1, the next pattern parameter will be loaded and started automatically after current pattern has finished.

The following table gives the current, pattern and the start/stop control source for each LED channel in true-color pattern mode.

Channel	Current Configuration Register	Pattern used	Pattern Start	Pattern Stop
LED1	ILED1_y	pattern #1, pattern #2, pattern #3	Write 1 to register PATRUN bit0	Write 1 to register PATRUN bit4
LED2	ILED2_y			
LED3	ILED3_y			

Note: Y=1~4, denotes 4 pre-defined color code (color #1, color #2, color #3 and color #4).

The following figure is an example of single pulse and color pattern repeating in true-color pattern mode.

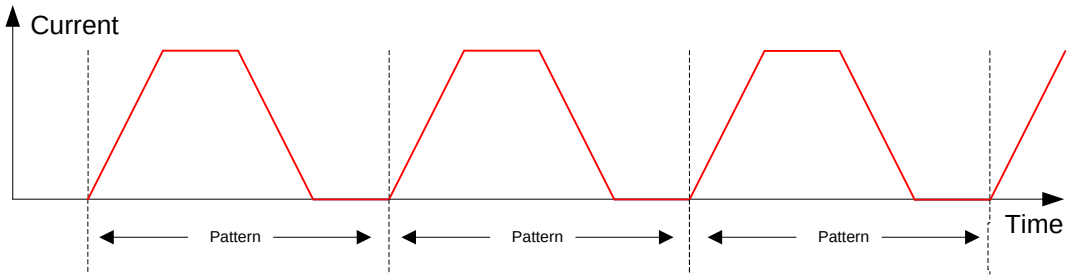


Figure 17. Example of single-pulse/single-color true-color pattern

The following figure is an example of multi pulse and multi color pattern repeating in true-color pattern mode.

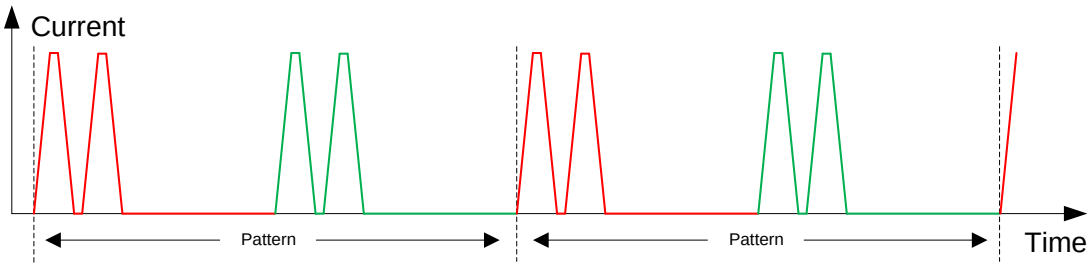


Figure 18. Example of multi-pulse/multi-color true-color pattern

The following figure is another example of three patterns running successively in true-color pattern mode.

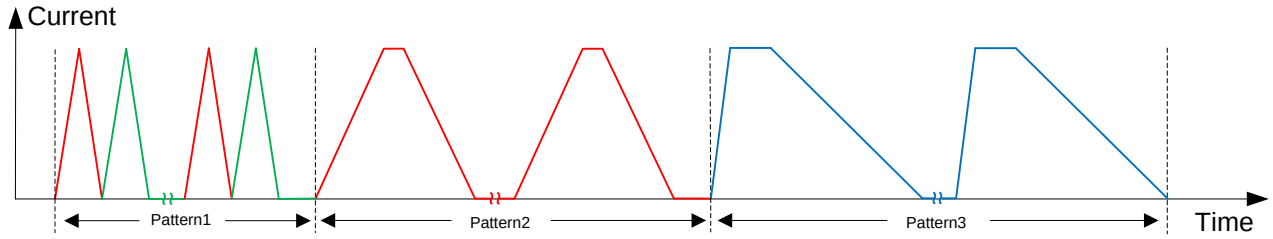


Figure 19. Example of 3 patterns running successively in true-color mode

Individual Breathing Lighting

In some application where three LED need blinking individually. When register bit LCFGx.LEDMD (register: 0x04, 0x05, 0x06 bit0) is set to 1, the corresponding LEDx operates in pattern mode. If register bit LEDCTR.SYNC (register: 0x08 bit3) is 0, all pattern run in individually. In this mode, the 3 internal pattern controllers and 3 groups of pattern parameters are distributed to 3 LED channel respectively. Each LED can be controlled independently to blink according to its own pattern definition.

In this mode, multi-pulse pattern is supported, but multi-color is not supported, the bits CE1~CE4 in register PATx_T4 are ignored. Only registers ILEDx_1 is active for LED current setting, the other register including ILEDx_2, ILEDx_3 and ILEDx_4 are all useless.

The following table gives the current, pattern parameter and the start/stop control source selection for each LED channel in individual breathing lighting mode.

Channel	Current Setting Register	Pattern used	Pattern Start	Pattern Stop
LED1	ILED1_1 (register: 0x10)	pattern #1	write 1 to PATRUN bit0	write 1 to PATRUN bit4
LED2	ILED2_1 (register: 0x11)	pattern #2	write 1 to PATRUN bit1	write 1 to PATRUN bit5
LED3	ILED3_1 (register: 0x12)	pattern #3	write 1 to PATRUN bit2	write 1 to PATRUN bit6

The following figure shows an example of 3 patterns run individually with different pattern parameters.

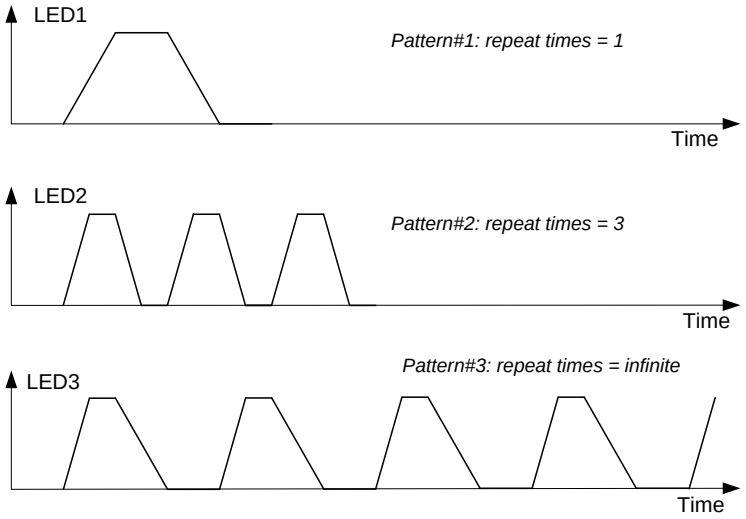


Figure 20. Example of Individual Pattern Mode

Manual Control Mode

When control bit LCFGx.LEDMD (register: 0x04, 0x05, 0x06 bit0) is set to 0, the corresponding LEDx is work in manual control mode.
In manual control mode, the LED lighting effects including color-mixed and brightness is directly configured by setting current/ PWM level register via I^2C interface.
When LEDCTR.SYNC (register: 0x08, bit3) is set to 0, three LED are controlled individually, the PWM level and current for each is defined by PWM1/PWM2/PWM3 (register: 0x1C/0x1D/0x1E) and ILEDx_1 (register 0x10/0x11/0x12) respectively.
When LEDCTR.SYNC (register: 0x08, bit3) is set to 1, the output currents of three LED are defined by register ILEDx_1 respectively, but their PWM level are determined commonly by register PWM1. So user can change the brightness of all LED simultaneously by modifying the value of register PWM1 only.

Channel	Current	Brightness		T_{RISE} and T_{FALL} time	
		SYNC=0	SYNC=1	SYNC=0	SYNC=1
LED1	ILED1_1	PWM1	PWM1	PAT1_T1/T2	PAT1_T1/T2
LED2	ILED2_1	PWM2		PAT2_T1/T2	
LED3	ILED3_1	PWM3		PAT3_T1/T2	

In manual control mode, auto dimming is supported. If LCFGx.FADE_OUT (register: 0x04, 0x05 0x06 bit2) is set to 1, automatic fade-out is enabled. If LCFGx.FADE_IN (register: 0x04, 0x05, 0x06 bit2) is set to 1, automatic fade-in is enabled. If a new value is set on PWMx register and auto dimming is enabled, the brightness of LED output ramp up/down smoothly, with its T_{RISE} and T_{FALL} time defined by corresponding pattern configuration (PATx_T1 and PATx_T2).

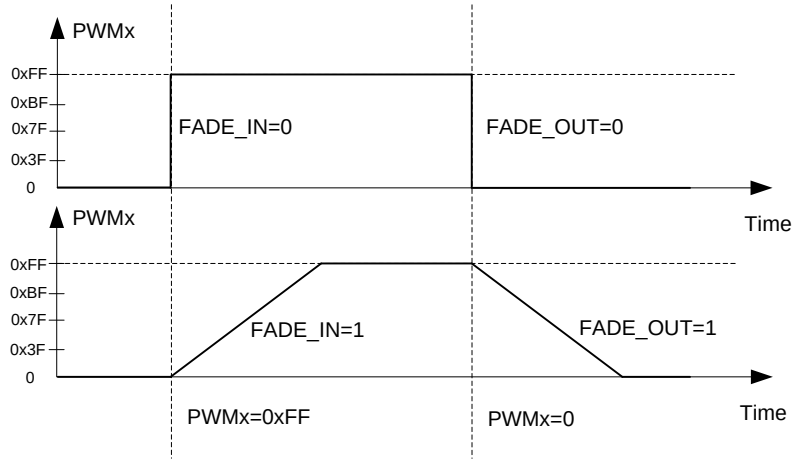


Figure 21. Manual Control Mode

REGISTER DESCRIPTION

REGISTER LIST

Addr (Hex)	Name	W/R	7	6	5	4	3	2	1	0
00	RSTIDR	R	1	0	1	1	0	0	0	1
01	GCR	WR						PWM_F	-	CHIPEN
02	STATUS	R				PUIS	-	LS2	LS1	LS0
03	IMAX	WR					-		IMAX	
04	LCFG1	WR	-	-	-	-		FADE_OUT	FADE_IN	LEDMD
05	LCFG2	WR	-	-	-	-		FADE_OUT	FADE_IN	LEDMD
06	LCFG3	WR	-	-	-	-		FADE_OUT	FADE_IN	LEDMD
07	LEDEN	WR		-	-	-	-	LED3EN	LED2EN	LED1EN
08	LEDCTR	WR			-	-	SYNC	-	PWMEXP	
09	PATRUN	WR	-	STOP3	STOP2	STOP1	-	RUN3	RUN2	RUN1
10	ILED1_1	WR	ILED1_1							
11	ILED2_1	WR	ILED2_1							
12	ILED3_1	WR	ILED3_1							
13	ILED1_2	WR	ILED1_2							
14	ILED2_2	WR	ILED2_2							
15	ILED3_2	WR	ILED3_2							
16	ILED1_3	WR	ILED1_3							
17	ILED2_3	WR	ILED2_3							
18	ILED3_3	WR	ILED3_3							
19	ILED1_4	WR	ILED1_4							
1A	ILED2_4	WR	ILED2_4							
1B	ILED3_4	WR	ILED3_4							
1C	PWM1	WR	PWM1							
1D	PWM2	WR	PWM2							
1E	PWM3	WR	PWM3							
30	PAT1_T1	WR	TRISE				TON			
31	PAT1_T2	WR	TFALL				TOFF			
32	PAT1_T3	WR	TSLOT				TDELAY			
33	PAT1_T4	WR	PATCTR	PATSW	MPULSE		CE4	CE3	CE2	CE1
34	PAT1_T5	WR	REPTIM							
35	PAT2_T1	WR	TRISE				TON			
36	PAT2_T2	WR	TFALL				TOFF			
37	PAT2_T3	WR	TSLOT				TDELAY			
38	PAT2_T4	WR	PATCTR	PATSW	MPULSE		CE4	CE3	CE2	CE1
39	PAT2_T5	WR	REPTIM							
3A	PAT3_T1	WR	TRISE				TON			
3B	PAT3_T2	WR	TFALL				TOFF			
3C	PAT3_T3	WR	-				TDELAY			
3D	PAT3_T4	WR	PATCTR	PATSW	MPULSE		CE4	CE3	CE2	CE1
3E	PAT3_T5	WR	REPTIM							
40	AUDCTR	WR	BUFBYPS	PRECHG	SYNC_MD			TRACKDIS	AGCEN	AUDEN
41	AUDSEL	WR						AS3	AS2	AS1
42	AUDFLT	WR	DECAY_FAC				ATTACK_FAC			
43	AGCGAIN	WR	-		-	GAIN_INI				
44	GAINMAX	WR				GAIN_MAX				
45	AGCCFG	WR		LOCK	DN_STEP		UP_STEP		AVE_PER	
46	AGCATTH	WR	-	ATTH						
47	AGCRLTH	WR	-	RLTH						
48	AGCNOISE	WR	-	NOISE						

49	AUDTIM	WR	-	AUDTIM
4A	ADCDATA	R	-	ADCDATA
4B	AUDLVL	R	-	AUDLVL

DETAILED L REGISTER DESCRIPTION

RSTIDR, Chip ID and Software Reset Register

Address: 0x00, R/W, default: 0xB1

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

Bit	Symbol	Description
7:0	IDR	Chip ID: 0xB1 Reset: write 0x55 to RSTIDR, reset internal logic and register

GCR, Global Control Register

Address: 0x01, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	PWM_F	-	CHIPEN

Bit	Symbol	Description
2	PWM_F	PWM Modulation Frequency Select 0: 122Hz PWM modulation 1: 245Hz PWM modulation
0	CHIPEN	Device operating Enable 0: Disable, the device is in standby state 1: Enable, the device enters active state

STATUS Register

Address: 0x02, R/W, default: 0x10

7	6	5	4	3	2	1	0
0	0	0	PUIS	-	LS3	LS2	LS1

Bit	Symbol	Description
4	PUIS	Power Up Interrupt Status 0: No power-up reset has taken place 1: Power-up reset has taken place
2	LS3	operating status indication for pattern controller 3 0: no pattern is running 1: pattern is running
1	LS2	operating status indication for pattern controller 2 0: no pattern is running 1: pattern is running
0	LS1	operating status indication for pattern controller 1

0: no pattern is running
1: pattern is running

IMAX, LED Maximum Current Register

Address: 0x03, R/W, default: 0x01

7	6	5	4	3	2	1	0
-	-	-	-	-	IMAX		

Bit	Symbol	Description
1:0	IMAX	Maximum LED Current Select 00：9mA 01：18mA 10：37mA 11：75mA

LCFG1-3 LED Configure Register

LCFG1: Address: 0x04, R/W, default: 0x01
LCFG2: Address: 0x05, R/W, default: 0x00
LCFG3: Address: 0x06, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	FADE_OUT	FADE_IN	LEDMD

Bit	Symbol	Description
2	FADE_OUT	Fade-out enable control, only active in manual mode 0: PWM fade-out is disable, 1: PWM fade-out is enable, the dimming time decide by Tfall
1	FADE_IN	Fade-in enable control, only active in manual mode 0: PWM fade-in is disable, 1: PWM fade-in is enable, the dimming time decide by T_{RISE}
0	LEDMD	LED Operating Mode Select. 0: Manual mode, LEDx is control directly by register ILEDx_1 and PWMx 1: Pattern mode

LEDEN, LED Channel Enable Register

Address: 0x07, R/W, default: 0x01

7	6	5	4	3	2	1	0
-	-	-	-	-	LED3EN	LED2EN	LED1EN

Bit	Symbol	Description
2	LED3EN	LED3 Enable 0: LED3 module stop work and LED3 out disable (default) 1: LED3 module enable
1	LED2EN	LED2 Enable 0: LED2 module stop work and LED2 out disable (default) 1: LED2 module enable
0	LED1EN	LED1 Enable

0: LED1 module stop work and LED1 out disable
1: LED1 module enable (default)

LEDCTR, LED Control Register

Address: 0x08, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	SYNC	-	PWMEXP	

Bit	Symbol	Description
3	SYNC	LED Breathing Synchronous Mode Select 0: 3 LED work in asynchronous mode with independent control 1: 3 LED work in synchronous mode for RGB application
1:0	PWMEXP	PWM exponential curve select 0x: Exponential of 60 10: Exponential of 10 11: Linearity

PATRUN, Pattern Run/Stop Register

Address: 0x09, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	STOP3	STOP2	STOP1	-	RUN3	RUN2	RUN1

Bit	Symbol	Description
6	STOP3	Write 1, LED3 pattern stop if independent mode; The bit clears to 0 automatically after write 1.
5	STOP2	Write 1, LED2 pattern stop if independent mode; The bit clears to 0 automatically after write 1.
4	STOP1	Write 1, LED1 pattern stop if independent mode; Write 1, pattern stop if pattern mode; The bit clears to 0 automatically after write 1.
2	RUN3	Write 1, LED3 pattern run if independent mode; The bit clears to 0 automatically after write 1.
1	RUN2	Write 1, LED2 pattern run if independent mode; The bit clears to 0 automatically after write 1.
0	RUN1	Write 1, LED1 pattern run if independent mode; Write 1, pattern run if pattern mode; The bit clears to 0 automatically after write 1.

ILED1_y, LED1 Current Register

ILED1_1: Address: 0x10, R/W, default: 0xFF
ILED1_2: Address: 0x13, R/W, default: 0x00
ILED1_3: Address: 0x16, R/W, default: 0x00
ILED1_4: Address: 0x19, R/W, default: 0x00

7	6	5	4	3	2	1	0

ILED1_y

Bit	Symbol	Description
2:0	ILED1_y	LED1 Current Configure Register, 8bit, the LED1 output current value is IMAX * ILED1_y / 255.

ILED2, LED2 Current Register

ILED2: Address: 0x11/0x14/0x17/0x1A, R/W, default: 0x00

7	6	5	4	3	2	1	0
ILED2_y							

Bit	Symbol	Description
7:0	ILED2_y	LED2Current Configure Register, 8bit, the LED2 output current value is IMAX * ILED2_y / 255.

ILED3, LED3 Current Register

ILED3: Address: 0x12/0x15/0x18/0x1B, R/W, default: 0x00

7	6	5	4	3	2	1	0
ILED3_y							

Bit	Symbol	Description
7:0	ILED3_y	LED3 Current Configure Register, 8bit, the LED3 output current value is IMAX * ILED3_y / 255.

PWM1/PWM2/PWM3 , PWM duty level Register

PWM1: Address: 0x1C, R/W, default:0xFF
PWM2: Address: 0x1D, R/W, default:0x00
PWM3: Address: 0x1E, R/W, default:0x00

7	6	5	4	3	2	1	0
PWMx							

Bit	Symbol	Description
7:0	PWMx	PWM level for LEDx,8bit.

PATx_T1, Time Parameter of Pattern x Register

PAT1_T1: Address: 0x30, R/W, default: 0x80
PAT2_T1: Address: 0x35, R/W, default: 0x00
PAT3_T1: Address: 0x3A, R/W, default: 0x00

7	6	5	4	3	2	1	0
TRISE				TON			

Bit	Symbol	Description
7:4	TRISE	Rise Time:

TRISE	Time	TRISE	Time
0000	0s	1000	2.1s
0001	0.13s	1001	2.6s

0010	0.26s	1010	3.1s
0011	0.38s	1011	4.2s
0100	0.51s	1100	5.2s
0101	0.77s	1101	6.2s
0110	1.04s	1110	7.3s
0111	1.6s	1111	8.3s

3:0 TON On Time:

TON	Time	TON	Time
0000	0.04s	1000	2.1s
0001	0.13s	1001	2.6s
0010	0.26s	1010	3.1s
0011	0.38s	1011	4.2s
0100	0.51s	1100	5.2s
0101	0.77s	1101	6.2s
0110	1.04s	1110	7.3s
0111	1.6s	1111	8.3s

PATx_T2, Time Parameter of Pattern x Register

PAT1_T2: Address: 0x31, R/W, default: 0x86
PAT2_T2: Address: 0x36, R/W, default: 0x00
PAT3_T2: Address: 0x3B, R/W, default: 0x00

7	6	5	4	3	2	1	0
TFALL				TOFF			

Bit Symbol Description
6:4 TFALL Fall Time of pattern:

TFALL	Time	TFALL	Time
0000	0s	1000	2.1s
0001	0.13s	1001	2.6s
0010	0.26s	1010	3.1s
0011	0.38s	1011	4.2s
0100	0.51s	1100	5.2s
0101	0.77s	1101	6.2s
0110	1.04s	1110	7.3s
0111	1.6s	1111	8.3s

3:0 TOFF Off Time of pattern:

TOFF	Time	TOFF	Time
0000	0.04s	1000	2.1s
0001	0.13s	1001	2.6s
0010	0.26s	1010	3.1s
0011	0.38s	1011	4.2s

0100	0.51s	1100	5.2s
0101	0.77s	1101	6.2s
0110	1.04s	1110	7.3s
0111	1.6s	1111	8.3s

PATx_T3, Time Parameter of Pattern x Register

PAT1_T3: Address: 0x32, R/W, default: 0x00
PAT2_T3: Address: 0x37, R/W, default: 0x00
PAT3_T3: Address: 0x3C, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	TSLOT			TDELAY			

Bit 6:4 Symbol TSLOT Description: Slot Time Between Pulses

TSLOT	Time
000	0ms
001	130ms
010	260ms
011	380ms
100	540ms
101	670ms
110	800ms
111	1024ms

Bit 3:0 Symbol TDELAY Description: Delay Time of Pattern Start

TDELAY	Time	TDELAY	Time
0000	0s	1000	2.1s
0001	0.13s	1001	2.6s
0010	0.26s	1010	3.1s
0011	0.38s	1011	4.2s
0100	0.51s	1100	5.2s
0101	0.77s	1101	6.2s
0110	1.04s	1110	7.3s
0111	1.6s	1111	8.3s

PATx_T4, Time Parameter of Pattern x Register

PAT1_T4: Address: 0x33, R/W, default: 0x00
PAT2_T4: Address: 0x38, R/W, default: 0x00
PAT3_T4: Address: 0x3D, R/W, default: 0x00

7	6	5	4	3	2	1	0
PAT_CTR	PAT_SW	MPULSE		CE4	CE3	CE2	CE1

Bit Symbol Description

7	PAT_CTR	Pattern running forever control 0: pattern run forever 1: pattern stop or switch to next pattern after repeating specified times.
6	PAT_SW	Pattern Switch enable, active only in true-color pattern mode. 0: Pattern switch is disabled 1: Pattern switch is enabled
5:4	MPULSE	Multiple Pulse mode selection. 00: 1 pulse 01: 2 pulses 10: 3 pulses 11: 4 pulses
3	CE4	Color #4 display enable 0: Color#4 is masked 1: Color#4 is allow to display
2	CE3	Color #3 display enable 0: Color#3 is masked 1: Color#3 is allow to display
1	CE2	Color #2 display enable 0: Color#2 is masked 1: Color#2 is allow to display
0	CE1	Color #1 display enable 0: Color#1 is masked 1: Color#1 is allow to display Note: if CE1~CE4 are all set to 0, Color #1 is displayed by default

PATx_T5, Time Parameter of Pattern x Register

PAT1_T5: Address: 0x34, R/W, default: 0x00
PAT2_T5: Address: 0x39, R/W, default: 0x00
PAT3_T5: Address: 0x3E, R/W, default: 0x00

7	6	5	4	3	2	1	0
REPTIM							

Bit	Symbol	Description
7:0	REPTIM	PATTERN Repeat Times REPTIM [7] = 0: Pattern repeats REPTIM[6:0]+1 times REPTIM [7] = 1: Pattern repeats (REPTIM[6:0]+1) * 16 times

AUDCTR, Audio Control Register

Address: 0x40, R/W, default:0x00

7	6	5	4	3	2	1	0
BYPSS	PRECHG	SYNC_MD			TRACK_DIS	AGCEN	AUDEN

Bit	Symbol	Description
7	BYPSS	Only for factory test, must be 0
6	PRECHG	Pre-amplifier input capacitance charge enable.

0: disable
1: enable input capacitance charge to build common mode voltage rapidly.

5:3	SYNC_MD	Audio LED Mode 000: Parallel mode with single color 001: Parallel mode with color switching periodically 010: Parallel mode with color switching on signal cross-zero 011: Parallel mode with color switching periodically or on signal cross-zero 100: Bar mode 101: RGB mode others: non-defined
2	TRACK_DIS	AGC Trace Disable, only used in test mode. 0: Enable gain trace 1: Disable gain trace
1	AGCEN	AGC Enable Control 0: Disable AGC, the gain of pre-amplifier is defined by register AGCGAIN 1: Enable AGC, the pre-amplifier adjust its gain with the audio analog input
0	AUDEN	Audio synchronization function enable control 0: Audio synchronization module is disabled 1: Audio synchronization module is enabled

AUDSEL, Audio LED Output Selection Register

Address: 0x41, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	-	-	-	-	AS3	AS2	AS1

Bit	Symbol	Description
2	AS3	LED3 output Audio synchronization signal selection. 0: Audio synchronization do not output to LED3 1: Audio synchronization output to LED3
1	AS2	LED2 output Audio synchronization signal selection. 0: Audio synchronization do not output to LED2 1: Audio synchronization output to LED2
0	AS1	LED1 output Audio synchronization signal selection 0: Audio synchronization do not output to LED1 1: Audio synchronization output to LED1

AUDFLT, Audio Filter Register

Address:0x42, R/W, default: 0x00

7	6	5	4	3	2	1	0
-		DECAY_FAC		-		ATTACK_FAC	

Bit	Symbol	Description
7:4	DECAY_FAC	Decay Factor for Peak Detect Filter 00: 32ms 01: 16ms 10: 8ms 11: 4ms

3:0	ATTACK_FAC	Attack Factor for Peak Detect Filter 00: 32us 01: 64us 10: 128us 11: 256us

AGCGAIN, AGC Gain Register

Address: 0x43, R/W, default: 0x10

7	6	5	4	3	2	1	0
-	-	-	GAIN				

Bit	Symbol	Description
4:0	GAIN	AGC Gain setting. When AGCEN=0, preamplifier's gain is fixed to the value decided by GAIN. When AGCEN=1, GAIN set the Initial gain.

GAINMAX, AGC Gain Maximum Value Register

Address: 0x44, R/W, default:0x1F

7	6	5	4	3	2	1	0
-	-	-	GAINMAX				

Bit	Symbol	Description
4:0	GAINMAX	The Maximum Gain that AGC can adjust to.

AGCCFG, AGC Configure Register

Address: 0x45, R/W, default: 0x3D

7	6	5	4	3	2	1	0
-	-LOCK	DOWNSTEP		UP_STEP		AVE_PER	

Bit	Symbol	Description
6	LOCK	Only for factory test, must be 0
5:4	DOWN_STEP	Gain Trace Down Speed. 00: 0.13s/step. 01: 0.26s/step 10:0.39s/step 11: 0.52s/step (default)
3:2	UP_STEP	Gain Trace Up Speed. 00: 0.26s/step. 01: 0.52s/step 10:0.78s/step 11: 1.04s/step (default)
1:0	AVE_PER	RMS Sampling Cycle 00: Fast 01: Normal (default) 10: Slow 11: Slowest

AGCATTH, AGC Attack Threshold Register

Address: 0x46, R/W, default: 0x30

7	6	5	4	3	2	1	0
	ATTH						

Bit	Symbol	Description
6:0	ATTH	AGC Attack Threshold AGC Gain decrease if RMS is larger than ATTH.

AGCRLTH, AGC Release Threshold Register

Address: 0x47, R/W, default: 0x20

7	6	5	4	3	2	1	0
	RLTH						

Bit	Symbol	Description
6:0	RLTH	AGC Release Threshold AGC Gain increase if RMS is smaller than RLTH.

AGCNOISE, AGC Noise Threshold Register

Address: 0x48, R/W, default: 0x00

7	6	5	4	3	2	1	0
-	NOISE						

Bit	Symbol	Description
6:0	NOISE	AGC Noise Threshold. AGC gain keep constant if RMS blew AGC_NOISE

AUDTIM, Audio Color Switch Timer Register

Address: 0x49, R/W, default: 0x00

7	6	5	4	3	2	1	0
-						AUDTIM	

Bit	Symbol	Description
1:0	AUDTIM	Color Switch Timer for audio synchronization mode, active only when AUDCTR.SYNC_MD =001 or 011. 00: 1s 01: 2s 10: 4s 11: 8s

ADCDATA, AUDIO ADC DATA

Address: 0x4A, R, default: 0x00

7	6	5	4	3	2	1	0
-	ADCDATA						

Bit	Symbol	Description

6:0	ADCDATA	AUDIO ADC Data

AUDLVL, Audio Level

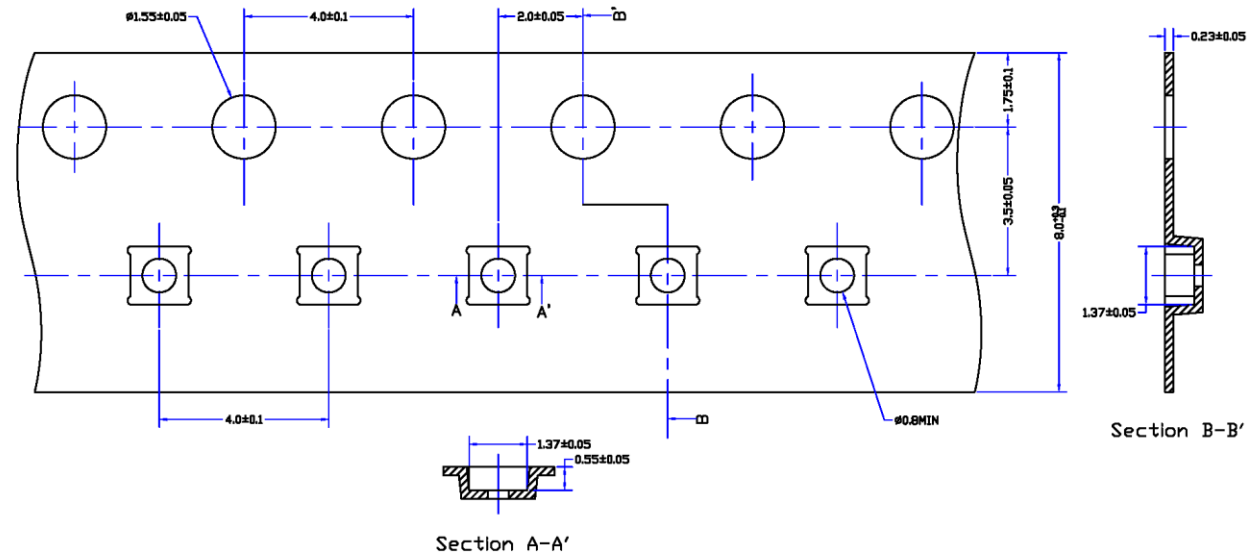
Address: 0x4B, R, default: 0x00

7	6	5	4	3	2	1	0
-	AUDLVL						

Bit	Symbol	Description
6:0	AUDLVL	Audio Level, time configuration refers to AGCCFG(0x45)

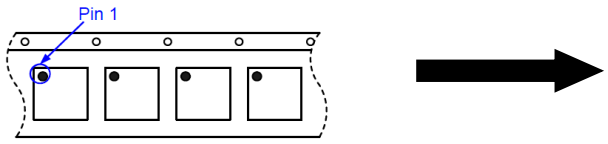
TAPE AND REEL INFORMATION

Carrier Tape



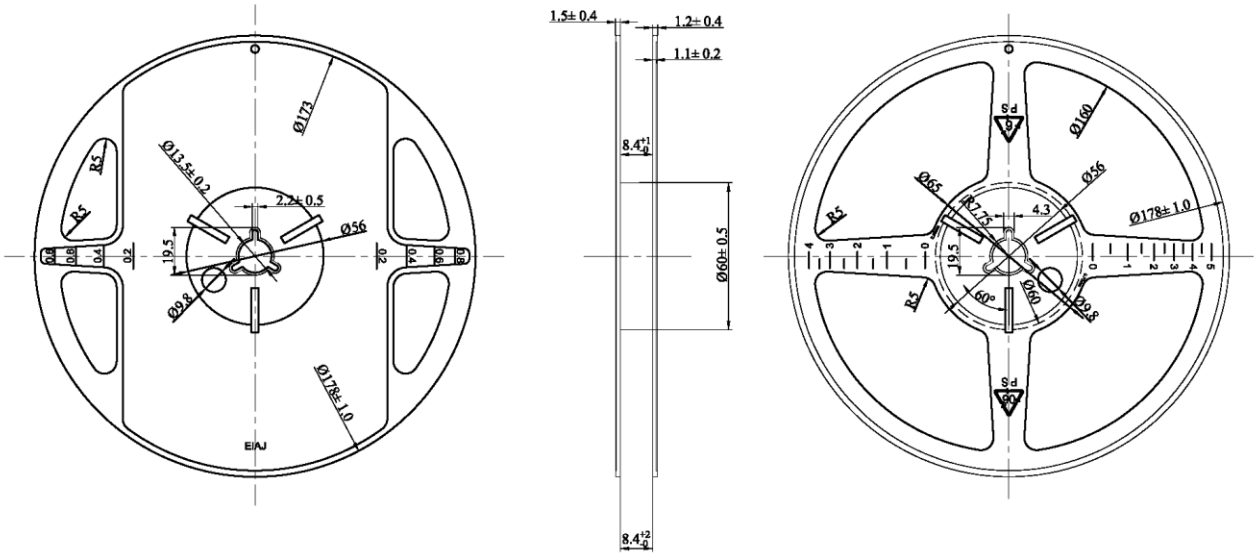
NOTES:
1.10 procket hole pitch cumulative tolerance ±0.2
2.The meander of the tape is assumed with 1mm or less every 100mm between 250mm
3.MATERIAL:CONDUCTIVE POYSTYRENE
4.ALL DIMS IN MM
5.There must not be foreign body adhesion and the state of the surface must be excellent
6.17" PAPER-Reel, 125000 pockets(500m)
7.Surface resistance 1X10E11(max) OHMS/SQ

PIN1 Direction

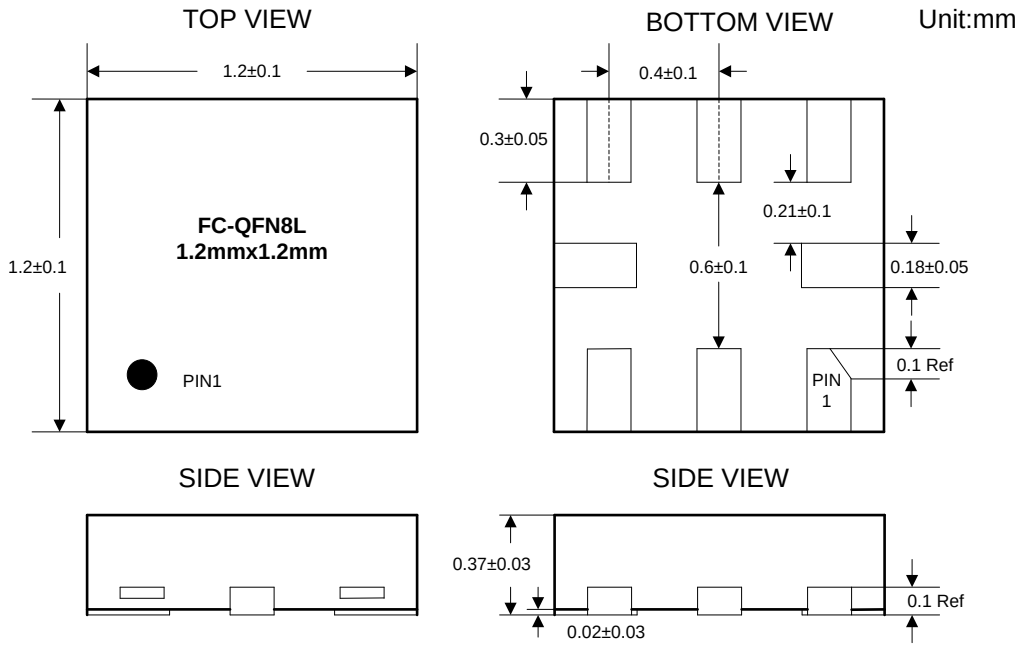


User Direction of Feed

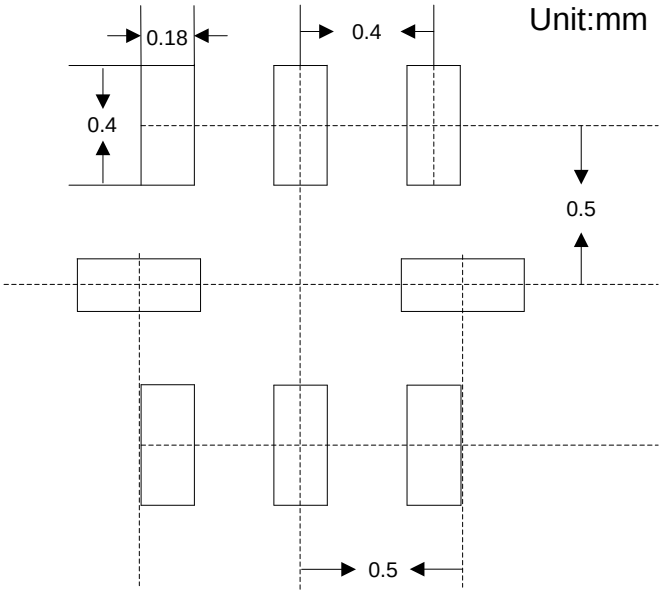
Reel



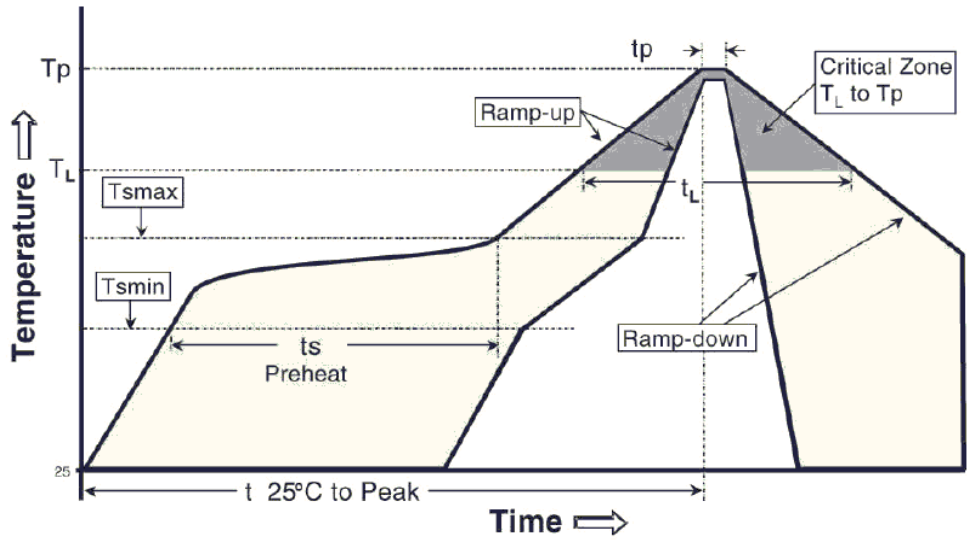
PACKAGE DESCRIPTION



RECOMMENDED LAND PATTERN



REFLOW PROFILE



Reflow profile

Classification Reflow Profile

Reflow condition	Sn-Pb eutectic assembly		Pb-Free assembly	
	Pkg. thickness ≥ 2.5 mm or Pkg. volume ≥ 350 mm³	Pkg. thickness < 2.5 mm and Pkg. volume < 350 mm³	Pkg. thickness ≥ 2.5 mm or Pkg. volume ≥ 350 mm³	Pkg. thickness < 2.5 mm and Pkg. volume < 350 mm³
Average ramp-up rate (Liquidus Temperature (T_L) to Peak)	3 °C/second max.		3 °C/second max.	
Preheat - Temperature Min ($T_{s(min)}$) - Temperature Max ($T_{s(max)}$) - Time (min to max) (t_s)	100 °C 150 °C 60-120 seconds		150 °C 200 °C 60-180 seconds	
$T_{s(max)}$ to T_L - Ramp-up Rate			3 °C/second max.	
Time maintained above: - Temperature (T_L) - Time (t_L)	183 °C 60-150 seconds		217 °C 60-150 seconds	
Peak Temperature (T_p)	225 +0/-5 °C	240 +0/-5 °C	245 +0/-5 °C	250 +0/-5 °C
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	10-30 seconds	10-30 seconds	20-40 seconds
Ramp-down Rate	6 °C/second max.		6 °C/second max.	
Time 25 °C to Peak Temperature	6 minutes max.		8 minutes max.	

Parameters for classification reflow profile

Note: 1. All of the temperature parameters are measured from the top of package;

2、AW2028H is suitable for Pb-Free assembly.

VERSION HISTORY

Version	Data	Change Record
V1.0	Aug. 2015	Officially Release
V1.1	Nov. 2017	1. Update ordering information 2. Update the chip marking 3. Add reflow profile 4. Delete the Chinese description

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