Final exam study guide

This study guide is based on material in lectures 15 to 19. Try to work out the questions without looking at the solutions and then check your work. While the questions in the final may be different from those below, answering these will help you study for the final.

Lectures 9 and 10

Design each of the following:

1. A 4-bit binary adder-subtractor.
2. A 4-bit decimal adder
3. A 4-bit by 3-bit binary multiplier.
4. A magnitude comparator.

Lecture 11 and 12

1. Design each of the following: SR Latch with NAND gates, SR latch with NOR gates
2. D latch
3. D flipflop
4. JK and T flipflops
5. What is the characteristic equation and excitation table for each type of flipflop.
6. Design counters using different type of flipflops.

Lectures 13 and 14

1. Design a universal shift register.

2.Using the synthesis procedure, design a counter with T flip flops that repeats the following count sequence: 1, three, four, seven. Show the state diagram, state table, flip flop input equations, and the circuit.

3. Repeat the previous problem using JK flip flops.

4. Using the synthesis procedure, design a BCD counter with D flip flops. Show the state diagram, state table, flip flop input equations, and the circuit.

5.What is a ring counter? Show the timing diagram for the circuit on slide 17 of lectures 15-16. How is it different from a Johnson counter?

Lectures 15 and 16

1. What is the difference between

(a) RAM and ROM

(b) SRAM and DRAM

2. Given the SRAM memory cell shown on slide 16 of lecture17_18, explain how the read and write operations work.

3. How can you build a 4x4 RAM using SRAM memory cells, a 2-to-4 decoder,and OR gates.

4. Explain how to program the 32x8 ROM shown on slide 21 using the truth table on slide 22.

5. How can you create a 256 K RAM using 4 64 K RAMs.

Lectures 17 and 18

1. Implement a logic function on a PLA.

2. Implement a logic function on a PAL.

3. Implement a logic function on an FPGA (see slide 19)

Lectures 5 and 6

1. Review half and full adders

2. Review 2-to-1, 4-to-1, 8-to-1 muxes.

3. How to create larger muxes from smaller ones.

4. Review 3-to-8-line decoder, creating an adder with a decoder.

5. What is a three-state gate?

Lectures 7 and 8

1. How to represent numbers in different bases

2. 1's complement and 2's complement system

3. Converting from 1 base to another

4. What are BCD numbers?

5. Binary addition and subtraction

6. Different types of codes

Lectures 1 and 2:

1. Review boolean theorems on slide 20

2. Review digital logic gates on slide 45

3. Representing functions using:

(a) standard forms (POS, SOP)

(b) canonical forms (sum of minterms, product of maxterms)

4. Using DeMorgan's theorem

5. Work out the problems on simplification using boolean algebra in slides and homework.

Lectures 3 and 4

1. Solve problems using 3, 4, and 5 variable Kmaps

2. SImplify a function with don't care conditions using a Kmap

3. Convert a AND-OR circuit to a NAND only circuit.

4. Convert a OR-AND circuit to a NOR only circuit.

5. What are the degenerate forms?

Review

Given a function f = ab + ac + bcd + bcf, design the following circuits for f:

(a) a multi-level circuit

(b) two-level circuit

What is the maximum delay along any path from input to output in each circuit? What is the area of each circuit?

2. What is the clock to Q delay Tckq, setup time Tsetup, and hold time Thold of a flip flop?