SANTA CLARA UNIVERSITY	ELEN 153	Dr. S. Krishnan T.A. Sanad Kawar
Laboratory #4: 3-Input NAND gate Schematic and Simulations		

I. OBJECTIVES

- To create a schematic and symbol for a 3 input NAND gate
- To perform simulations to verify the NANDs functionality.

II. LAB PROCEDURE

PART A: 3-Input schematic and Symbol

- Enter a schematic of a 3-input NAND gate using Synopsys Custom Compiler: Name your inputs pins: A, B, C. Make pin A to be the closest from the output pin and pin C, the farthest (near Ground). Name your output pins: OUT.
  Note: For PMOS and NMOS device aspect rations (W/L), size the devices to match the rise and fall time of the inverter created in Lab 2. **Explain how you arrived at your answer in your lab report.**
- Create a symbol for your NAND gate. Make sure to use the correct symbol shape. Refer to the tutorial if needed.

PART B: Transient Simulation

In this section, we will perform a transient simulation to verify the NANDs functionality.

- Create a new test-bench to simulate the NAND gate:

- For inputs(A,B and C) of the NAND, connect Pattern sources **Vpat** from **analoglib**.
- Setup the patterns in each source so that all input combinations (000, 001, 010…111) are produced. Set the sample time as 200nS and the rise/fall time as 10nS
- Connect a load capacitance at OUT1: CLOAD = 2pF
- Use SAE to setup a transient simulation, and plot the inputs and outputs. Decide how long the transient simulation needs to run, and make sure to run the transient simulation long enough to see all input combinations.
- Verify that the NAND is operating as intended.
- **Measure the Rise and Fall time of the output**.

PART C: Voltage Transfer Characteristics

1. **Input A Sweep**
   a) Connect a dc voltage source **vdc**, from analoglib, to input A. set it's DC value to 1.2V.
   b) Repeat for inputs B,C.
   c) Setup a DC simulation in SAE, and sweep the voltage source **connected to input A** from 0 to 1.2 V.
   d) Setup the output of the NAND gate (OUT) as your output in SAE.
   e) Before running the simulation, change the plotting type in SAE, from the default replace, or the new that you usually use, into **append**. This will allow us to super-impose the different plots in this section.
   f) Netlist and Run the simulation.
   g) Find V_M on that plot, the same way you found V_M for the inverter in Lab 2.

2. **Input B Sweep**
   a) Repeat steps in c-g above for input B now. i.e. change the DC simulation to sweep the source connected to **input B** instead.
   b) Is V_M the same or different?

3. **Inputs A and B Sweep**
   a) Delete the DC voltage source connected to input B.
   b) Connect the DC voltage source at A to B as well, i.e. one voltage source is connected to both A and B inputs.
   c) Repeat steps c-g.
   d) What is V_M now?

III. REPORT

Write a short laboratory report that details all the work done. Describe the objective and procedures of this lab with your own words. The lab report should contain the following:

a) All schematics and testbenches used in your lab.
b) Simulation setup and all waveforms.
c) Answer any questions in the lab assignment
d) Conclusions