SANTA CLARA UNIVERSITY	ELEN 153	Dr. S. Krishnan T.A. Sanad Kawar
Laboratory #1: Introduction to Synopsys		

I. OBJECTIVES

- To learn how to setup and use Synopsys Custom Compiler to create and simulate schematics.
- To simulate the I-V characteristics of an NMOS transistor.
- To construct and simulate a simple voltage divider network and an RC network

II. LABORATORY PROCEDURE

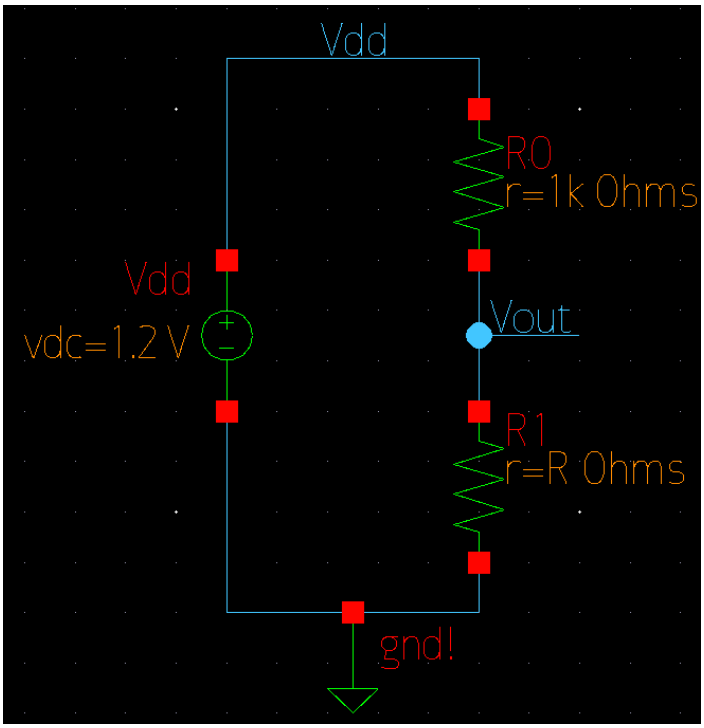
PART A: Synopsys Tutorial and NMOS I-V Curves

- Follow pages 1-20 of the Synopsys Custom Compiler Part 1: Schematics and Simulations, in order to learn how to setup and run Synopsys tools and to simulate the I-V curves of an NMOS.

PART B: Voltage Divider

1. Schematic

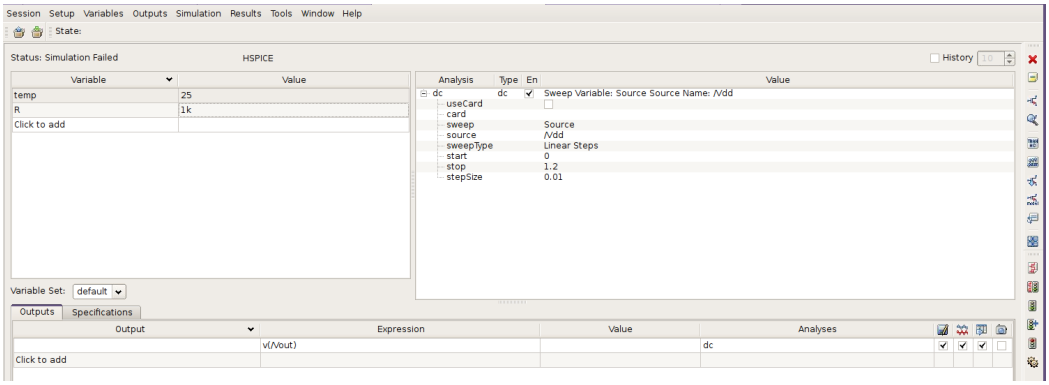
- Using the same steps in the Tutorial, create a new Library. Name it Lab1.
- Create a Cell "Voltage_Divider", and create a Schematic View for it. Draw the following Voltage Divider Circuit. Make sure to give R1 the design variable value **R**, as we will vary this value in the simulation.
  Reminder: Res, Vdc and gnd! Components can be found in AnalogLib Library.



2. Simulation

Source Sweep

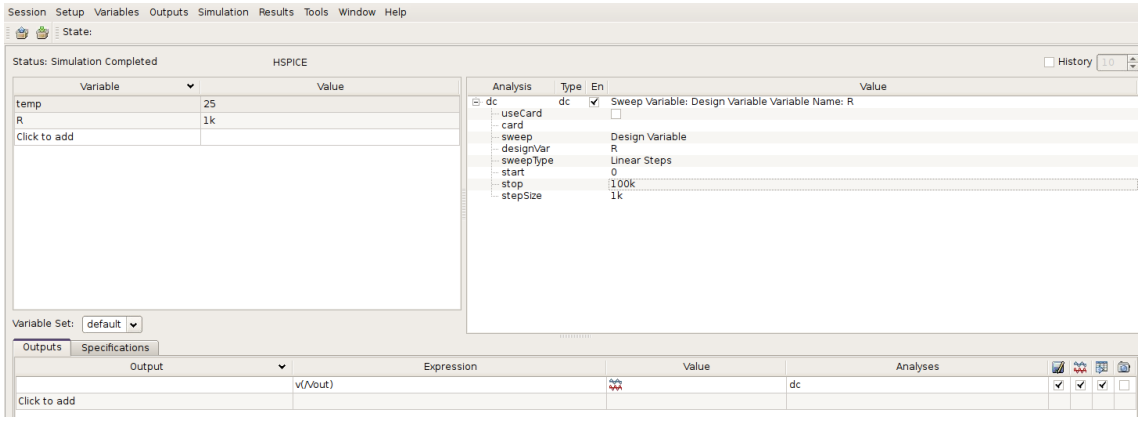
- Refer to the Tutorial to setup a DC simulation in SAE, and sweep the source voltage, Vdd, from 0 to 1.2V. Plot Vout.
- Define Design Variable **R**, and assign **1k** value to it. Your setup should match the figure below.



- Run the simulation and view the Vout plot.
  Questions:
- What is Vout when Vdd=0.6V? 1.2V?

Resistance Sweep

- Adjust the DC simulation to sweep the design variable R, from 0 to 1MΩ. Your setup should match the figure below.



- Run the simulation and view the Vout plot.

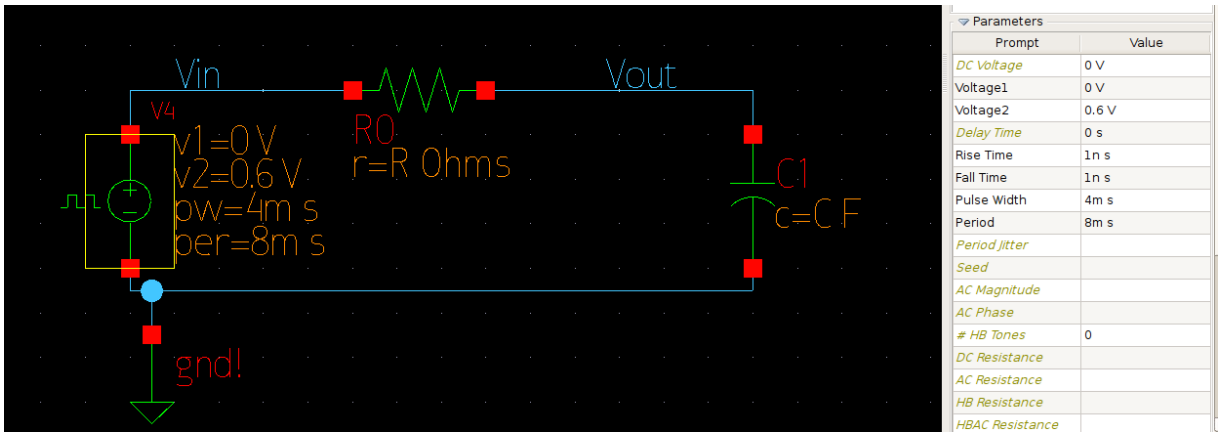
Questions:

- What is Vout when R=0? What is it when R=1MΩ?

PART C: Simple RC Network

1. Schematic

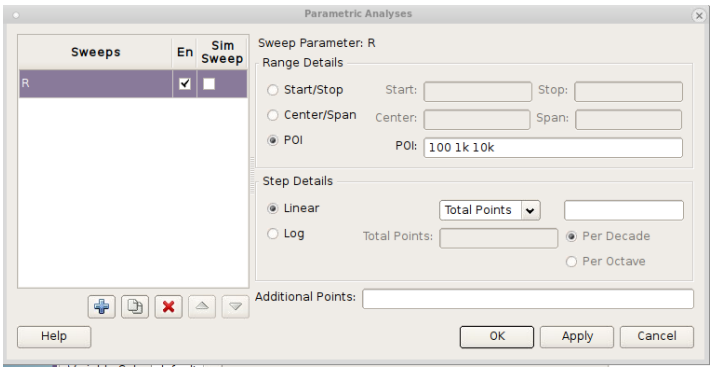
- In the Lab1 library, create a Cell "RCnetwork", and create a Schematic View for it. Draw the following RC Circuit. Make sure to give R1 the design variable value **R** , and **C.**
  Note: For the input voltage source, use **vpulse** from the AnalogLib library. Setup the parameters as shown on the right-side parameters section in the figure below.



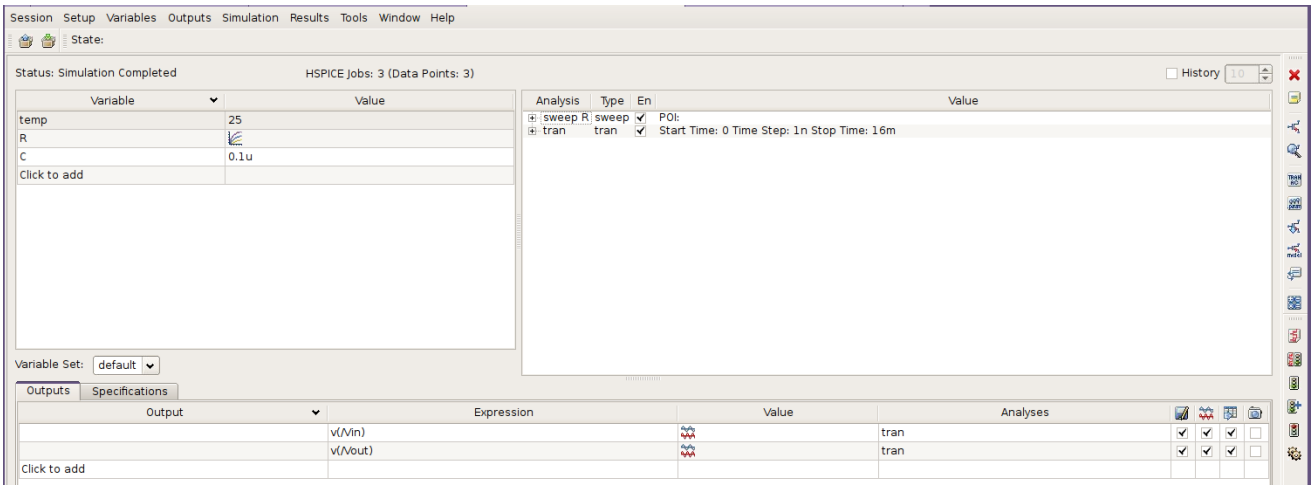
2. Simulation

Resistance
Refer to transient simulations section of the tutorial, pages 29-32 to do the following:

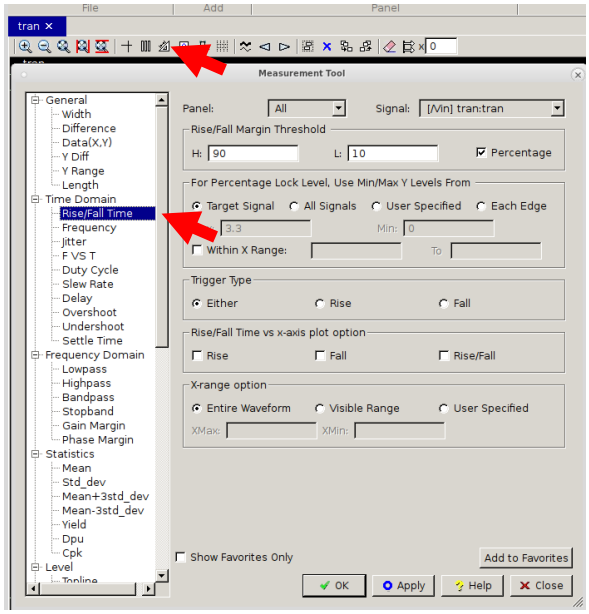
- Open SAE and setup a transient simulation with time step 1nS and stop time 16mS.
- Define design variable **C** as 1uF and **R** as 1kΩ.
- Setup a Parametric Analysis for design variable R, and assign values 100, 1k and 10kΩ as shown below.



Your setup should match the figure below

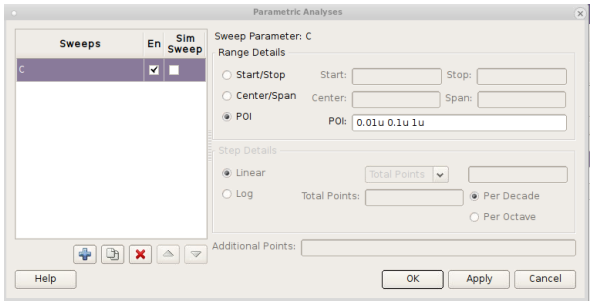


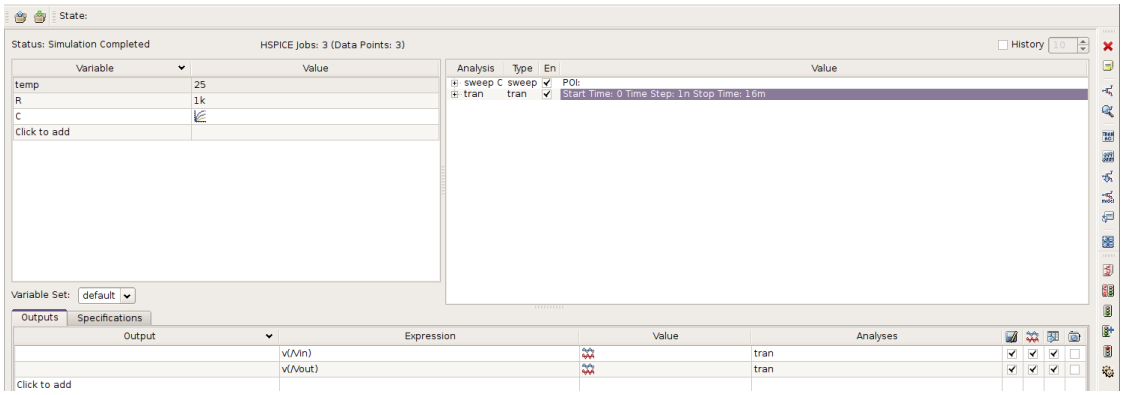
- Run the simulation and view Vin and Vout waveforms.
- Use the measurement tool in WaveView to measure the rise and fall time of each case as shown below. Include these measurements in your report.



Capacitance

- Repeat the above steps, but adjust the parametric analysis to assign design variable C to 0.01u, 0.1u and 1uF. Make sure Parametric Analysis for R is turned off and R is fixed at 1kΩ. Your Parametric analysis and simulation setup should match the figures below.





- Run the Simulation and view Vin and Vout waveforms.
- Use the measurement tool to measure rise and fall times in each case. Remember to include these measurements in your report

V. REPORT

Write a short laboratory report that details all the work done. Describe the objective and procedures of this lab with your own words. The lab report should contain the following:

a) All schematics used in your lab.
b) Screenshots of all Simulation setups in SAE
c) All Simulation Results, including waveforms and any required values/measurements.
d) Answer any questions in the lab assignment
e) Conclusions