ELEN 153: Digital Integrated Circuit Desb 59114

Lab 2: CMOS Inverter

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Wednesday 2:15-5:00pm 2017/10/4

I. OBJECTIVE

- To learn how to create and edit symbols and testbenches in Synopsys Custom Compiler
- To capture a CMOS inverter schematic and symbol
- To simulate the Voltage transfer characteristic (VTC) of the inverter as well as a transient simulation.

II. LAB PROCEDURE

1. Schematic and symbol

With the help of the Synopsys Tutorial, I created the schematic shown in Figure 1, and saved it as a symbol shown in Figure 2. In order for the symbol to function better, I removed some extra signs on the original given symbol.

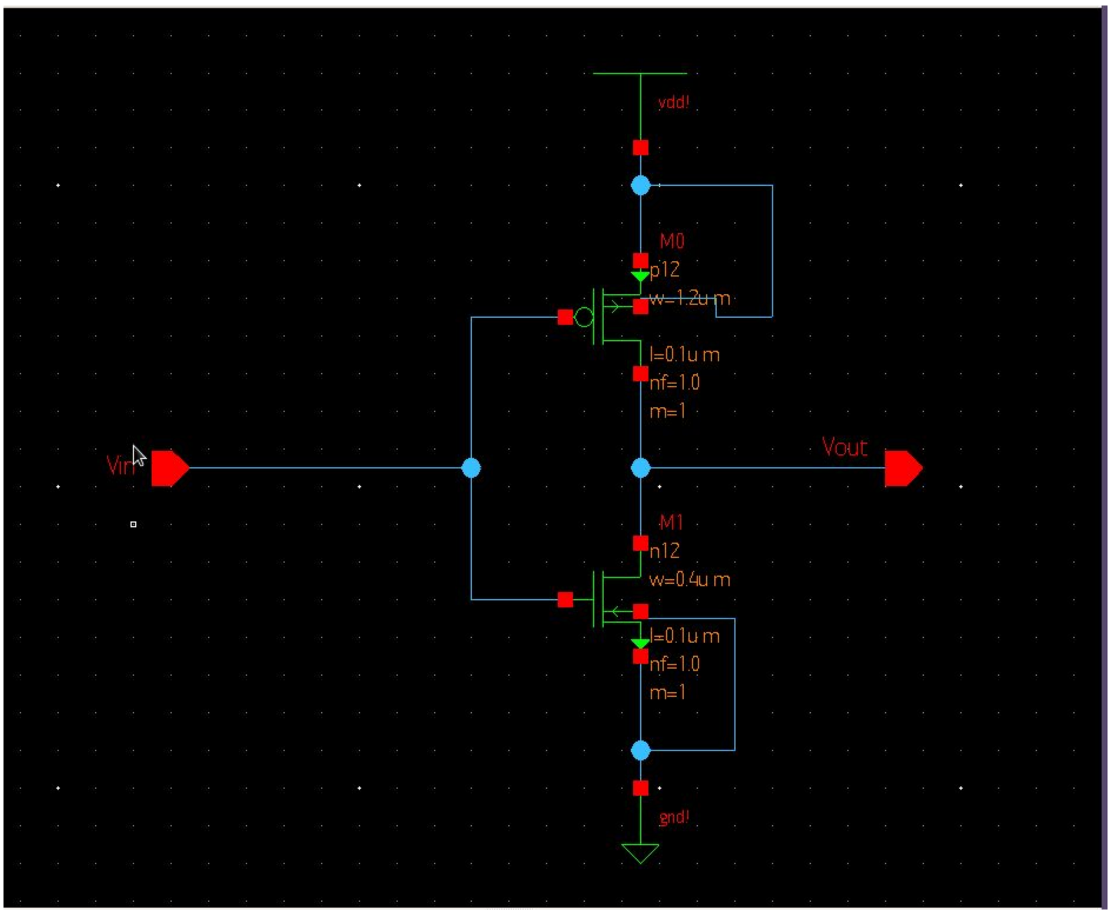


Figure 1. Schematic of CMOS inverter

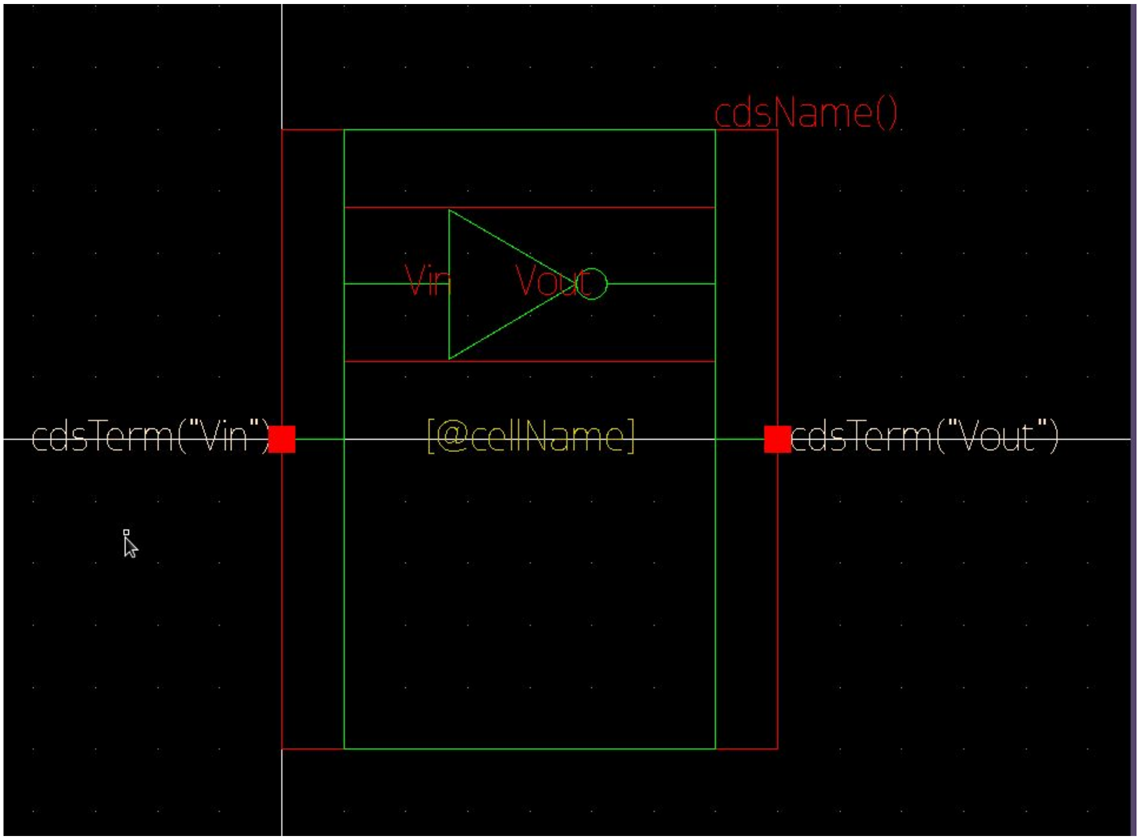


Figure 2. Symbol of CMOS inverter

2. Simulations

First create a new cell called testbench_inverter and a schematic cell view of it, which is shown in Figure 3.

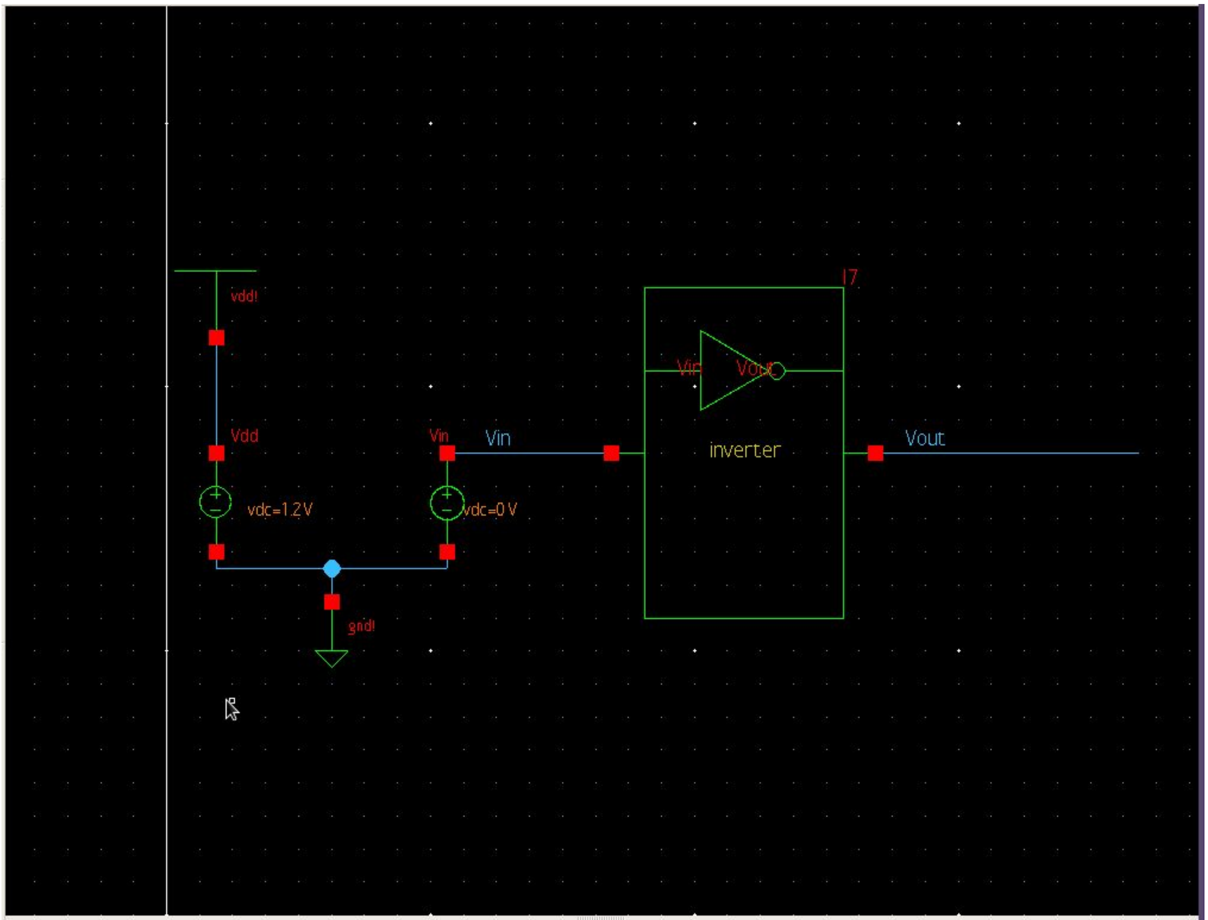


Figure 3. Schematic of testbench of inverter

DC/VTC simulation

To obtain the VTC for the inverter, a DC simulation must be setup to sweep Vin from 0 to 1.2V and plot Vout vs. Vin.

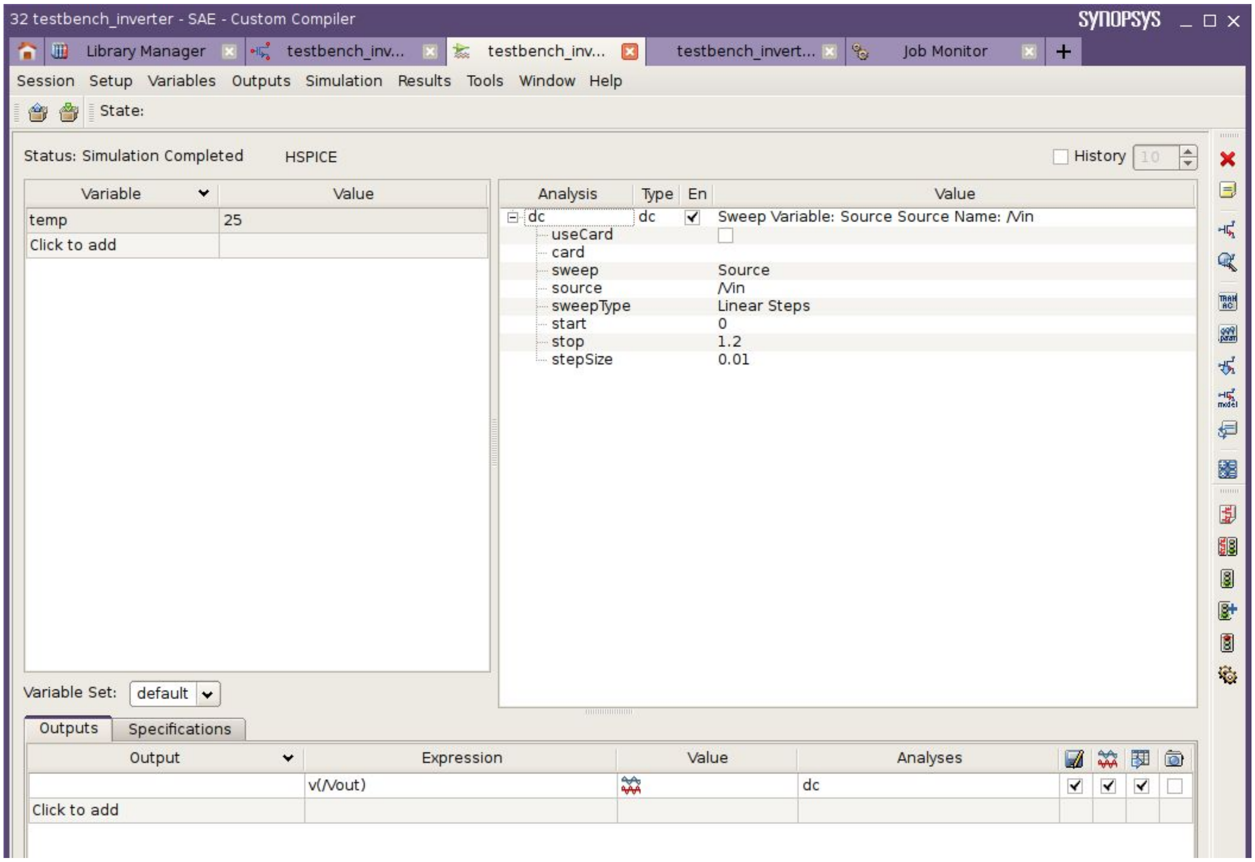


Figure 4. SAE setup of VTC simulation

From what we learn from the lecture, we should expect a reverse “S” curve, like what is shown in Figure 5.

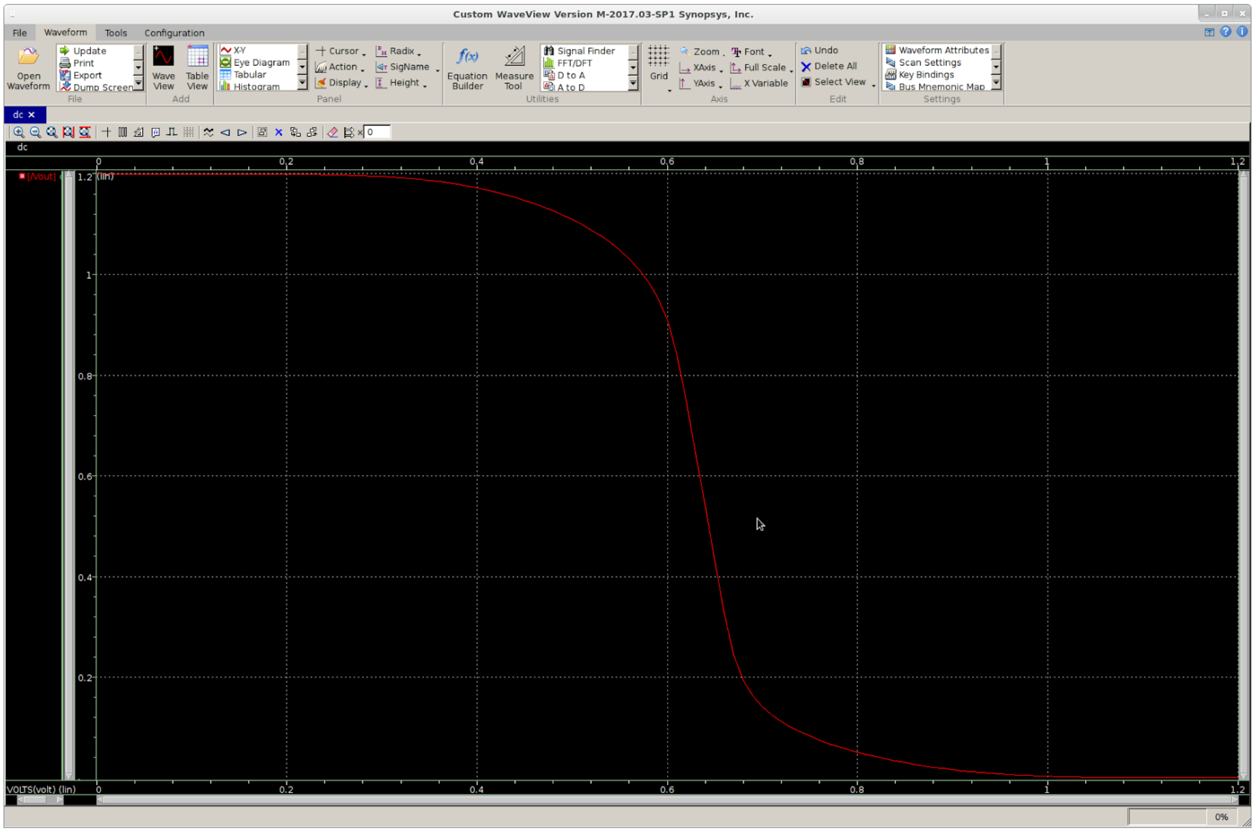


Figure 5. Waveform of VTC simulation

DC Operating Points

DC operating points allow us to find many transistor parameters. In order to do this, we need to add an analysis and select “op” as analysis type as shown in Figure 6.

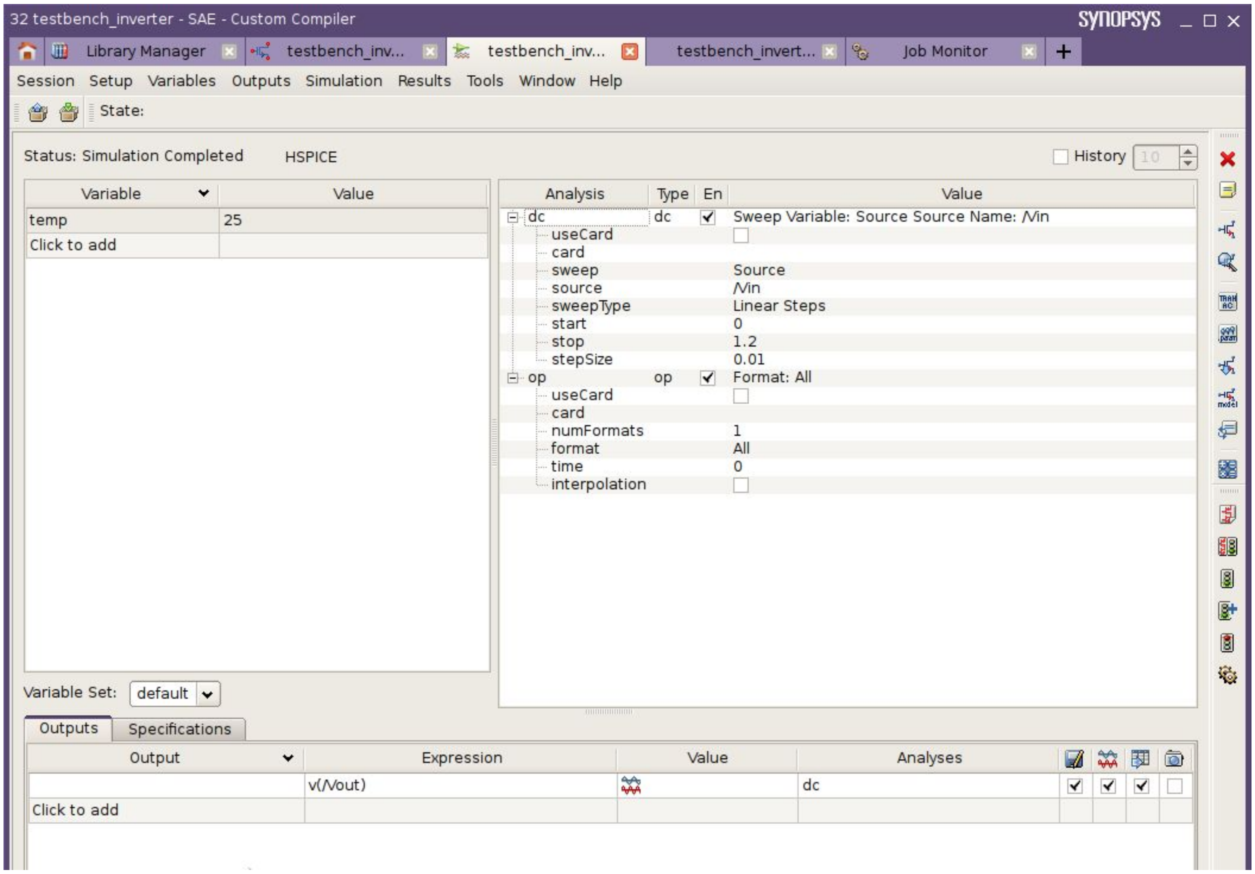
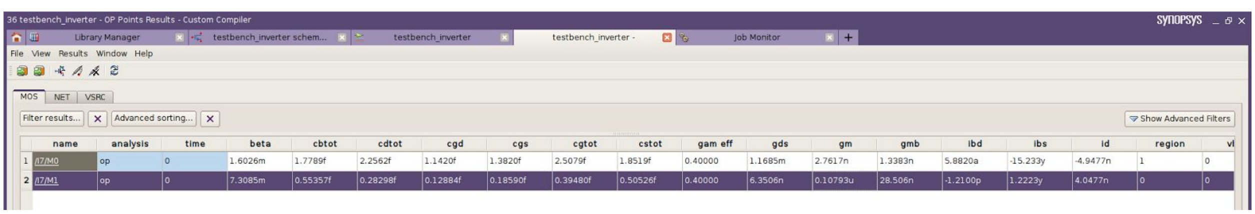


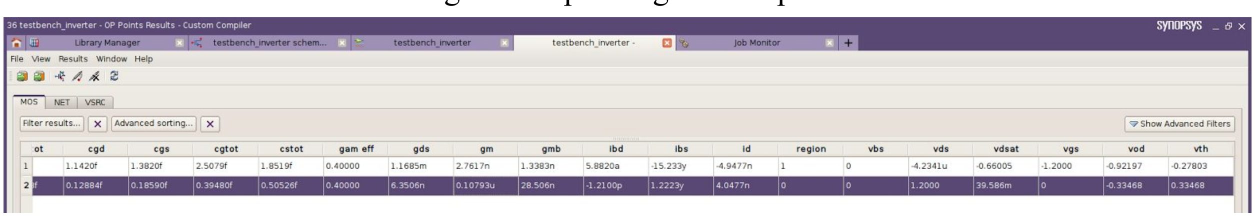
Figure 6. SAE setup of DC Operating Points

We should expect 0.10793u and 2.7617n in the columns of gm and 0.33468 and -0.27803 in the columns of vth.



	name	analysis	time	beta	cbtot	cdtot	cgd	cgs	cgtot	cstot	gam eff	gds	gm	gmb	ibd	ibs	id	region	vl
1	/I7/M0	op	0	1.6026m	1.7789f	2.2562f	1.1420f	1.3820f	2.5079f	1.8519f	0.40000	1.1685m	2.7617n	1.3383n	5.8820a	-15.233y	-4.9477n	1	0
2	/I7/M1	op	0	7.3085m	0.55357f	0.28298f	0.12884f	0.18590f	0.39480f	0.50526f	0.40000	6.3506n	0.10793u	28.506n	-1.2100p	1.2223y	4.0477n	0	0

Figure 7. Operating Point report



	ot	cgd	cgs	cgtot	cstot	gam eff	gds	gm	gmb	ibd	ibs	id	region	vbs	vds	vdsat	vgs	vod	vth
1		1.1420f	1.3820f	2.5079f	1.8519f	0.40000	1.1685m	2.7617n	1.3383n	5.8820a	-15.233y	-4.9477n	1	0	-4.2341u	-0.66005	-1.2000	-0.92197	-0.27803
2	f	0.12884f	0.18590f	0.39480f	0.50526f	0.40000	6.3506n	0.10793u	28.506n	-1.2100p	1.2223y	4.0477n	0	0	1.2000	39.586m	0	-0.33468	0.33468

Figure 8. Operating Point report (Cont.)

Transient simulation

To plot the input and output waveforms of the inverter, as a function of time, a transient simulation is needed. First, we need to replace the DC voltage source at the input of the inverter with a sine wave source. To do that, I inserted a vsin instance and connect it to the input as shown in Figure 9.

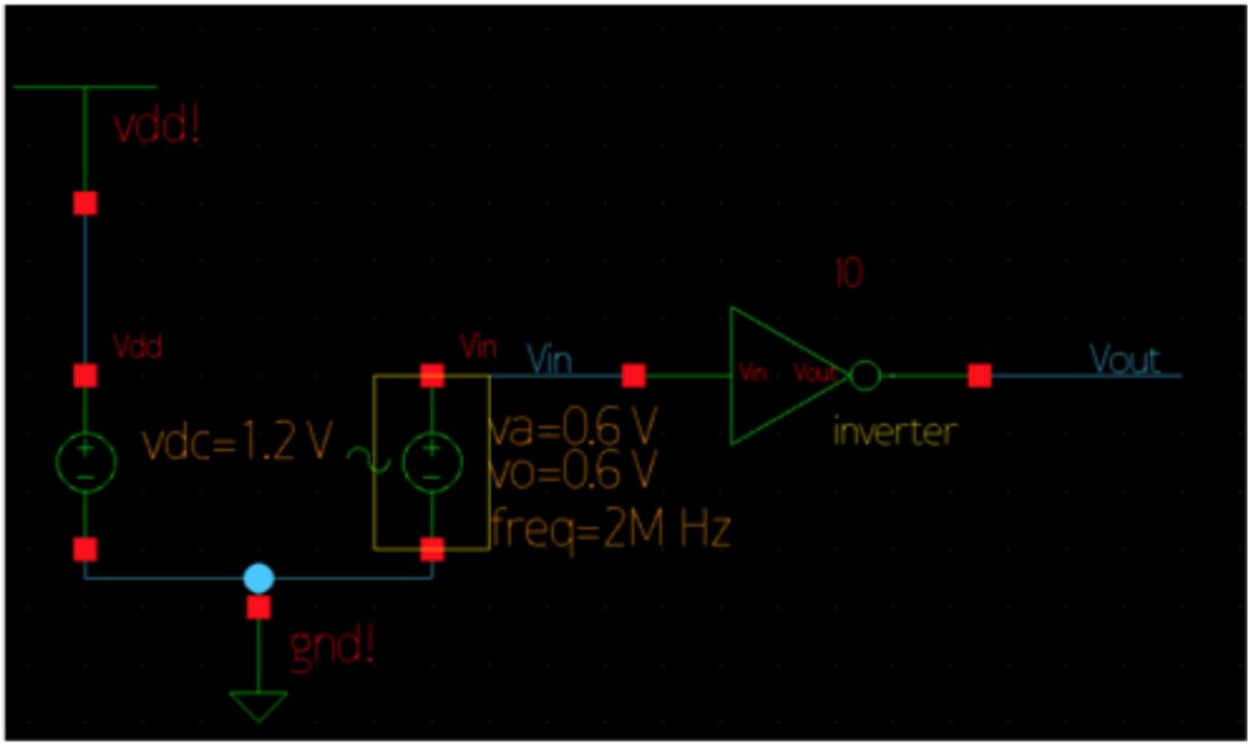


Figure 9. Schematic of Transient Simulation

In Analysis Type, select tran for transient, and setup SAE as shown in Figure 10.

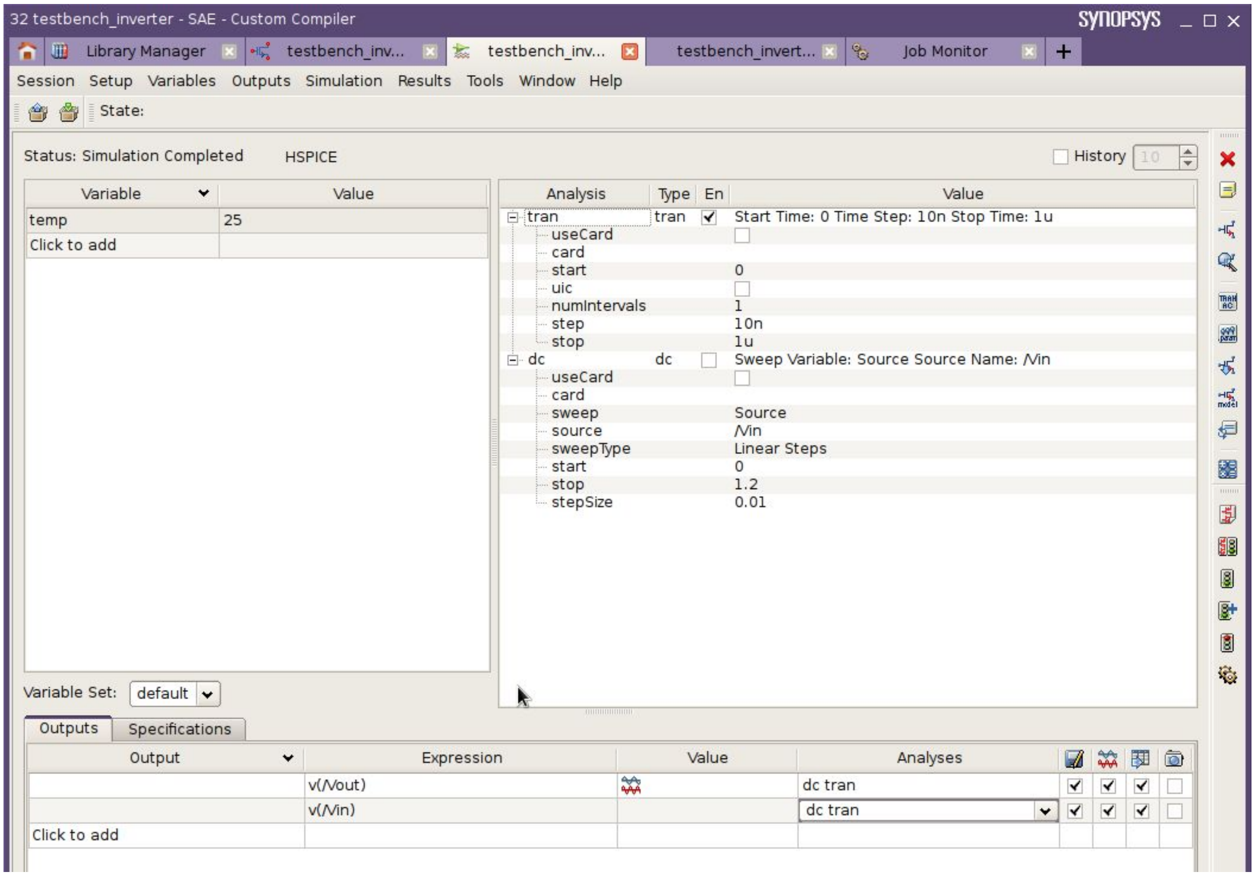


Figure 10. SAE of Transient Simulation

Because we want to plot both Vin and Vout, we need to have both of them in the output pane. Also, we need to disable DC because we don't have a DC input voltage source and it would not produce any relevant results.

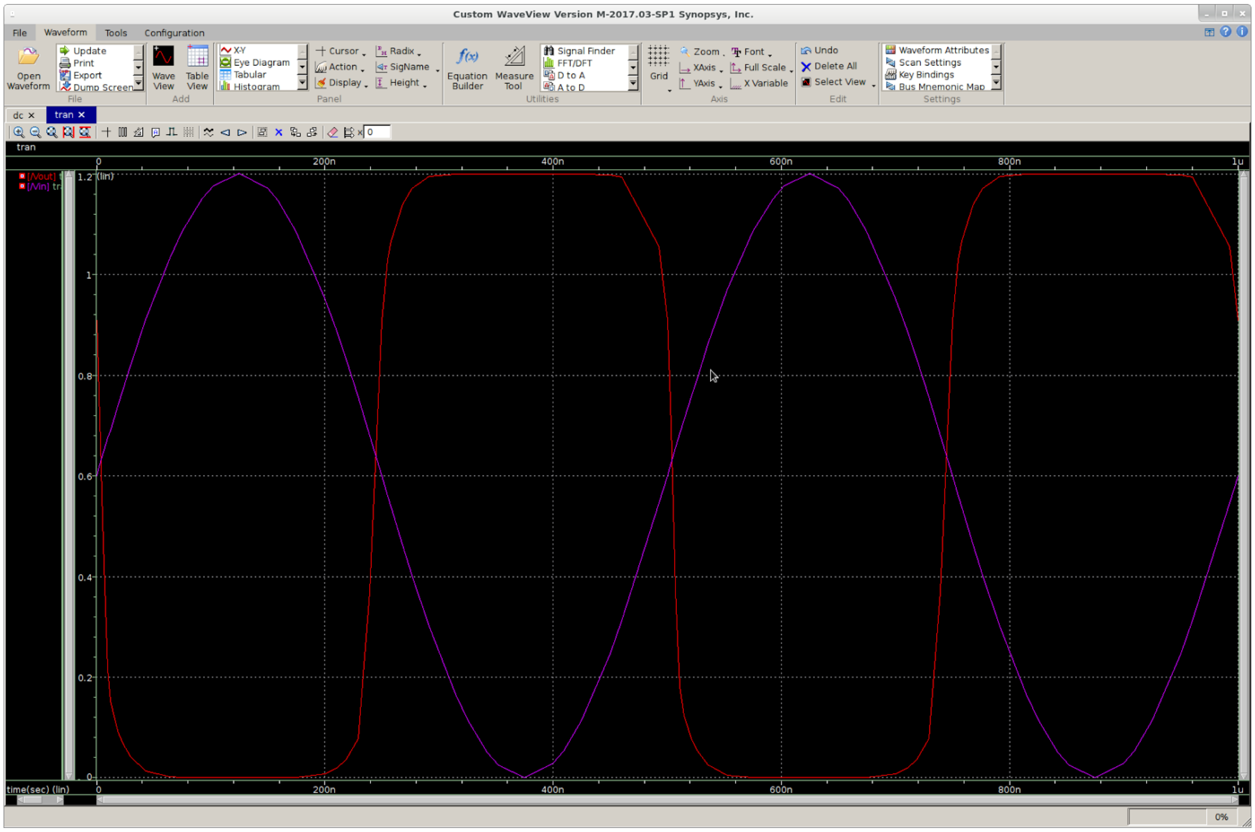


Figure 11. Waveform of Transient Simulation

3. Inverter Threshold Voltage

First, find the inverter threshold voltage VM, where VM = Vin = Vout. Look at the number inside the yellow box at the bottom of the graph and the number in the middle sidebar as shwon in Figure 12.

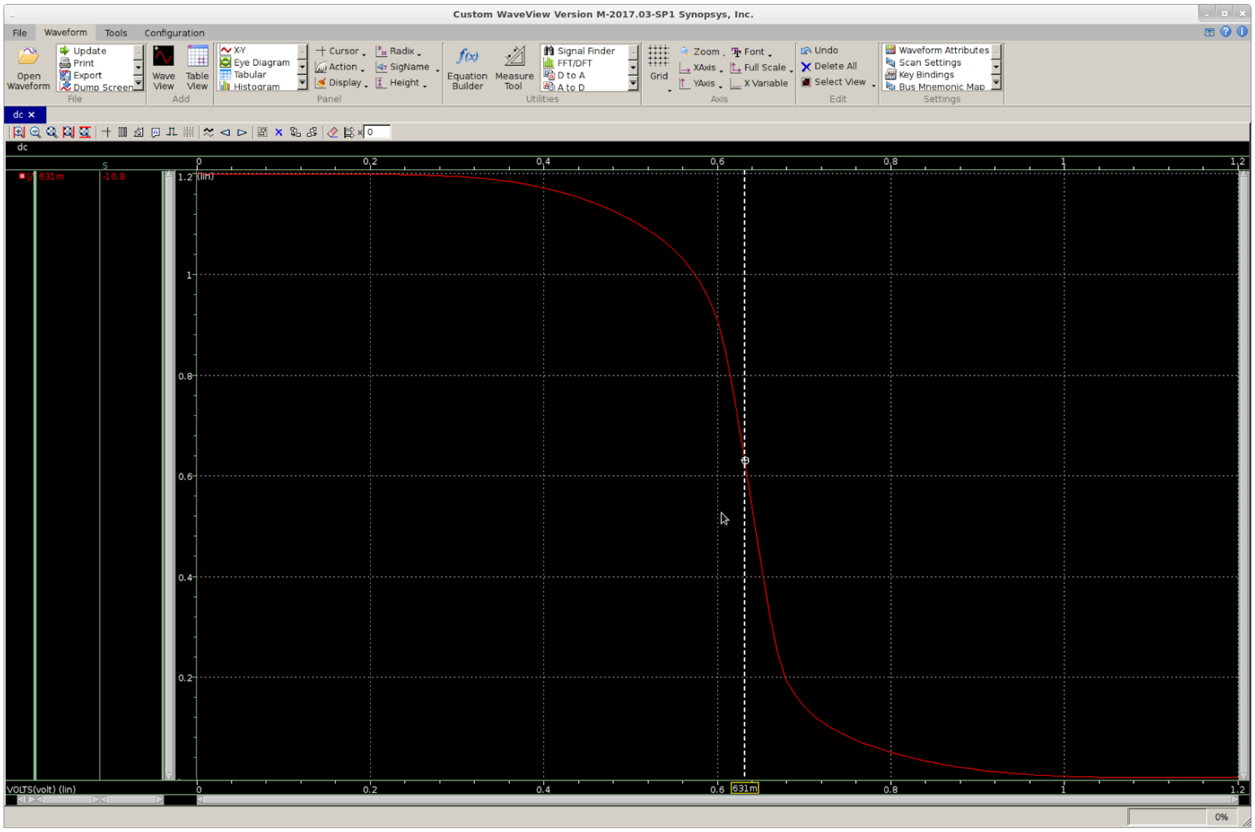


Figure 12. Inverter threshold voltage VM

In order to find V_{IH} and V_{IL}, we need to add a cursor to the waveform, and select the Waveform Monitor tool, and select derivative. Now all we need to do is to find the Vin value for when Vout slope is -1. In Figure 13, the derivative of the point of V_{IL} is -1.11. No exactly the same with -1, but it is the closest value that I can find. In Figure 14, the derivative of the point of V_{IH} is -1.08, and is also the closest value that I can find.

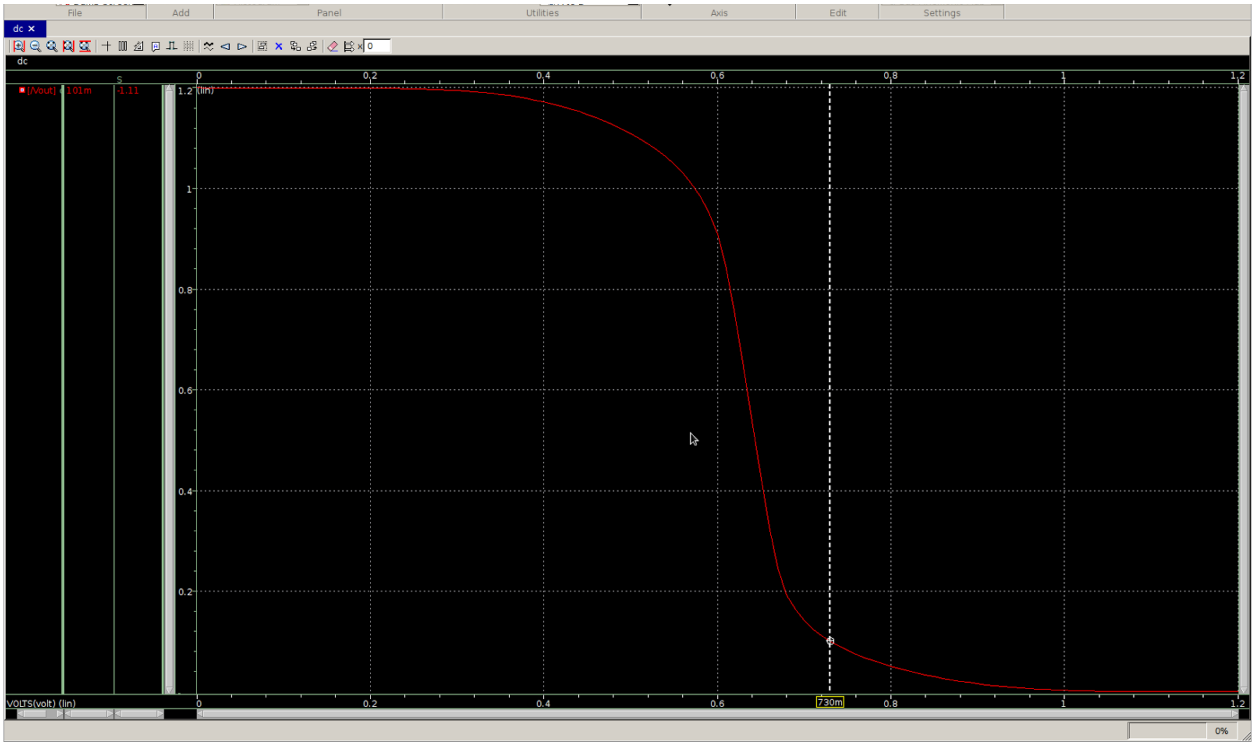


Figure 13. Waveform indicating V_{IL}

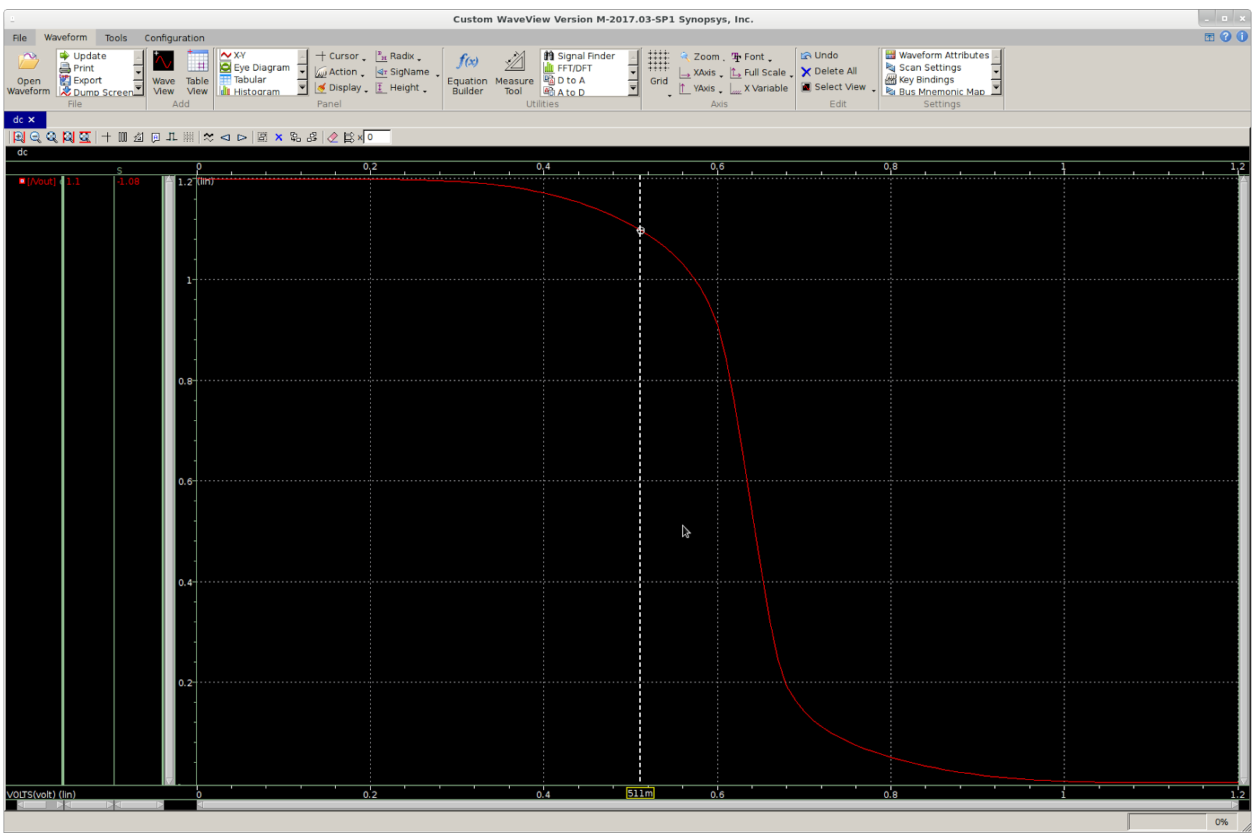


Figure 14. Waveform indicating V_{IH}

III. CONCLUSION

In this lab, I learn how to create schematic and symbol and testbenches and how to do VTC simulation and transient simulation of the inverter. During the lab, I have error when running the simulation. At first, I thought there is error in my schematic, so I looked back into the first schematic and found that the PMOS was not connected with the circuit. I rebuilt the schematic and ran again, but I still got error. With the help of the TA, I learnt that I forgot to add the model files. After including the path, $SAED90_PDK/hspice, I was able to run and get the desired waveform and results.