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Laboratory #4: Multiplexer Design

For lab sections May 2-5, 2017

I. OBJECTIVES

In this laboratory you will design and use a multiplexer as:

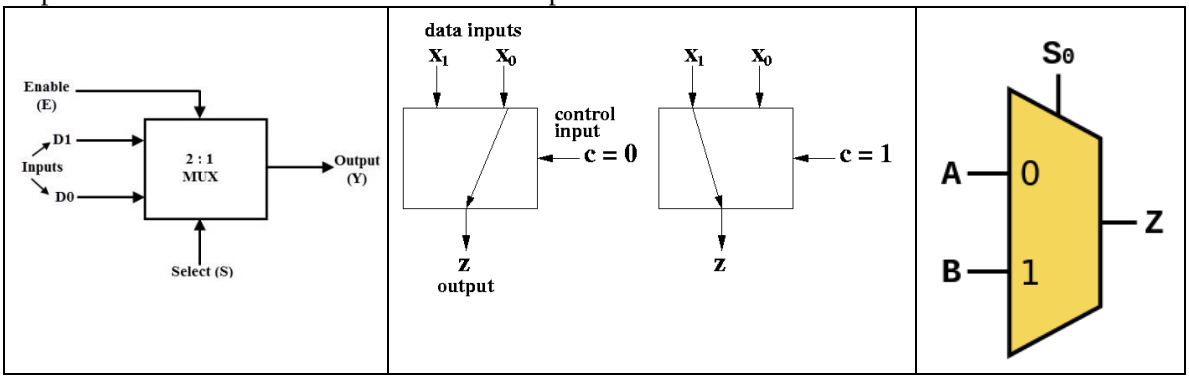
- A switch to connect different inputs to a single wire.
- A building block for logic circuits.

PROBLEM STATEMENT

In this laboratory assignment, you will design a 2 to 1 Multiplexer (MUX) and then use it as a building block to design an 8:1 MUX. A 2 to1 MUX is a switch that allows you to select one of two inputs to appear at the output. (This is similar to selecting a channel number on a television to choose which program will appear on your TV screen for viewing, except that you have a lot more than two choices of channels to view.)

A 2 to 1 MUX has three inputs and one output. Two of the inputs, *w0* and *w1*, are **data inputs**. The third input, *s*, the **select input,** determines which of the data inputs, *w0* or *w1*, will appear on the **output *z***. If *s* is "0", then the output *z* is *w0*. If *s* is "1", then the output *z* is *w1*.

There are many symbolic ways to show a MUX and a variety of naming conventions for the inputs and outputs.. The diagram on the left below shows a 2:1 MUX as a simple box with select input S and data input D1 and D2. On the right the MUX is shown as a trapezoid with data inputs A and B. The diagram in the middle shows the switching model of a 2:1 MUX for the case where select input c is 0 and for the case where select input c is 1. A MUX may have an enable input. If the enable input is "0", the MUX output will be zero no matter what the other inputs are.



More generally, a multiplexer (MUX) is a switch which connects one of 2^n MUX data inputs to a single output. The *n* select inputs of the MUX determine which of the MUX data inputs will appear at the MUX output. An 8:1 Mux selects one of 8 data input signals to appear at the output. Eight of the inputs, *w0, w1*, ……, *w6* and *w7*, are **data inputs**. The three **select inputs**, *s*2 *s*1 *s*0, are the binary value of the index of the input selected to appear at the output.

Multiplexers are a basic building block for logic design and they are fundamental to data routing in computer architecture, processor design, and embedded systems

II. PRE-LAB

Prelab Part 1: Circuit 1 - Multiplexer as a switch

Design a **2-to-1** ***multiplexer*** with a select input *s*, two data inputs *w0* and *w1*, and output *z*.

(a) Show the truth table for this multiplexer

(b) Draw the sum-of-products logic implementation for the circuit.

Prelab Part 2: Circuit 2 – Hierarchical design of Multiplexers

Design and build an **8-to-1** multiplexer using **2-to-1** multiplexers in a hierarchical manner.
How many 2:1 MUXes are needed?
Draw the schematic clearly showing the hierarchical design and clearly indicate in your block diagram the select inputs and the ordering of the data inputs.
Show what the output of each 2:1 MUX in your design will be if $s2\ s1\ s0 = 1\ 0\ 0$.
Show what the output of each 2:1 MUX in your design will be if $s2\ s1\ s0 = 0\ 1\ 1$.

Prelab Part 3: Circuit 3 - Multiplexer as a logic building block

A multiplexer can be used as a standard building block to implement any desired logic function without requiring any minimization techniques. Further, if the specification of the logic function changes, the circuit can be modified by simply changing the MUX data inputs corresponding to the changed truth table values.

> *A majority circuit is to be built whose output F is high when the majority of its three inputs A,B and C are one.*

Draw the truth table for the majority circuit with the three bits A,B and C as the inputs and F as the output. Design the majority circuit using only an 8 to 1 MUX.

Turn in the circuit diagrams of all three circuits as your prelab and answer all questions.

III. LAB PROCEDURE

Design and simulate both Circuit 1 and Circuit 2 in Quartus II:

- Create the schematic for Circuit 1 from your pre-lab in Quartus II.
- Simulate Circuit 1 and obtain the waveforms with all possible input combinations.
- Create a symbol for your 2:1 MUX. (Follow instructions from the laboratory assistant.)
- Create the schematic for circuit 2 from your pre-lab in Quartus II using your 2:1 MUX symbol.
- Simulate Circuit 2 as directed by your laboratory assistant.
- Add an enable to your 8:1 MUX so that the MUX will function normally when the enable is "1" and the MUX output will be "0" whenever the enable is "0".
- Assign pins for all inputs and outputs to connect to LEDs and switches.

- Download the design for the 8:1 MUX onto the FPGA and test it.
    - For each combination of the three select bits:
        - Set all the inputs to 0 and verify that the output is zero.
        - Then individually set each data input to 1 while all the other data inputs are 0. For each data input, observe the output for all select input combinations. Verify that only the correct data input appears at the output for all select input combinations.
- After you have verified that your MUX is working correctly, set up the data inputs for your 8:1 MUX to implement a majority circuit and demonstrate it to your lab assistant.
- Set up the data inputs for your 8:1 MUX to implement a circuit which outputs a "1" whenever an odd number of inputs are "1" and a "0" whenever an even number of inputs are "1." Demonstrate this to your lab assistant.

IV. REPORT

To be completed with your lab group and submitted to Camino before the beginning of the next lab.

- Write an introduction about what your group accomplished during the lab.
- Write the procedure and results obtained (schematics, waveforms, features used, proof of design in FPGA, etc.).
- Explain how you tested the operation of the 8:1 MUX. If you found problems with the circuit that required correction and a new download, explain what you observed that indicated there was a problem and describe how you fixed it.
- Show how you would design a 16:1 MUX using 8:1 and 2:1 MUXes.
- Write a conclusion about the challenges of this lab and what you learned in this lab.