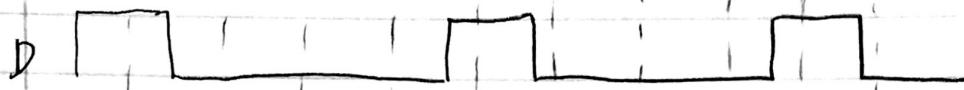
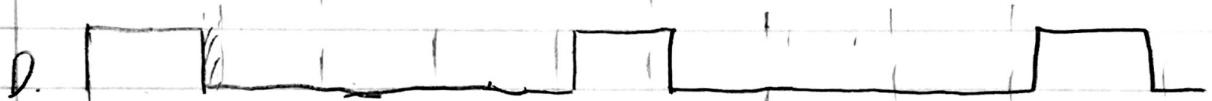


1



A hand-drawn timing diagram illustrating a digital signal. The signal starts at a low level and exhibits several sharp, regular transitions to a high level. These transitions are marked by small arrows pointing upwards, indicating the direction of the signal change. The label 'CLK' is written to the left of the signal waveform.

b



A hand-drawn timing diagram illustrating a clock signal (CLK) and its corresponding output signal. The CLK signal is a square wave with a period of two horizontal grid units. The output signal is also a square wave, delayed by one clock cycle relative to the CLK signal. Arrows point to the rising edges of both signals.

1-Overlap

A timing diagram illustrating a digital clock signal (CLK). The signal is represented by a series of rectangular pulses. Arrows pointing upwards from the baseline indicate the timing of each rising edge.

Δm

c

Any

1