ELEN 153: Digital Integrated Circuit Des 59114

Lab 4: 3-Input NAND gate Schematic and Simulations

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Wednesday 2:15-5:00pm 2017/10/18

I. OBJECTIVE

- To create a schematic and symbol for a 3 input NAND gate
- To perform simulations to verify the NANDs functionality.

II. LAB PROCEDURE

Part A: 3-Input schematic and Symbol

Create a schematic of a 3-intput NAND gate, with inputs A, B, and C, and output OUT.

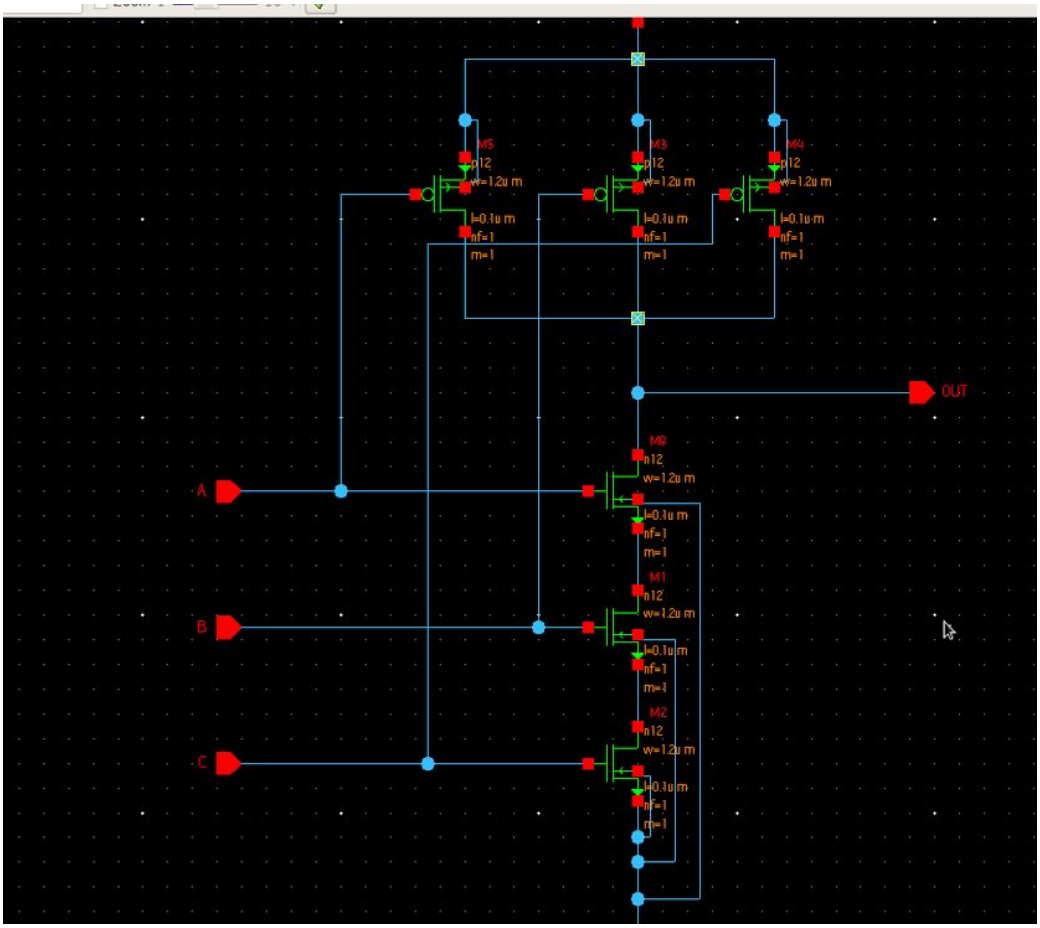

Figure 1. Schematic of 3-input NAND gate(detailed)

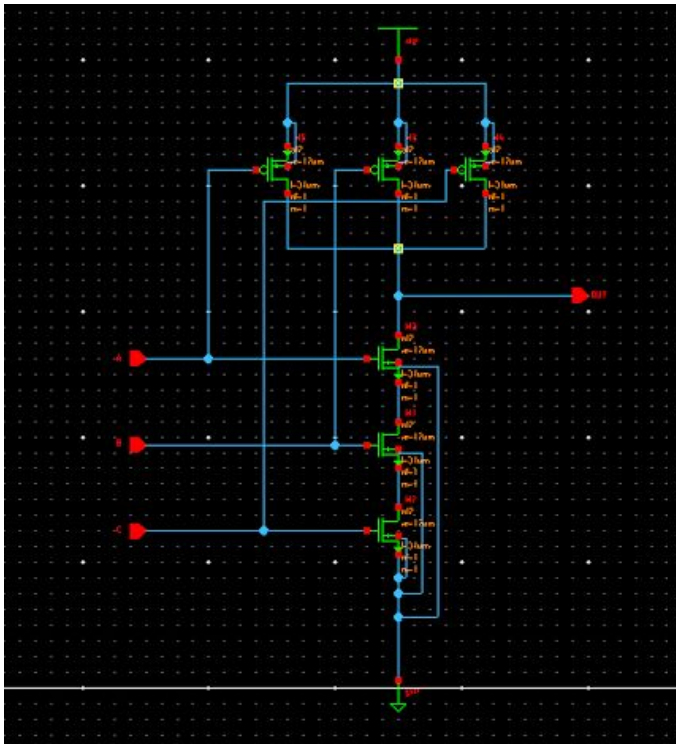

Figure 2. Schematic of 3-input NAND gate

In order to have the PMOS and NMOS devices match the rise and fall time of the inverter created in Lab2, we should have $(W/L)_p = 3(W/L)_n$. I set $W_n = 1.2$ um, $L_n = 0.1$ um, $W_p = 1.2$ um, $L_p = 0.1$ um, so we have $(W/L)_n = (1.2 * 3)/(0.1 * 3) = 12$ and $(W/L)_p = (1.2 * 3)/0.1 = 36$, so that $(W/L)_p = 3(W/L)_n$.

Then create a symbol for the NAND gate. Use nd3 as the symbol shape.

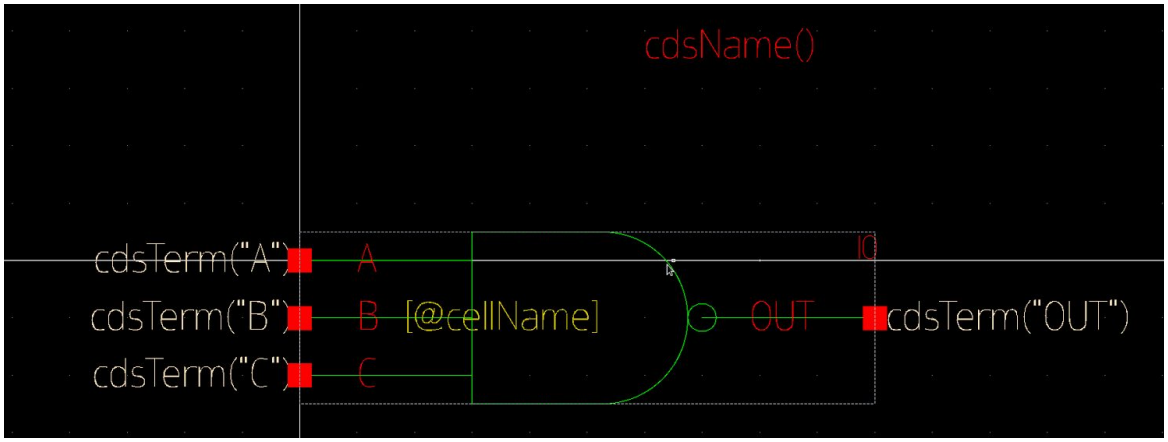

Figure 3. Symbol for the NAND gate

<u>Part B</u>: Transient Simulation

Create a test-bench to simulate the NAND gate.

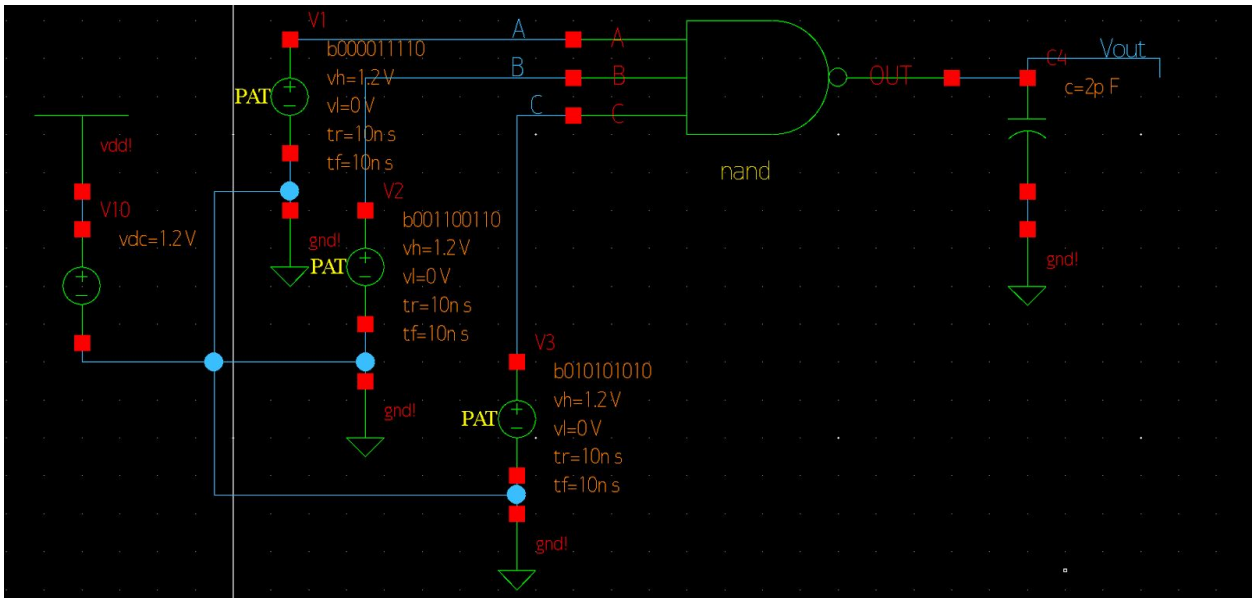

Figure 4. Schematic to perform transient simulation

I set up the input combinations as shown in Table 1. The reason that we need an extra 0 at the end, because we need to see the rise. If the inputs remain high(at 1), which is default if we don't change the combination, the output is just going to be low(at 0), as shown in Figure 5.

Table 1. Input combinations

A	000011110
B	001100110
C	010101010

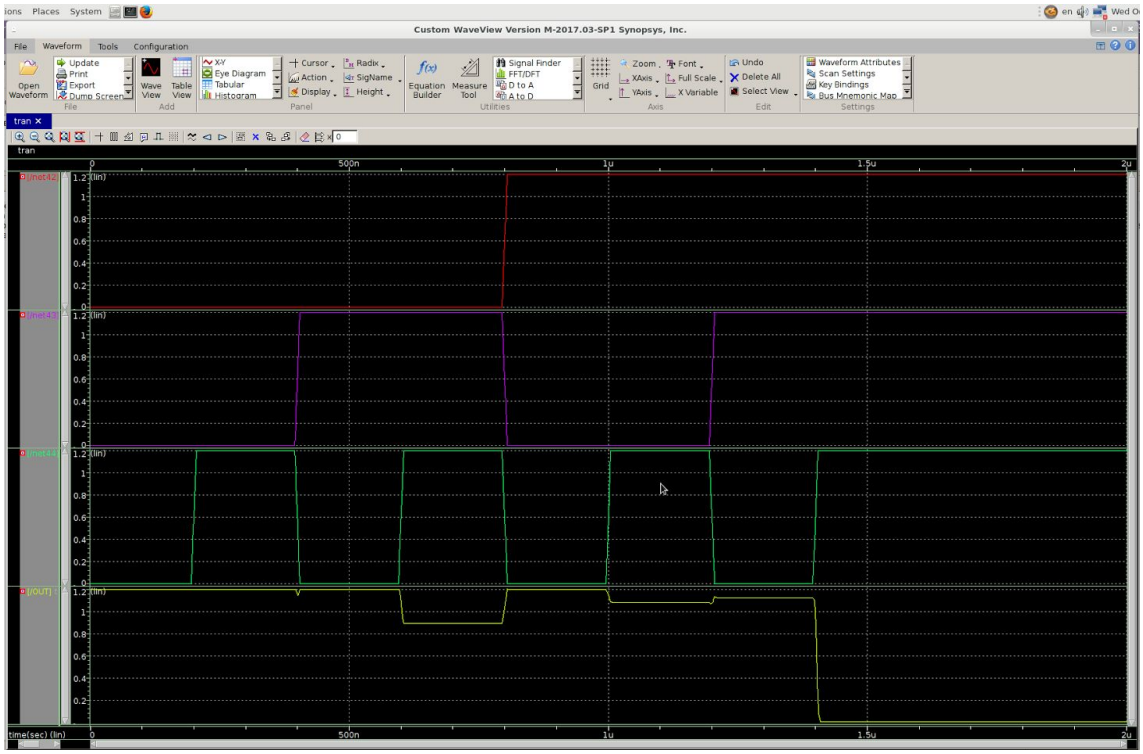

Figure 5. Simulation if we just have 8 bit for inputs

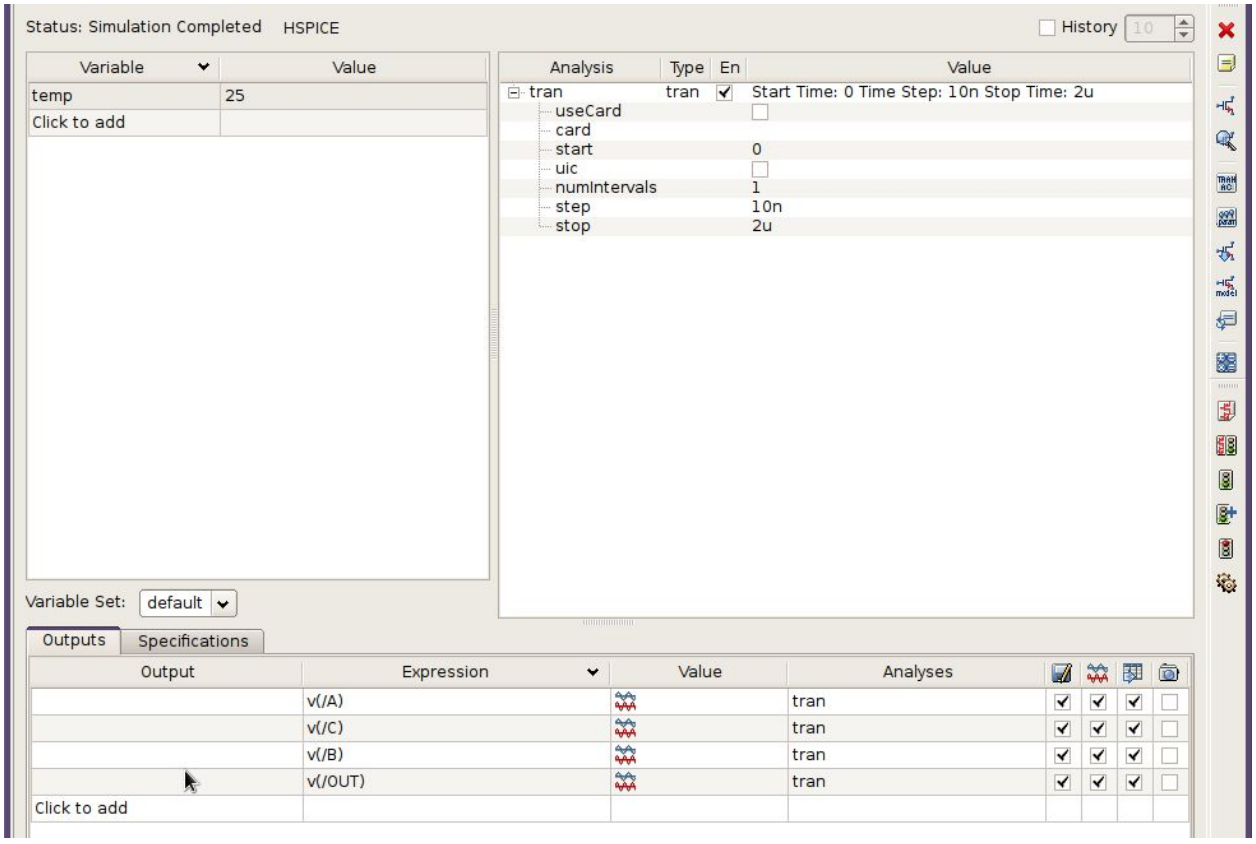

Figure 6. SAE setup for transient simulation

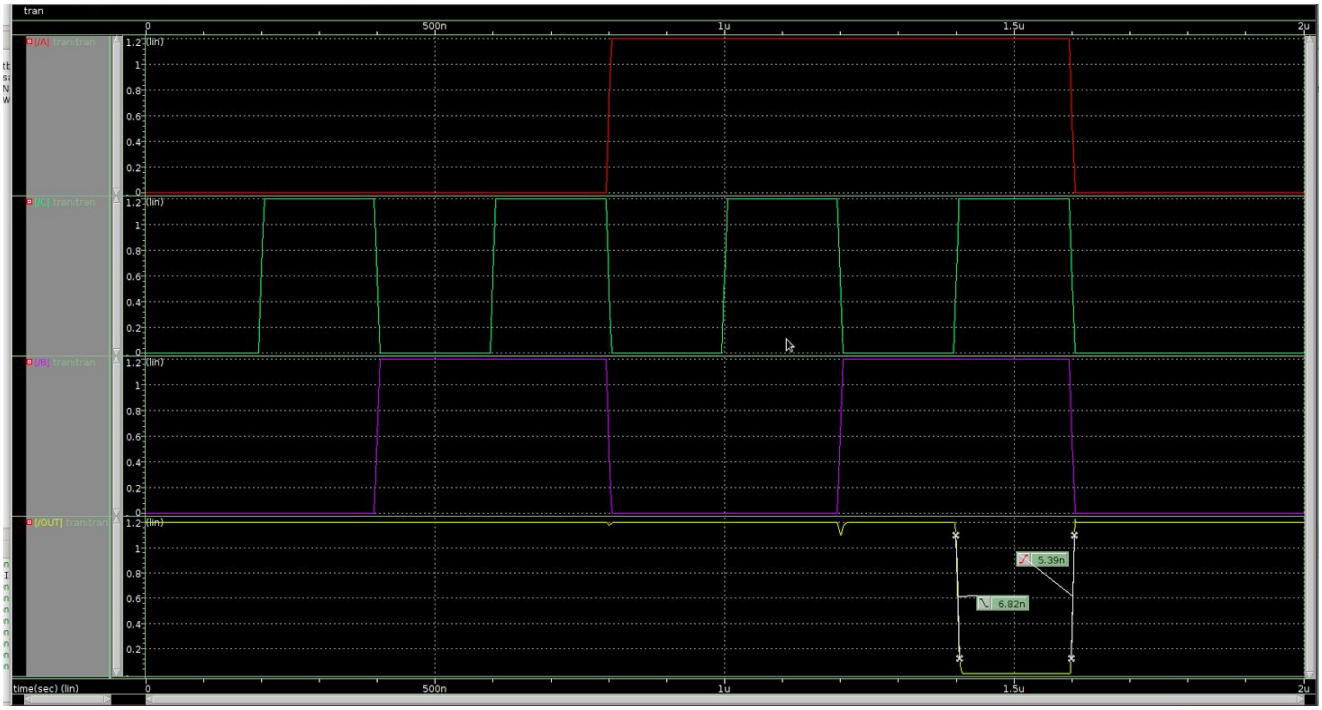

Figure 7. Transient simulation for the 3-input NAND gate

As we can see from Figure 7, rise time = 5.39ns, fall time = 6.82ns.

<u>Part C</u>: Voltage Transfer Characteristics

1. **Input A Sweep**

Setup the schematic as shown in Figure 8. In order to sweep only A, we need to setup a DC simulation in SAE, and sweep the voltage source connected to input A from 0 to 1.2 V. Before running the simulation, we need to change the plotting type in SAE so we can have many different plots in the same section. Even though I add box indicating which curve is from what kind of sweep, I will also use Table 2 to show it.

Table 2. Table indicating different kinds of sweep

Blue	Sweep A
Yellow	Sweep B
Red	Sweep A&B

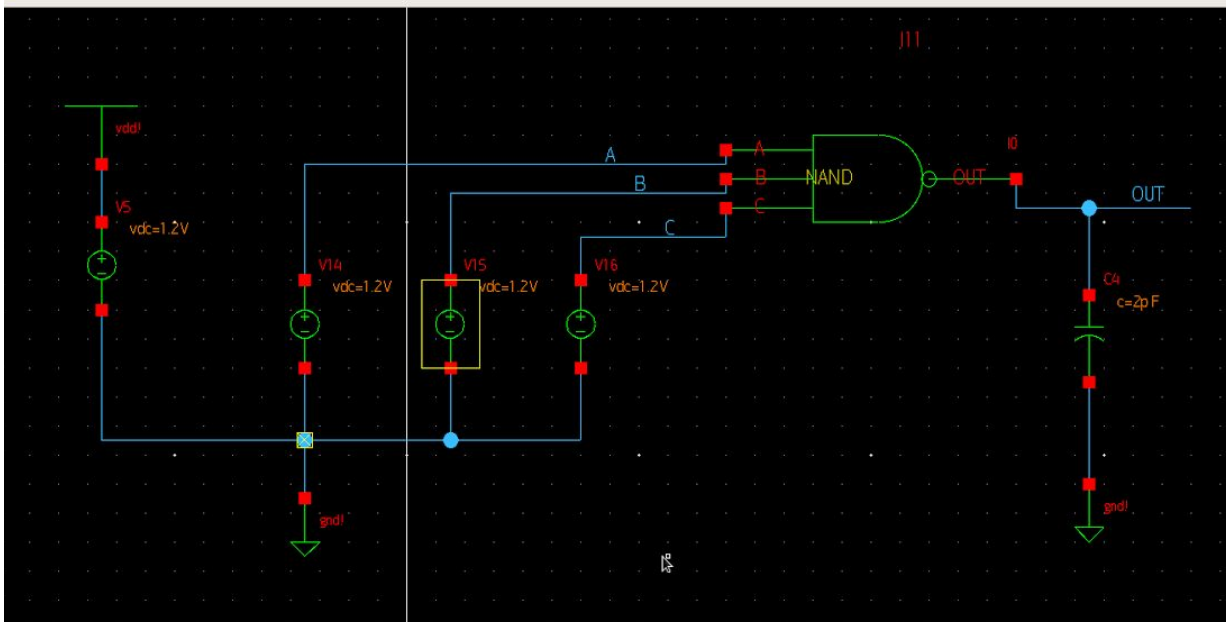

Figure 8. Schematic to Sweep A or B only

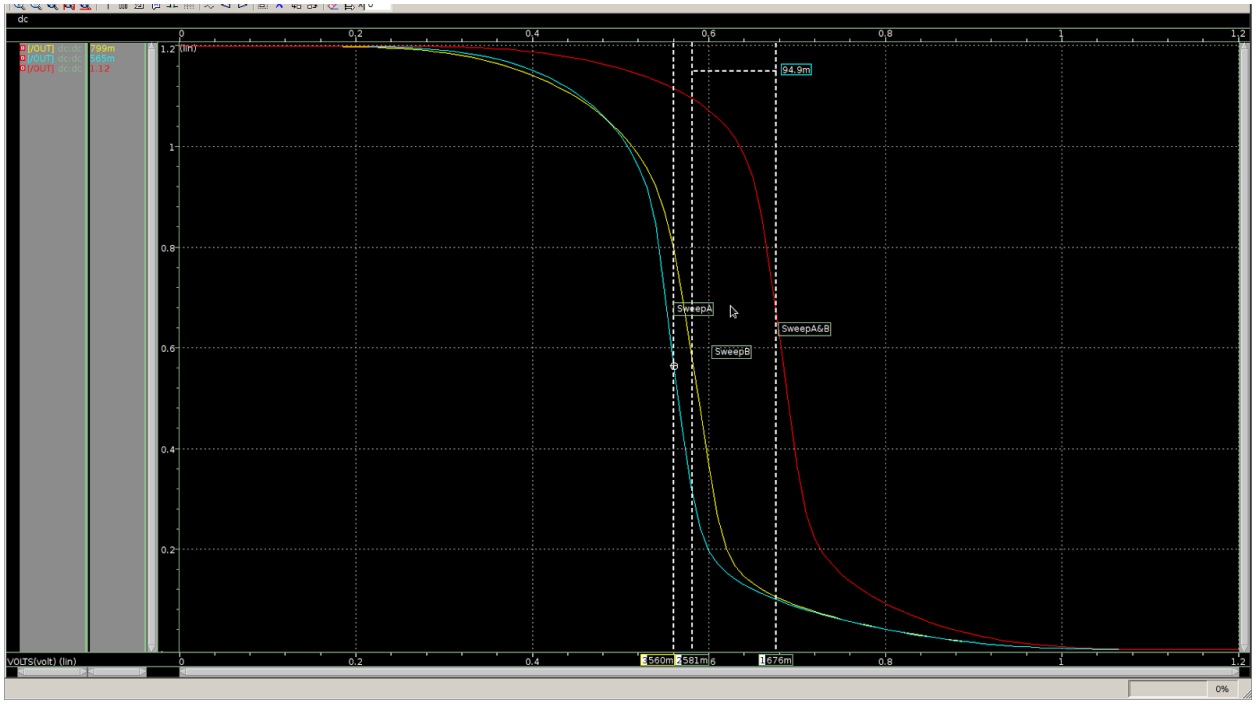

Figure 9. Waveform of input A sweep

Sometimes the cursor doesn't want to stay on one curve, so I took multiple screenshot for different V_M. As we can see from Figure 9, the closest V_M that I can get is V_M = 565 mV, in which V_{in} = 560 mV and V_{out} = 565 mV.

2. Input B Sweep

Repeat steps that we take to sweep input A for input B only.

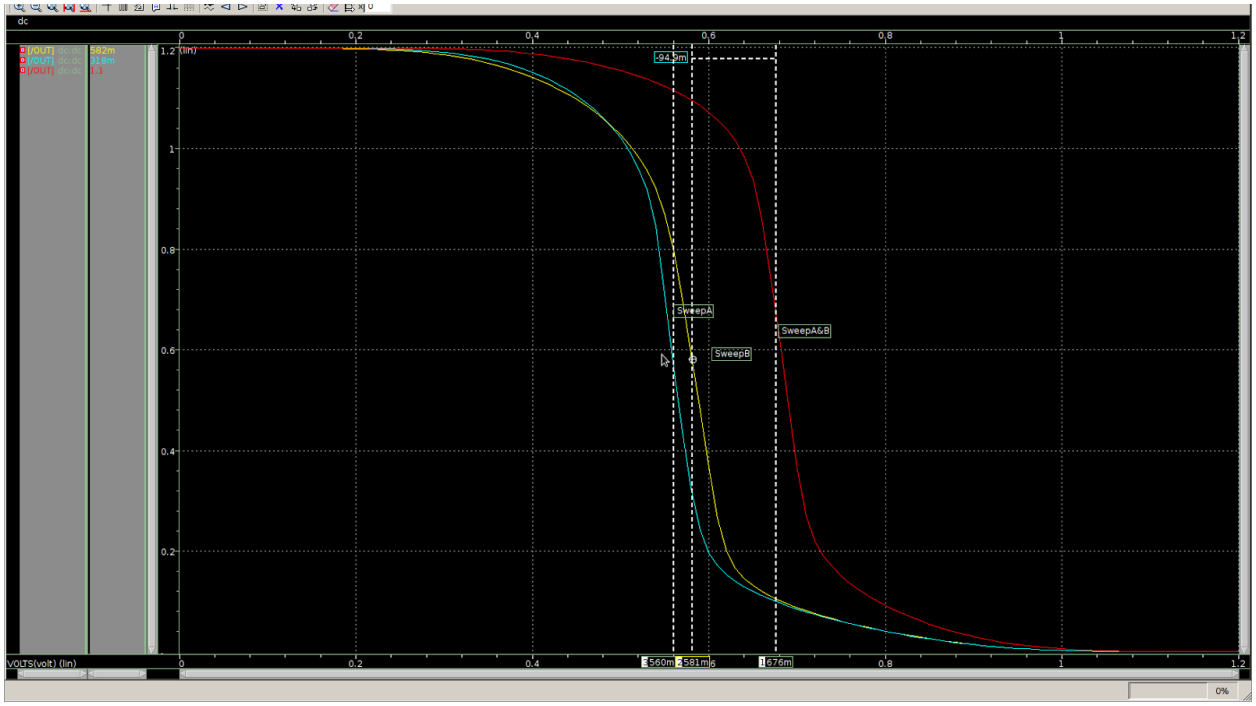

Figure 10. Waveform of input B sweep

From Figure 10, we can see that V_M = 582 mV, in which V_{in} = 581 mV and V_{out} = 582 mV. Obviously, V_M is different from sweep A.

3. Inputs A and B Sweep

In order to sweep both A and B, we connect both inputs to the same voltage source. Be careful to connect B directly to the red spot, or we will not be able to sweep A and B at the same time.

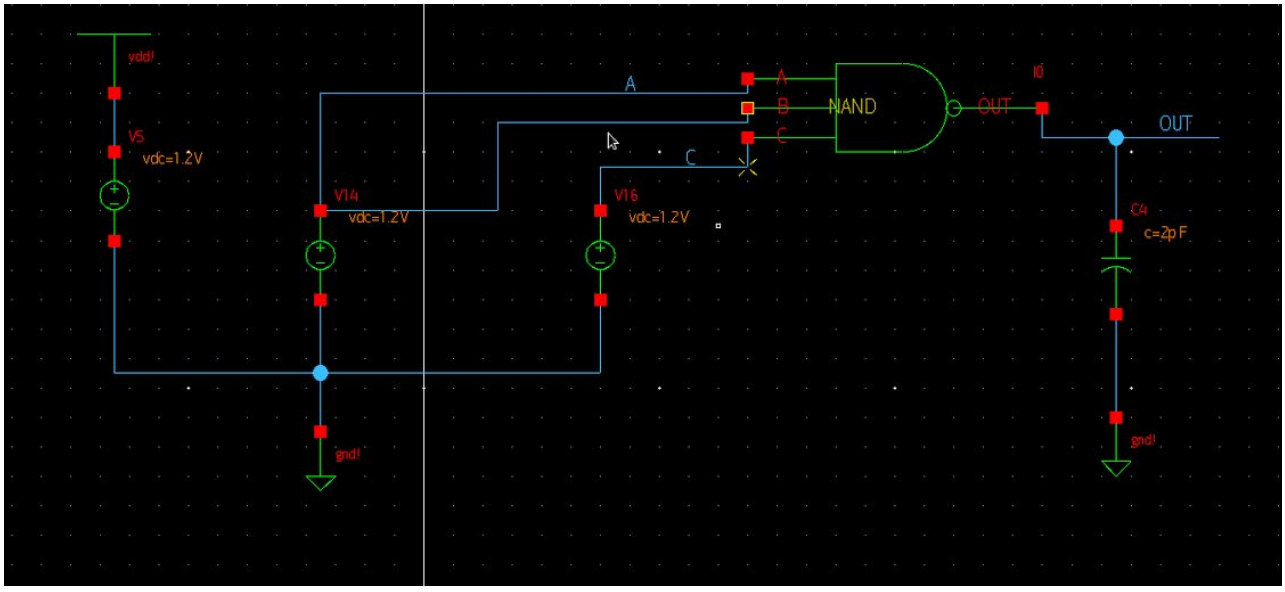

Figure 11. Schematic to sweep A and B

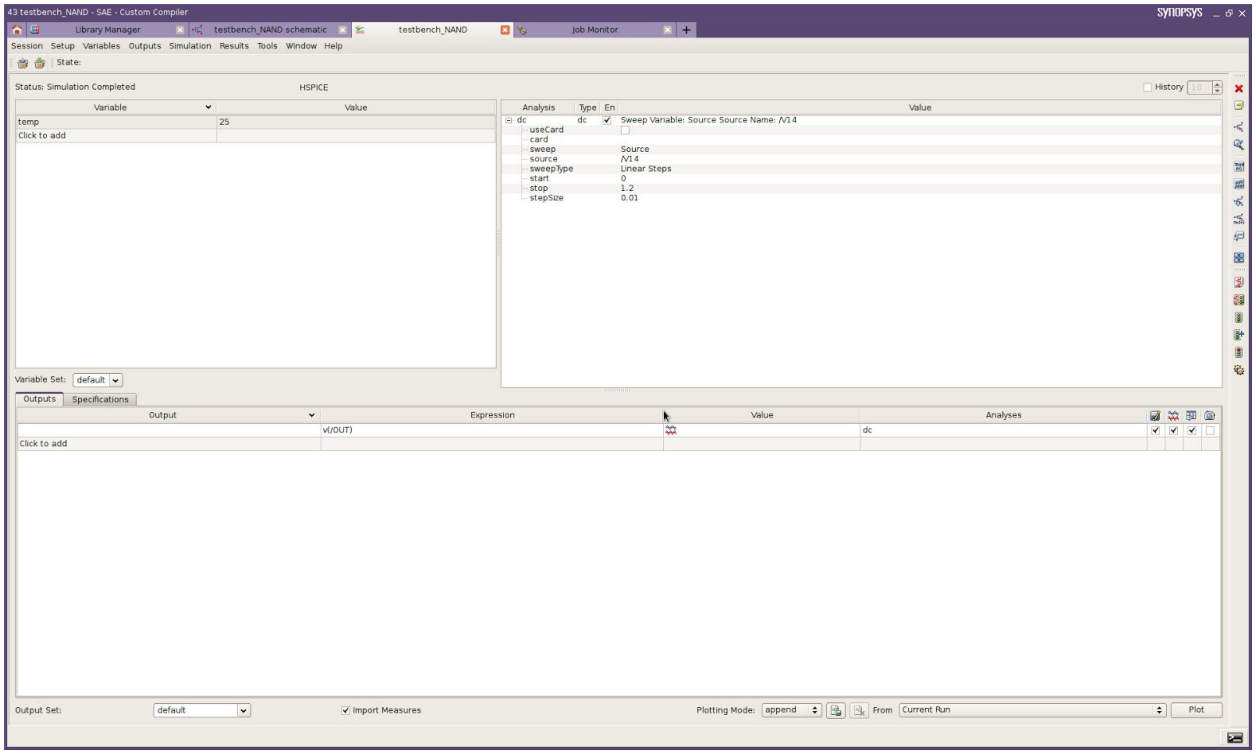

Figure 12. SAE setup for inputs A and B sweep

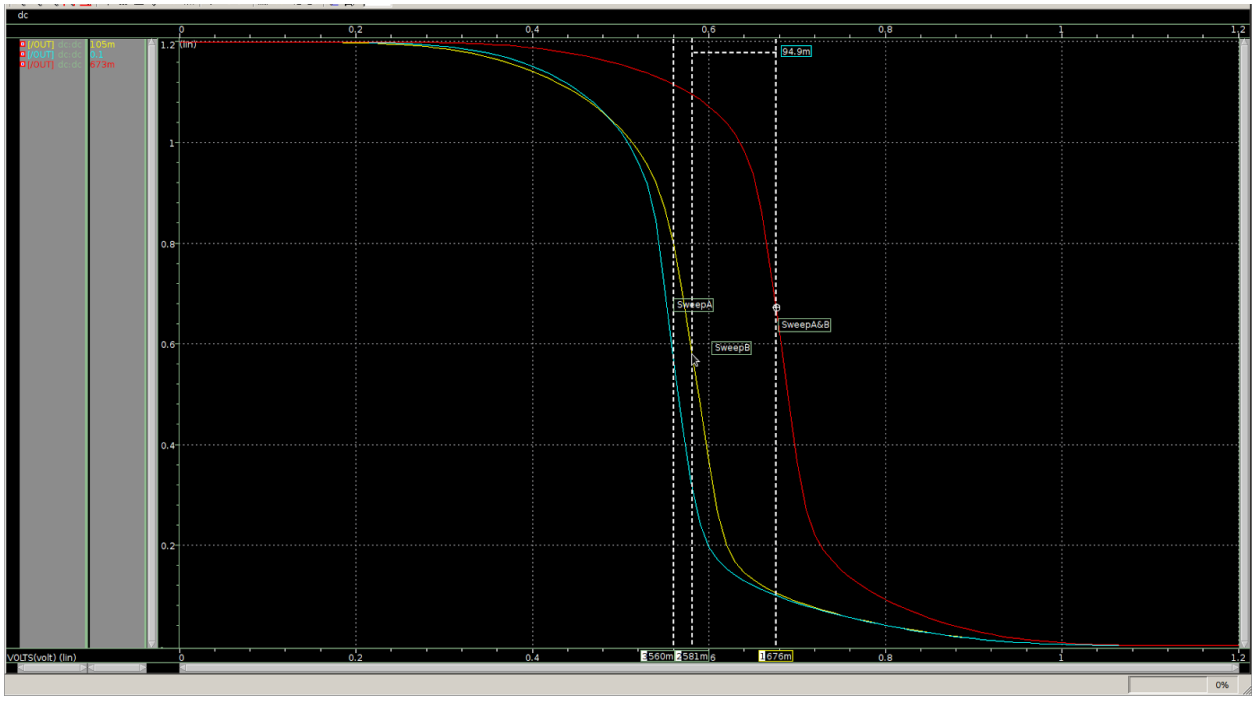

Figure 13. Waveform of inputs A and B sweep

From Figure 13, we can see that V_M = 676 mV, in which V_{in} = 673 mV and V_{out} = 676 mV.

Table 3. V_M to corresponding sweep

Sweep	V_M (mV)
A	565
B	582
A and B	676

III. CONCLUSION

In this lab, I learn how to create the schematic and symbol for a 3 input NAND gate. I also learn that the PMOS and NMOS device aspect ratio (W/L) can change fall and rise time. Also, in order to obtain rise time, we need to get into the second cycle by setting all inputs to low (at 0). When we are to sweep voltage source, we need to change from pattern sources Vpat into dc voltage, I struggle for quite a while figuring out this. The coolest thing that I learn in this lab is to change the color of the curve and add name tag for it. But I still need to work on the cursor more, because I don't know how to make the cursor remain on only one curve, so for the case that we have in Lab4, I don't need to take three different screenshots, I will only need one!