Assignment 4 - Pipeline Buffers

COEN 122L - Fall 2018
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Description

The purpose of a buffer is to receive data as an input, and pass the same data through to the next stage. By including buffers, we split our datapath into multiple stages that are each handling a different instruction. As a result, we can begin processing another instruction while others are still being processed and being passed down the datapath. This allows us to create a faster and more efficient datapath.

Assignment

In this lab, you will design the three pipeline buffers shown in figure 1, in Verilog. The buffers should receive a clock as an input, this way we can ensure that all the data is passed onto the next stage in unison.

Deliverables

To receive full credit, you will need to demo your working code. In addition, you must submit your source code (commented), your test-bench code (commented), and a screenshot of your waveform. To submit online, make sure everything is in a zipped folder (name the folder firstname_lastname.zip) and turn it into Camino. Please copy your code into individual .txt files and include those in the folder.

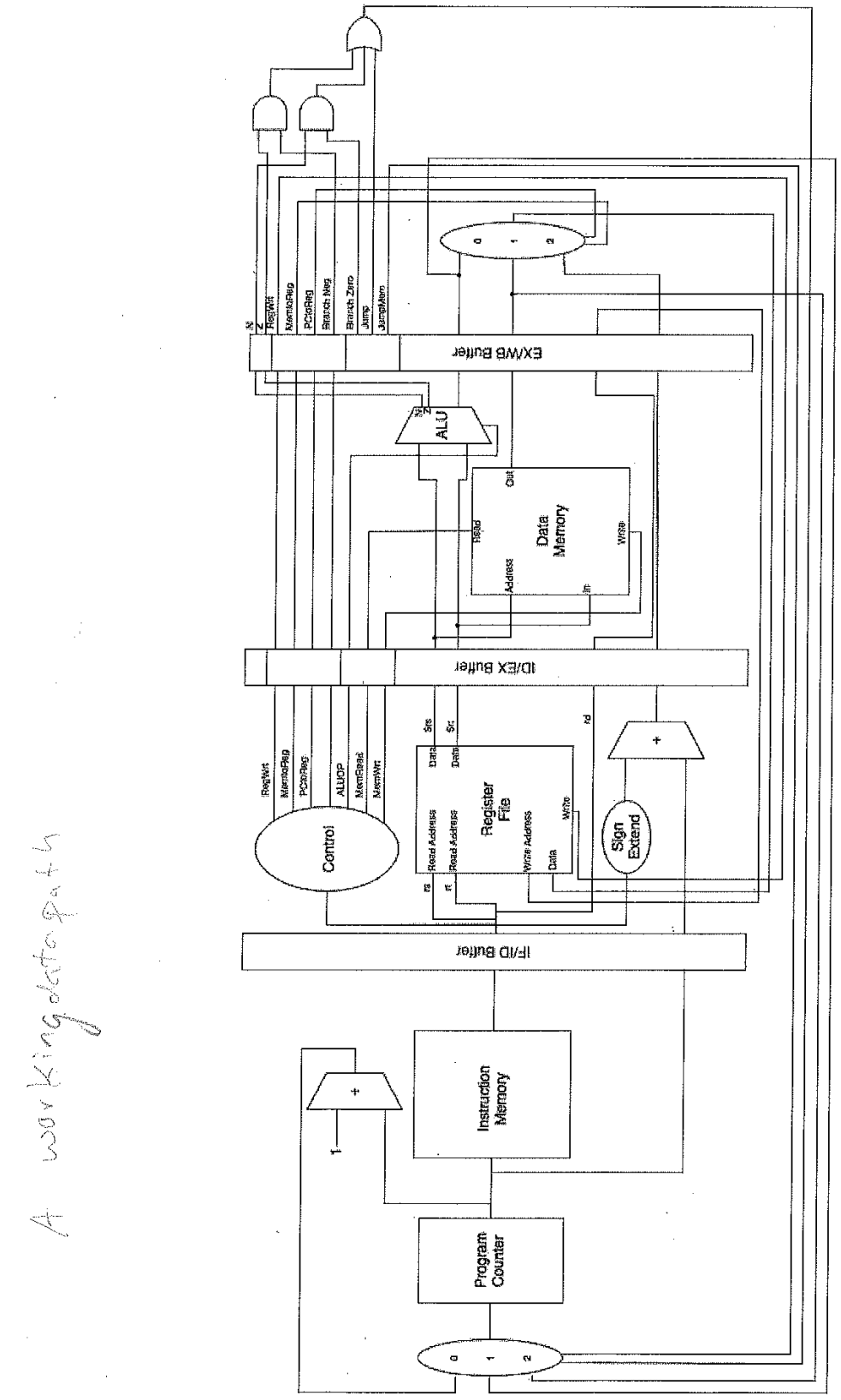

Figure 1: Working Datapath from Professor Shang