ELEN 153: Digital Integrated Circuit Des 59114

Lab 5: 3-Input NAND gate Layout

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I. OBJECTIVE

- To create a layout for the NAND gate and verify it with DRC and LVS.
- To perform parasitic extraction and post-layout simulations.

II. LAB PROCEDURE

1. NAND Layout

I use four materials to help me create the layout.

1. Schematic that I created in lab4
2. Tutorial part 2 on how to create the layout for a CMOS, which is my main source
3. My prelab
4. Design rules Excel sheet

But I make a mistake in my prelab, I have C as the input that is the closest to output, but what we should do is to have A as the closest input, and C should be grounded.

Some modifications needed compared to CMOS:

1. Because we have 3 inputs now, we should have larger nFET and pFET, whose size should follow what is on the schematic: W_n = 1.2 um and W_p = 1.2um, which will make nFET and pFET the same size.
2. Instead of just having 1 DIFFCON for nFET, having four in a row may make the connection better.
3. We should extend our inputs' PO so we can connect them with POLYCON and label the as A, B, and C. Be mindful that C should be the one connected to ground!

It is important to turn on visual DRD so we can know whether we do wrong when drawing the layout.

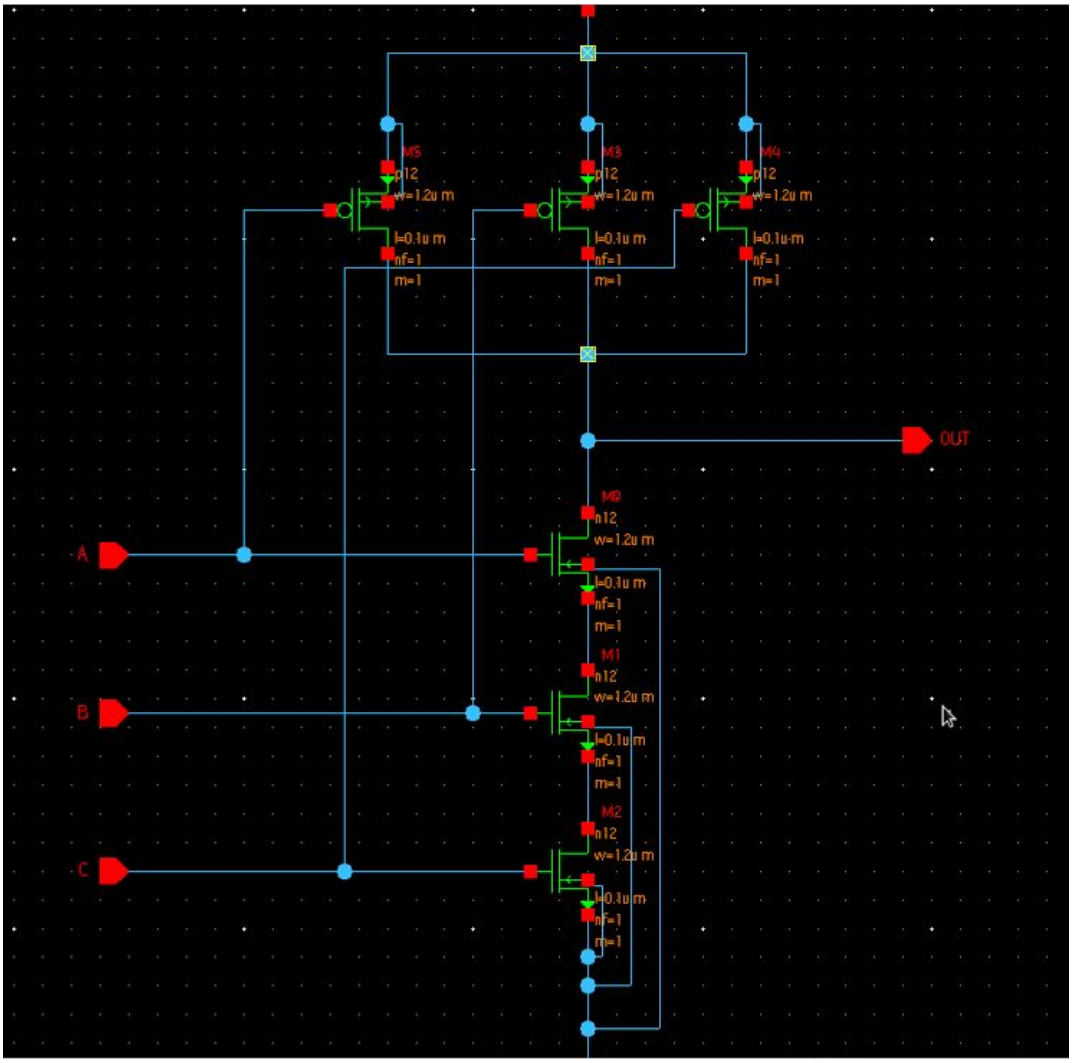

Figure 1. Schematic of 3-input NAND gate

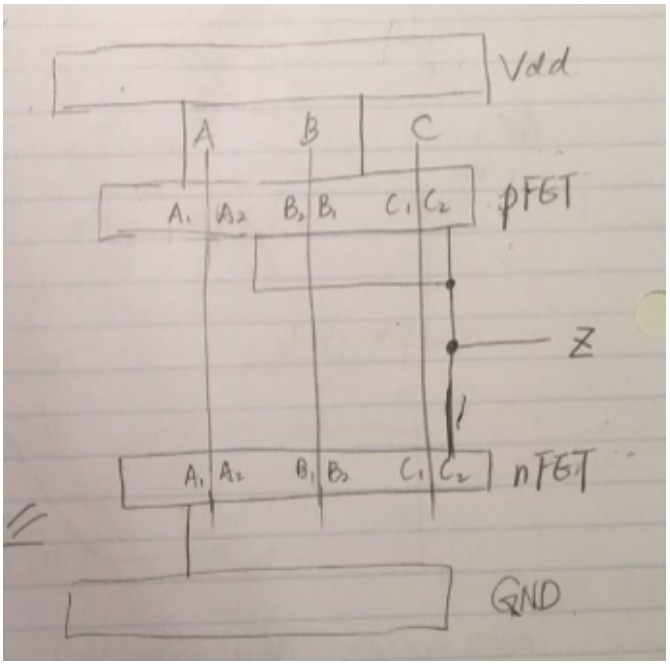

Figure 2. Stick diagram of 3-input NAND gate in my prelab

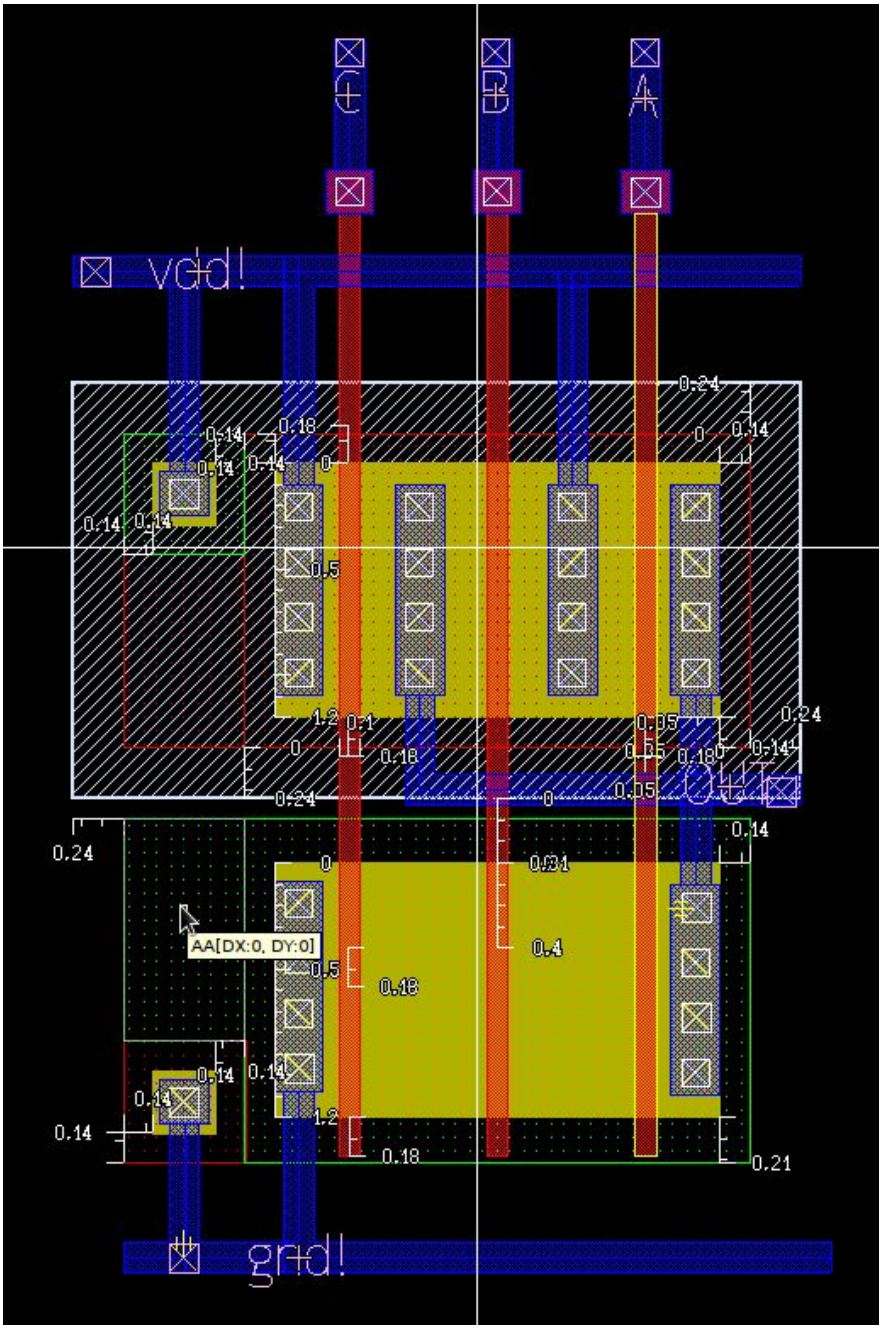

Figure 3. Layout of 3-input NAND

2. DRC and LVS

DRC

DRC confirms that the layout obeys all Design Rules required by this process, including rules for minimum spacing, minimum area or width, minimum enclosure etc. If any errors exist, it will tell you exactly what and where the error is.

Figure 4. DRC CLEAN

LVS

LVS confirms that the layout indeed matches the schematic which is intended to layout.

For the first time that I run LVS simulation, it fails and tells me that I have 2 unmatched ports, as shown in Figure 5. I didn't quite get it at first about the OUT and Vout, but I go back to my schematic and find out that I mistaken inputs A for C. The correct layout should be that input A is the closest one to the output, and input C is grounded. After changing A and C, I still have the OUT and Vout error, now I realize I have two different names for my output, so I change the output name in my layout into OUT, then my LVS simulation passes.

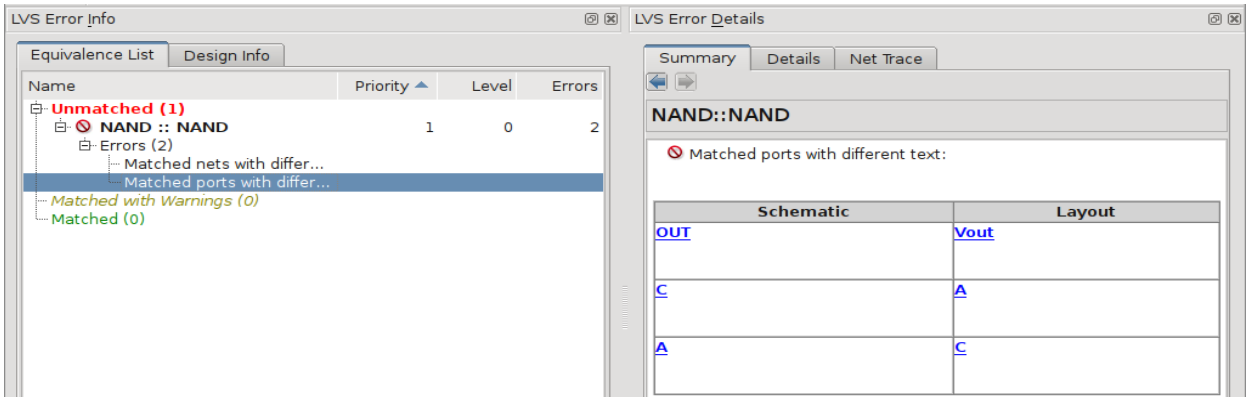

Figure 5. LVS FAIL

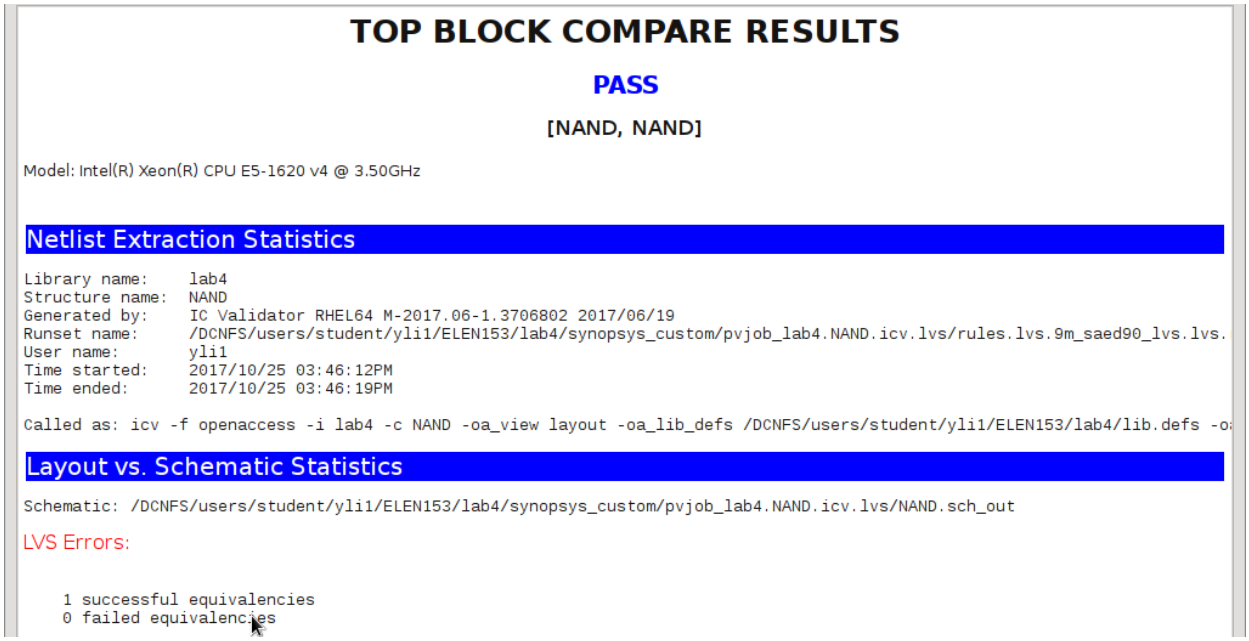

Figure 6. LVS PASS

Question: In order to reduce area and improve performance, I think I can:

1. make the distance from inputs B to C and from inputs B to A smaller, only to the degree that it obeys all rules.
2. have the inputs B and C not straight line, so we can have smaller nFET.

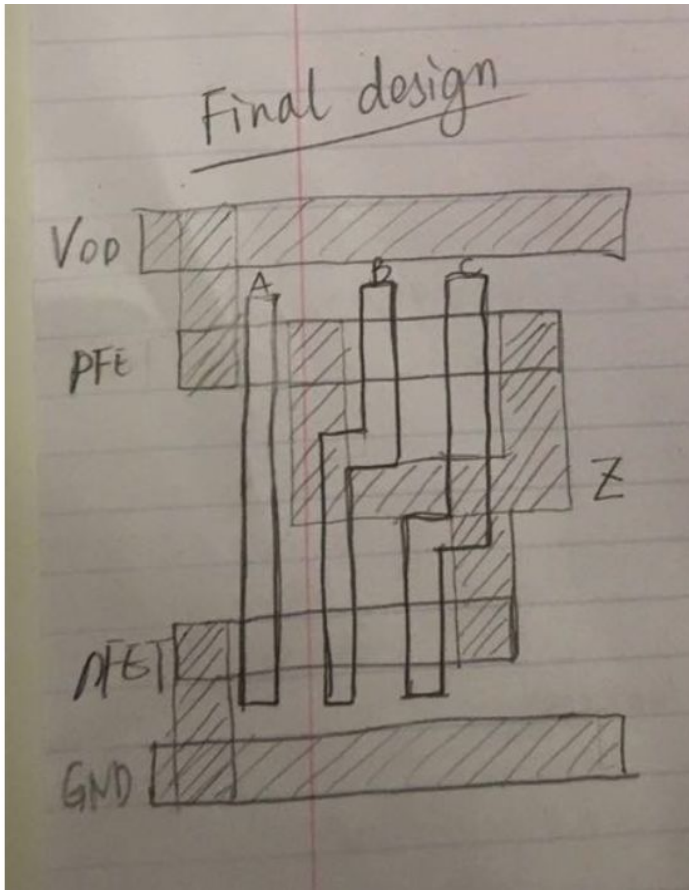

Figure 7. Idea from my prelab to reduce area

III. CONCLUSION

In this lab, I learn how to create the layout for the NAND gate based on the schematic that we created in the former lab. It is important that the ports should match in the schematic and in the layout. I also learn that, when seeing the tutorial for CMOS, we need to proportional increase the area/length or certain instances, and remain the same for some instances, for example, in NAND gate, we need to have width of pFET 4 times that of CMOS. However, simply multiplication will not be so efficient in minimizing area, but it is a good way to start. It is important to turn on visual DRD to check whether we have any error when we are creating the layout. Also, ruler is necessary, but should be deleted once that instance is finished or the final layout will look really messy. I was lucky that I haven't have any DRC FAIL, so I haven't really started on how to fix DRC errors. Having the experience of fixing LVS errors this time, I believe I will be more confident on fixing LVS errors in the future.