ELEN 153: Digital Integrated Circuit Des 59114

Lab 7: Hierarchical Design - Four-Bit Adder

Yutong Li

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Q1. List down the sizes that you used (just widths) for all the transistors in your circuit. (For both, the C²MOS latch and the inverters).

(1) Inverter with 1 pFET and 1 nFET

$W_p = 1.2um$ $L_p = 0.1um$ $W_n = 0.4um$ $L_n = 0.1um$

$W_n/L_n = 4$ $W_p/L_p = 12$

$k_n'(W_n/L_n) = 3*k_p'(4) = 12k_p'$ $k_p'(W_p/L_p) = 12k_p'$

(2) Inverter with 2 pFET and 2 nFET

$R \rightarrow ½R \rightarrow W/L \rightarrow 2W/L$

$W_n/L_n = 8$ $W_p/L_p = 24$

(3) Transistors of the C²MOS

In C²MOS, we have two pNET and two nNET in series, so in each pNET and each nNET,

$W_n/L_n = 16$ $W_p/L_p = 48$

Q2. Compare prelab waveform with your simulation result for the C²MOS latch without any inverters. What changes do you observe? Explain why you see those changes.

What is on the prelab is the ideal result of the C²MOS latch, but in "real life", in the waveform, we can see that even when we are not at the clock edge, Qs is changing, because the pFET and nFET in the latch are charging and discharging all the time despite the clock, which causes the output the change not exactly at the clock edge.

Q3. Why did we add pseudo-static inverter feedback loop? Does this create any potential hazard in the circuit?

Because of pseudo-static inverter feedback loop, Qs is able to change on the edge of clock because the loop of inverter is correcting 0 to 1, so it can always feed the correct value to the next latch, but wait, it is changing on the edge of CLKb, not we want from CLK!

Q4. Why did we add the third inverter?

With the third inverter, Qs can finally changes on the edge of CLK, and because we want even number of inverters totally, we need one more inverter at the end.

Q5. list down the setup time, hold time and clock to Q time that you measured for both, pre and post layout simulation. Do you see any difference between them? How would you explain the difference?

	Pre layout	Post layout
Setup time	22.5ps	36.9ps

Hold time	0	0
Clock to Q time	58ps	91.3ps

Hold time: 0 for both pre and post layout, because hold time is defined as the minimum amount of time after the clock's active edge during which data must be stable, so hold time remains 0
Setup time: Post layout is larger than pre layout, because setup time is defined as the minimum amount of time before the clock's active edge that the data must be stable for it to be latched correctly, since we have pseudo-static inverter feedback loop and a third inverter to have the output changes on the edge of CLK and make the sub threshold current as small as possible, the setup time for post layout should be large.
Clock to Q time: Post layout is larger than pre layout, because clock to Q delay/time is defined as the time needed to propagate 'Qm' to 'Q', equals to transmission gate delay + inverter delay, since we have more inverters in post layout, the clock to Q delay/time for post layout should be larger.