ELEN 153: Digital Integrated Circuit Desb 59114

Lab 3: CMOS Inverter Layout

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Wednesday 2:15-5:00pm 2017/10/11

I. OBJECTIVE

- To develop skills for CMOS layout using Synopsys Custom Compiler.
- To create an inverter layout and verify it using DRC and LVS.
- To perform parasitic extraction and post-layout simulation.

II. LAB PROCEDURE

1. Inverter Layout

Before beginning to draw out the layout, we need to turn on DRD since it can visually indicate any design rule violation live as we draw the layout. However, the instruction in the Tutorial doesn’t give the drop-down menu of DRD, instead of doing **Window→Toolbars→DRD** directly, we need to do **Tools→SDL**, press ok on the pop up, then go back to do **Window→Toolbars→DRD**. Next, open **Options->Display**, and turn on Dynamic and DX/DY so we can see X and Y measurement on the cursor as we draw.

Now we begin the layout. Note that the magnitude of every component needs to be exactly the same as told. When placing the Diffusion Contacts on PMOS, remember to enter “4” for the number of rows or there will be error if you try to add one by one.

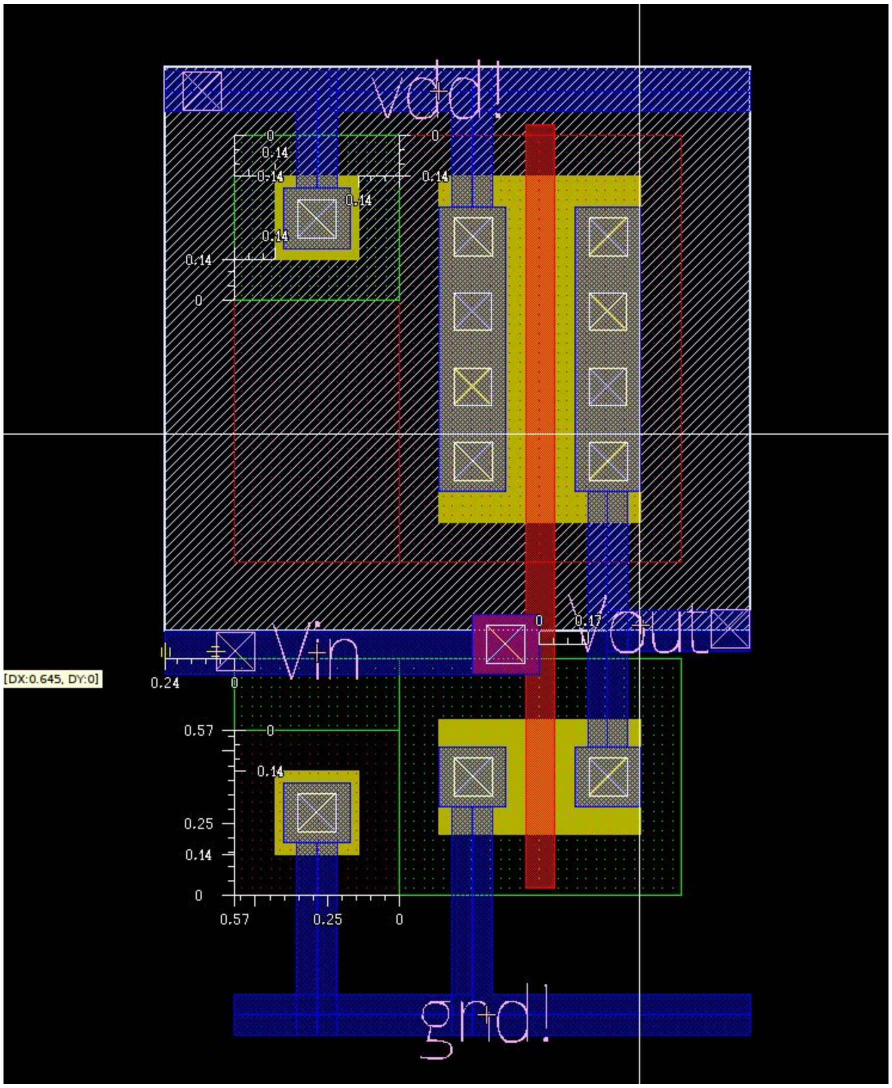


Figure 1. Final design of CMOS inverter layout

Table 1. Layout layers and their corresponding name in Synopsys tools

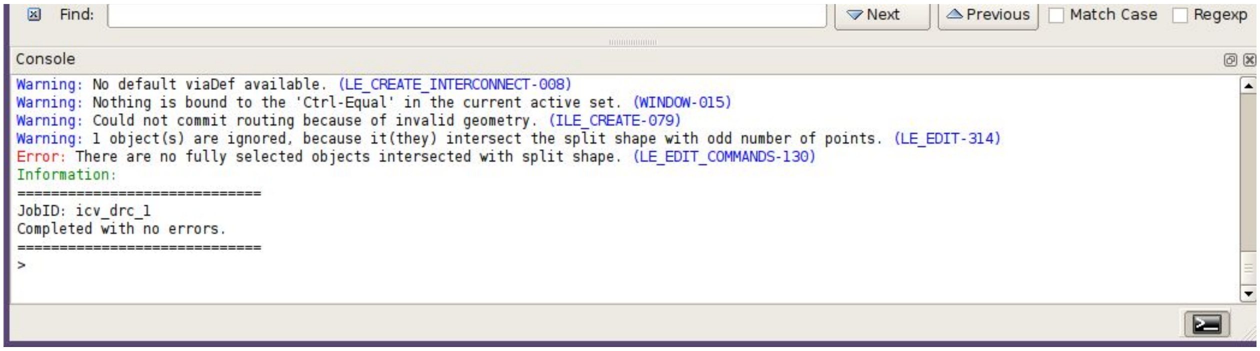
Layout layers	Corresponding name in Synopsys tools
N-Well	NWELL
N+ Implantation	NIMP
P+ Implantation	PIMP
Diffusion	DIFF
Poly Silicon	PO

Metal 1	M1
Metal 2	M2
Metal 1 Pin	M1PIN

2. DRC and LVS

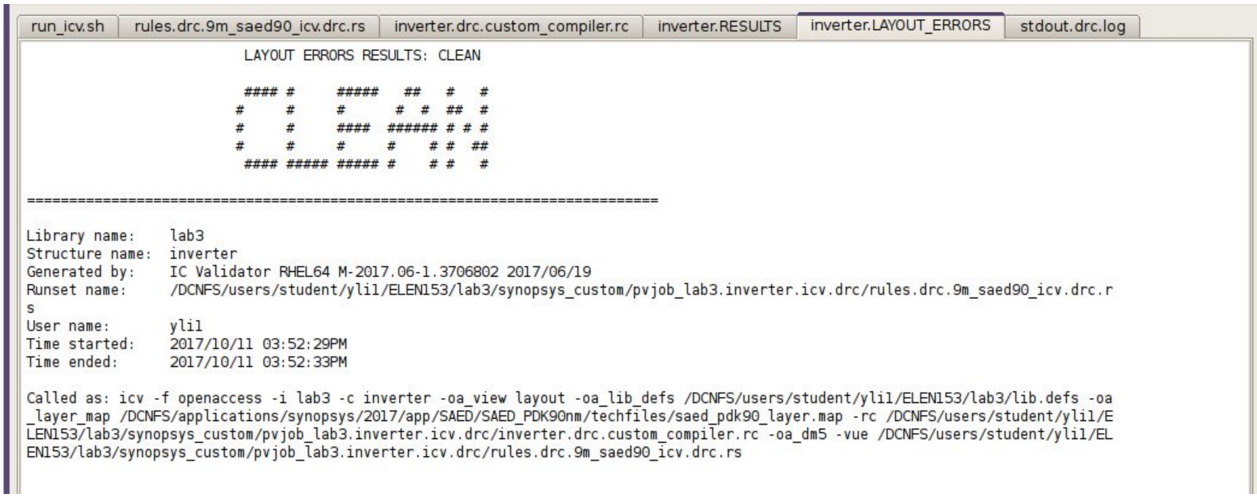
Design Rule Check(DRC)

Select **Verification→DRC→Run**. The text view will pop-up to show the progress of the DRC. If the layout is correct in terms of rules, the screen should match Figure 3.



```
Warning: No default viaDef available. (LE_CREATE_INTERCONNECT-008)
Warning: Nothing is bound to the 'Ctrl-Equal' in the current active set. (WINDOW-015)
Warning: Could not commit routing because of invalid geometry. (ILE_CREATE-079)
Warning: 1 object(s) are ignored, because it(they) intersect the split shape with odd number of points. (LE_EDIT-314)
Error: There are no fully selected objects intersected with split shape. (LE_EDIT_COMMANDS-130)
Information:
=============================
JobID: icv_drc_1
Completed with no errors.
=============================
>
```

Figure 2. Console indicating no errors

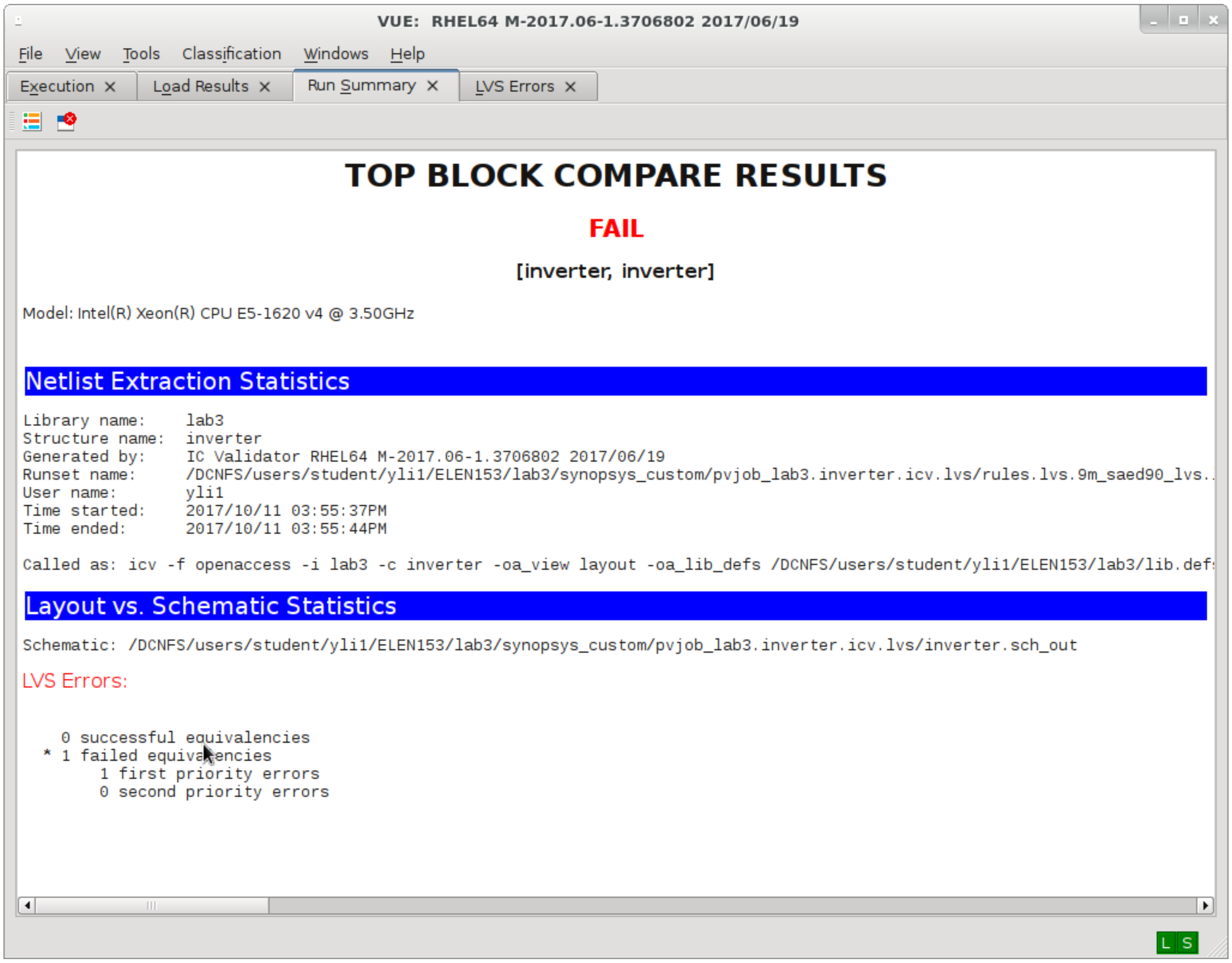


```
                            LAYOUT ERRORS RESULTS: CLEAN

                            #### #     #####   ##   #   #
                           #     #     #      #  #  ##  #
                           #     #     ####  ###### # # #
                           #     #     #     #    # #  ##
                            #### ##### ##### #    # #   #

=============================================================================

Library name:    lab3
Structure name:  inverter
Generated by:    IC Validator RHEL64 M-2017.06-1.3706802 2017/06/19
Runset name:     /DCNFS/users/student/ylil/ELEN153/lab3/synopsys_custom/pvjob_lab3.inverter.icv.drc/rules.drc.9m_saed90_icv.drc.r
s
User name:       ylil
Time started:    2017/10/11 03:52:29PM
Time ended:      2017/10/11 03:52:33PM

Called as: icv -f openaccess -i lab3 -c inverter -oa_view layout -oa_lib_defs /DCNFS/users/student/ylil/ELEN153/lab3/lib.defs -oa
_layer_map /DCNFS/applications/synopsys/2017/app/SAED/SAED_PDK90nm/techfiles/saed_pdk90_layer.map -rc /DCNFS/users/student/ylil/E
LEN153/lab3/synopsys_custom/pvjob_lab3.inverter.icv.drc/inverter.drc.custom_compiler.rc -oa_dm5 -vue /DCNFS/users/student/ylil/EL
EN153/lab3/synopsys_custom/pvjob_lab3.inverter.icv.drc/rules.drc.9m_saed90_icv.drc.rs
```

Figure 3. inverter.LAYOUT_ERRORS

Layout Vs. Schematic (LVS)

Select **Verification→LVS→Run**. At first, on the pop-up VUE window I got FAIL, as shown in Figure 4.


VUE: RHEL64 M-2017.06-1.3706802 2017/06/19
File View Tools Classification Windows Help
Execution ✕
Load Results ✕
Run Summary ✕
LVS Errors ✕
L S

TOP BLOCK COMPARE RESULTS

FAIL

[inverter, inverter]

Model: Intel(R) Xeon(R) CPU E5-1620 v4 @ 3.50GHz

Netlist Extraction Statistics

```
Library name:     lab3
Structure name:   inverter
Generated by:     IC Validator RHEL64 M-2017.06-1.3706802 2017/06/19
Runset name:      /DCNFS/users/student/yli1/ELEN153/lab3/synopsys_custom/pvjob_lab3.inverter.icv.lvs/rules.lvs.9m_saed90_lvs.
User name:        yli1
Time started:     2017/10/11 03:55:37PM
Time ended:       2017/10/11 03:55:44PM

Called as: icv -f openaccess -i lab3 -c inverter -oa_view layout -oa_lib_defs /DCNFS/users/student/yli1/ELEN153/lab3/lib.def
```

Layout vs. Schematic Statistics

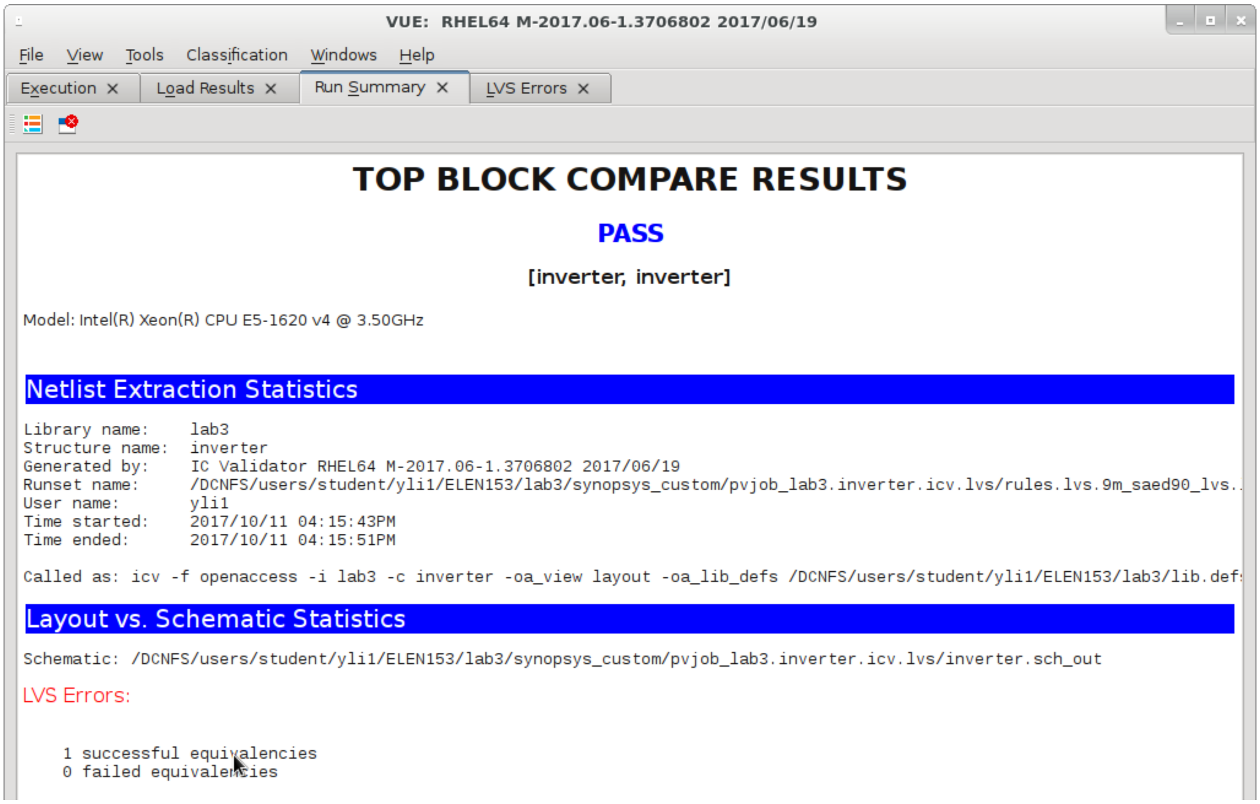
```
Schematic: /DCNFS/users/student/yli1/ELEN153/lab3/synopsys_custom/pvjob_lab3.inverter.icv.lvs/inverter.sch_out
```

LVS Errors:

```
    0 successful equivalencies
  * 1 failed equivalencies
        1 first priority errors
        0 second priority errors
```

Figure 4. VUE indicating failing LVS

Then, I learn that it fails because I didn't have this layout in the same folder that holds the schematic and symbol for CMOS inverter. In order to solve this, the TA suggests and helps me build another schematic and symbol in the current file. After this modification, I got PASS.



TOP BLOCK COMPARE RESULTS

PASS

[inverter, inverter]

Model: Intel(R) Xeon(R) CPU E5-1620 v4 @ 3.50GHz

Netlist Extraction Statistics

```
Library name:    lab3
Structure name:  inverter
Generated by:    IC Validator RHEL64 M-2017.06-1.3706802 2017/06/19
Runset name:     /DCNFS/users/student/yli1/ELEN153/lab3/synopsys_custom/pvjob_lab3.inverter.icv.lvs/rules.lvs.9m_saed90_lvs..
User name:       yli1
Time started:    2017/10/11 04:15:43PM
Time ended:      2017/10/11 04:15:51PM

Called as: icv -f openaccess -i lab3 -c inverter -oa_view layout -oa_lib_defs /DCNFS/users/student/yli1/ELEN153/lab3/lib.def
```

Layout vs. Schematic Statistics

```
Schematic: /DCNFS/users/student/yli1/ELEN153/lab3/synopsys_custom/pvjob_lab3.inverter.icv.lvs/inverter.sch_out
```

LVS Errors:

```
    1 successful equivalencies
    0 failed equivalencies
```

Figure 5. VUE indicating passing LVS

3. LPE and Post-Layout Simulation

Select **Verification→LPE→Setup and Run**. In the **Extraction Options** bar, include Tutorial_final_2017/synopsys_custom/pvjob_Tutorial.inverter.icv.lvs/pex_runset_report to the Runset report file.

When LPE is completed successfully, the inverter starrc view will pop-up to show the Layout parasitics on the layout as shown in Figure 6. Zoom-in so we can see there are many resistors and capacitances.

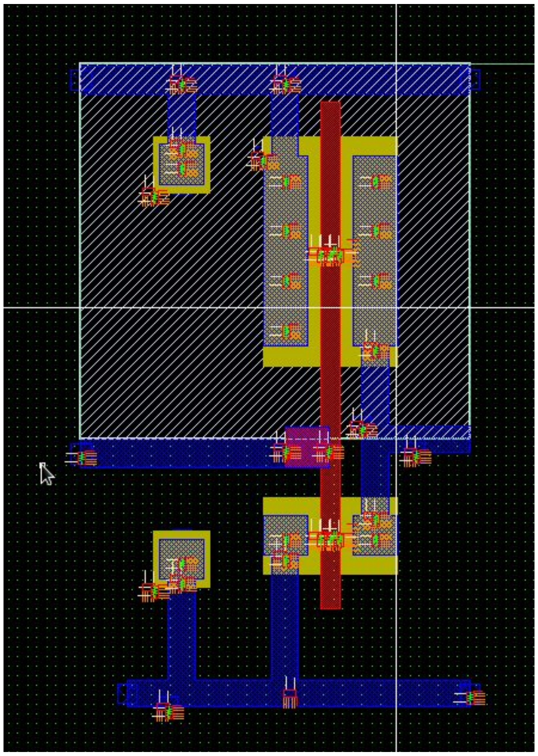


Figure 6. Inverter starrc view

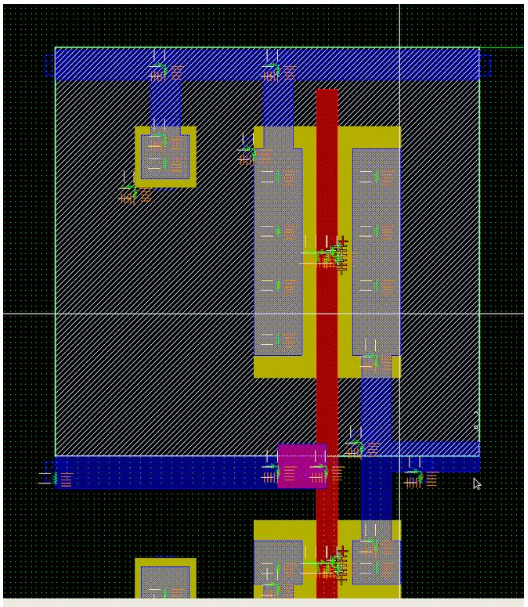


Figure 7. Detail of Figure 6

In order to do the Post-Layout Simulations, we need to create a new cellview for the testbench_inverter cell named config. Type **schematic hspice** in View Search List. Then click on the empty space under the Selected Column corresponding to the inverter, and select the **starrc** view. Then load the config state on **SAE**, perform a transient simulation, and select **append** in the Plotting Mode drop-down menu, in order to superimpose pre- and post-layout simulations.

Keep the WaveView of pre-layout simulation in order to compare with that of post-layout simulation. Change the design from config view back to schematic view to run post-layout simulation. The input and output waveforms for the pre-layout simulation will be appended to the WaveView window as shown in Figure 9.

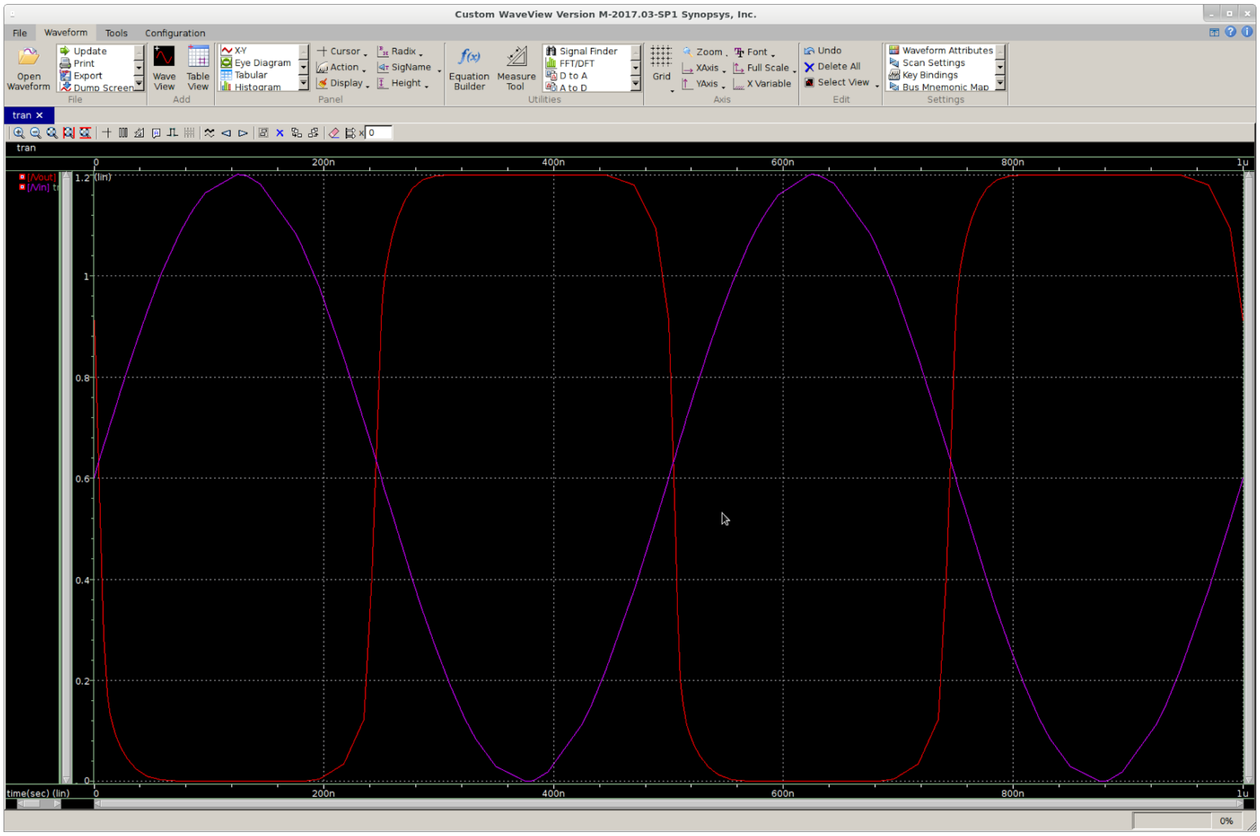


Figure 8. Pre-layout simulation waveform

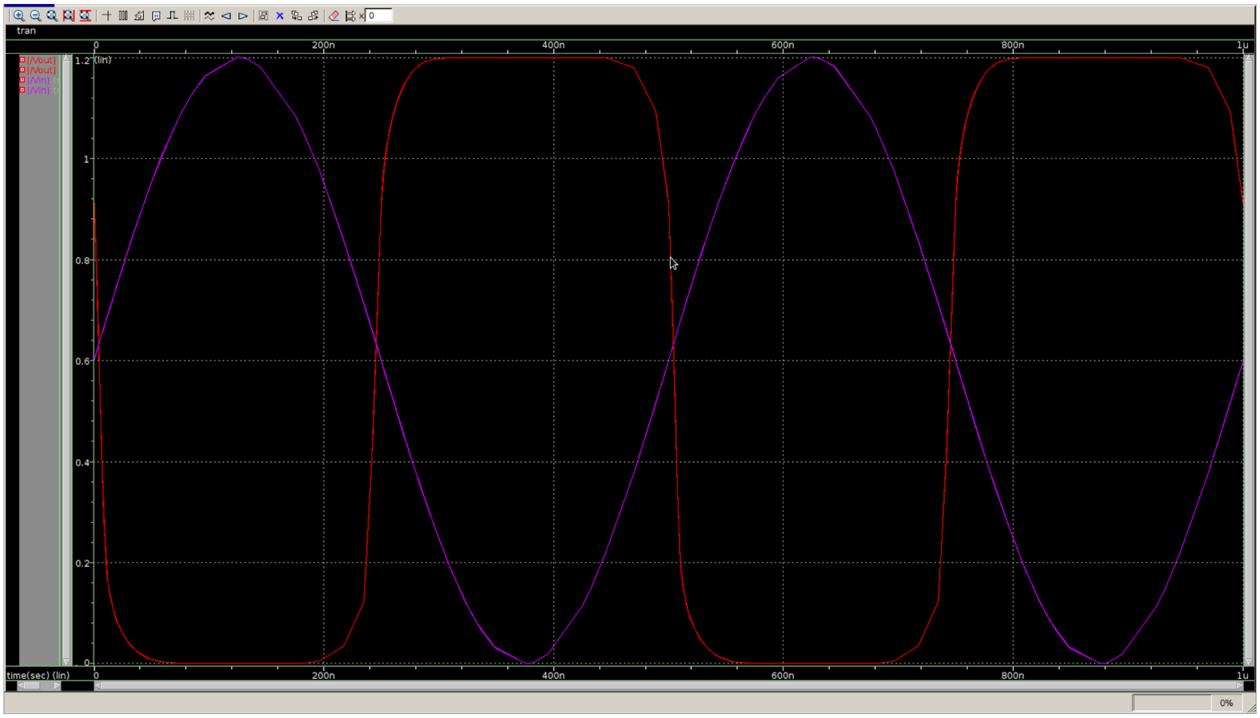
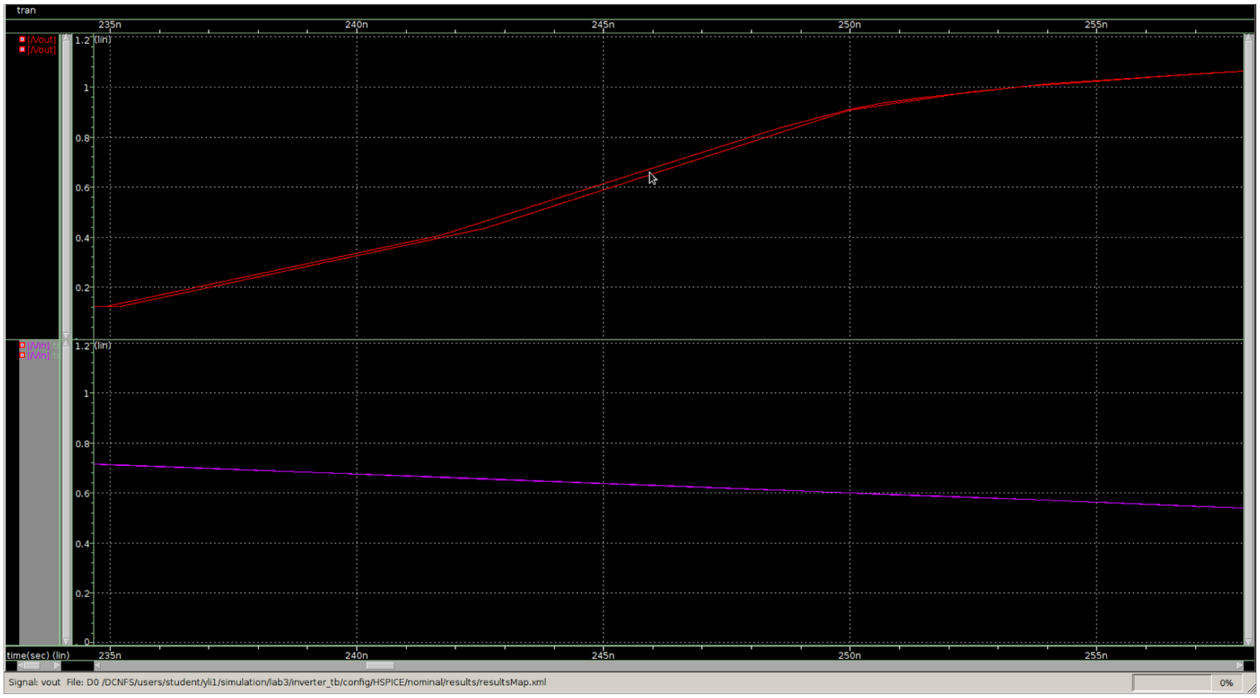


Figure 9.Post-layout simulation waveform

First, ungroup the waveforms to have 4 waveforms. Then group them so we have 2 groups: Vout and Vin, as shown in Figure 10.



Signal: vout File: D0 /DCNFS/users/student/yli1/simulation/lab3/inverter_tb/config/HSPICE/nominal/results/resultsMap.xml

Figure 10. Waveform after ungrouping and grouping

We can see that the two waveforms of Vout are not identical, because of the resistors and capacitances. In our case, the number of capacitances is not huge, so the difference is small and neglectable.

III. CONCLUSION

In this lab, I learn how to create CMOS layout, verify it using DRC and LVS, and perform parasitic extraction and pre- and post-layout simulations, and notice the difference through waveform. I also learn that when creating the layout, we should be very strict about the magnitude so that we can have the layout function. During the lab, because I didn't build the layout in the same folder that holds the symbol and schematic for the CMOS inverter, I had to either rebuild the schematic and symbol in the current file, or rebuild the layout in the former folder. The TA suggested the first option, and helped me a lot with it. Also, I learnt that I forgot to add the model files again. After including the path, $SAED90_PDK/hspice, and select TT_12, I was able to run and get the desired waveform and results.