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ELEN21L_lab3

The design process:

1. Review lecture material on K-maps and logic design.
2. Read the problem statement and clearly identify the inputs and outputs for the circuit you are designing.

Inputs: CS, LS, RS, RR
Outputs: CL, LL, RL

3. From the problem statement, write algebraic expression for the traffic controller outputs.

CS	LS	RS	RR	CL	LL	RL
0	0	0	0	0	0	1
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

4. Create K-maps for the functions and find the minimized SOP implementation using AND and OR logic gates with as many inputs as needed.

SOP refers to minterms.

Let CS be a, LS be b, RS be c, and RR be d.

(CS,LS)\(RS,RR)	00	01	11	10
00	0	0	0	0
01	1	1	1	0
11	0	0	0	0
10	0	0	0	0

K-map for LL
f = a'bc' + a'bd

(CS,LS)\(RS,RR)	00	01	11	10
00	1	1	1	1
01	0	0	0	1
11	0	0	0	0
10	0	0	0	0

K-map for RL
f = a'b' + a'cd'

(CS,LS)\(RS,RR)	00	01	11	10
00	0	0	0	0
01	0	0	0	0
11	1	1	1	1
10	1	1	1	1

K-map for CL
f = a

	00	01	11	10
00	1	1	0	0
01	0	0	0	0

11	0	0	0	0
10	0	0	0	0

a’b’c’

5. Find minimized logic function in POS form.

For LL
f’ = b’ + cd’ + a
f = a’b(c’ + d)
For RL
f’ = a + bc’ + bd
F = a’(b’ + c)(b’ + d)
For CL
f’ = a’
f = a

6. Compare the cost of the POS form and the SOP form when the cost is measured by the sum of the number of logic gates and the number of inputs to all logic gates.

For LL, we will need 2 AND gates, 1 OR gates, and 3 NOT gates so 6 gates in total in SOP form, and we will need 1 AND gates, 1 OR gates, and 2 NOT gates so 4 gates in total in POS form.
For RL, we will need 2 AND gates, 1 OR gates, and 4 NOT gates so 7 gates in total in SOP form, and we will need 1 AND gates, 2 OR gates, and 4 NOT gates so 7 gates in total in POS form.
For CL, we will need 0 AND gates, 0 OR gates, and 0 NOT gates so 0 gate in total in SOP form, and we will need 0 AND gates, 0 OR gates, and 0 NOT gates so 0 gate in total in POS form.