SANTA CLARA UNIVERSITY	ELEN 153 Fall 2017	Dr. S. Krishnan
Pre-Lab #2: The CMOS Inverter		

For the MOS devices in 90nm technology use the parameters listed below.
NMOS: V_{tn0}= 0.39V, k_n' = 200μA/V^2, γ_n= 0, λ_n=0
NMOS: V_{tn0}= 0.27V, k_p' = 60μA/V^2, γ_p= 0, λ_p=0

V_{DD} = 1.2V.
The V_{IH} = 0.8V and V_{IL} = 0.5V.

(a) Draw the VTC for this inverter.
(b) Give the logic swing and noise margins for this inverter?
(c) What is the power consumed by this inverter:
  (i) when the input = 0V?
  (ii) when the inverter drives the output from "0" to "1" with load capacitance of 1pF at a clock frequency of 100MHz.