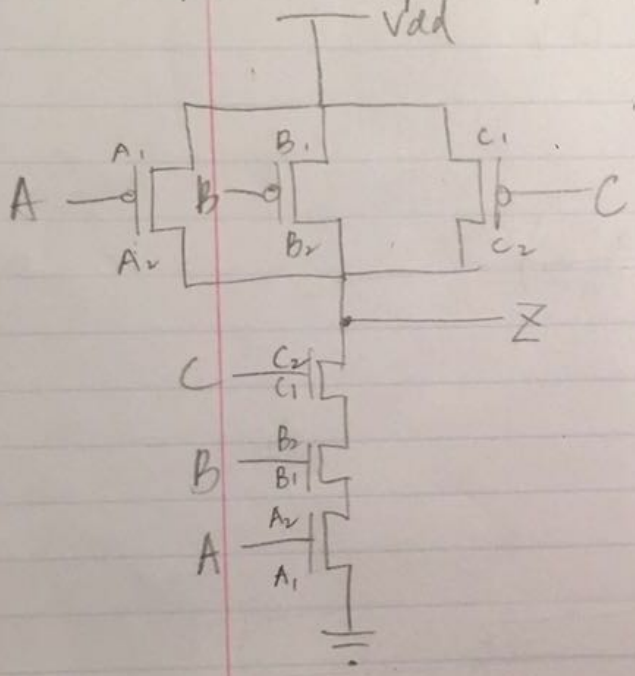
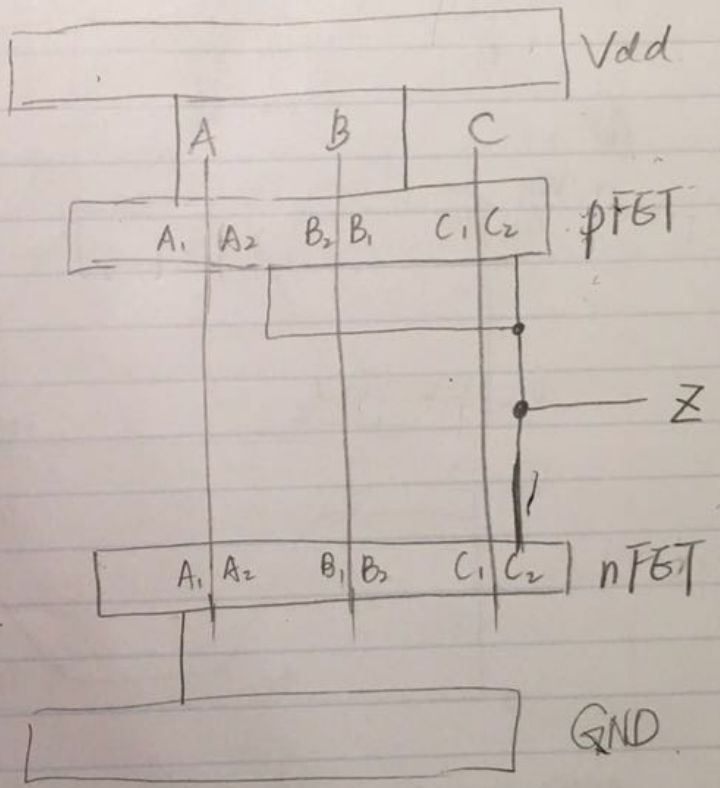
Prelab 5

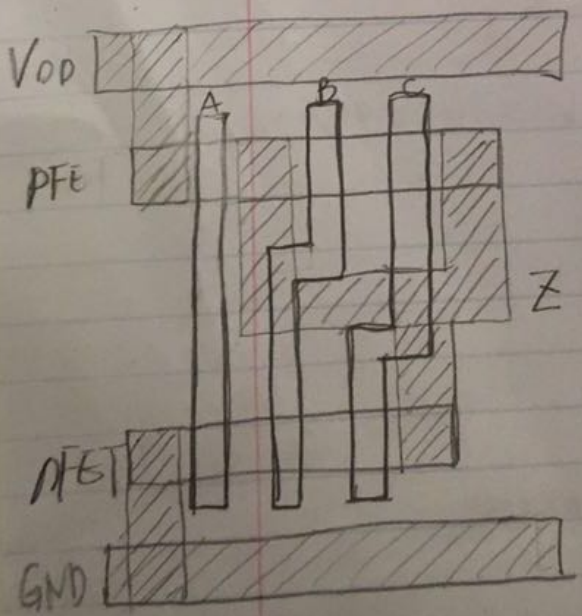
NMOS: $V_{Tn} = 0.39V$, $K_n' = 200\mu A/V^2$, $\gamma_n = 0$, $\lambda_n = 0$

PMOS: $V_{Tp} = 0.27V$, $K_p' = 60\mu A/V^2$, $\gamma_p = 0$, $\lambda_p = 0$





Final design



I curve inputs B and C, so output Z don't have to be outside the rectangle of VDD and GND.