Part 1

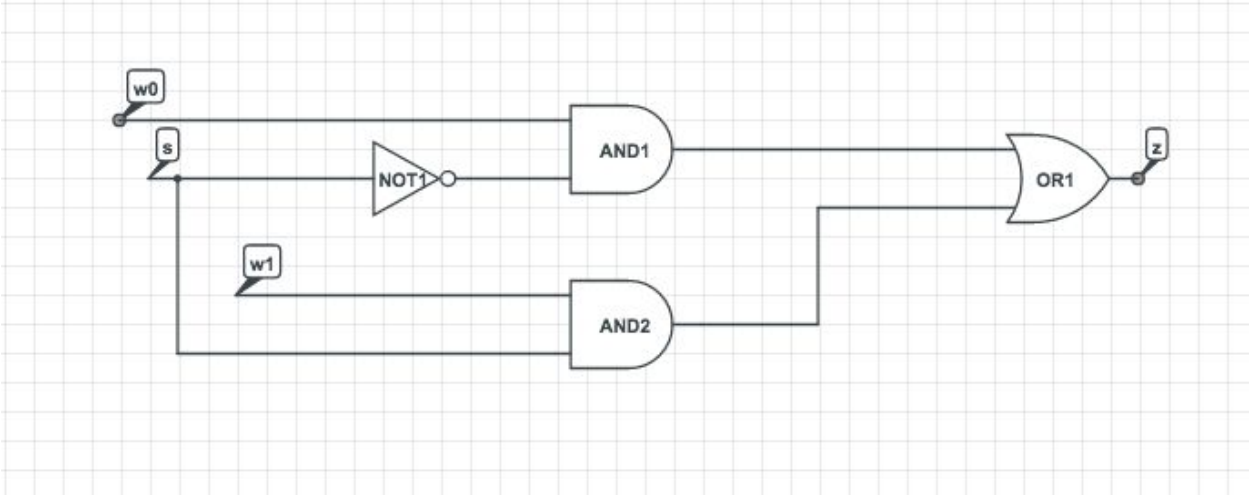
a)

w0	w1	s	z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

b)

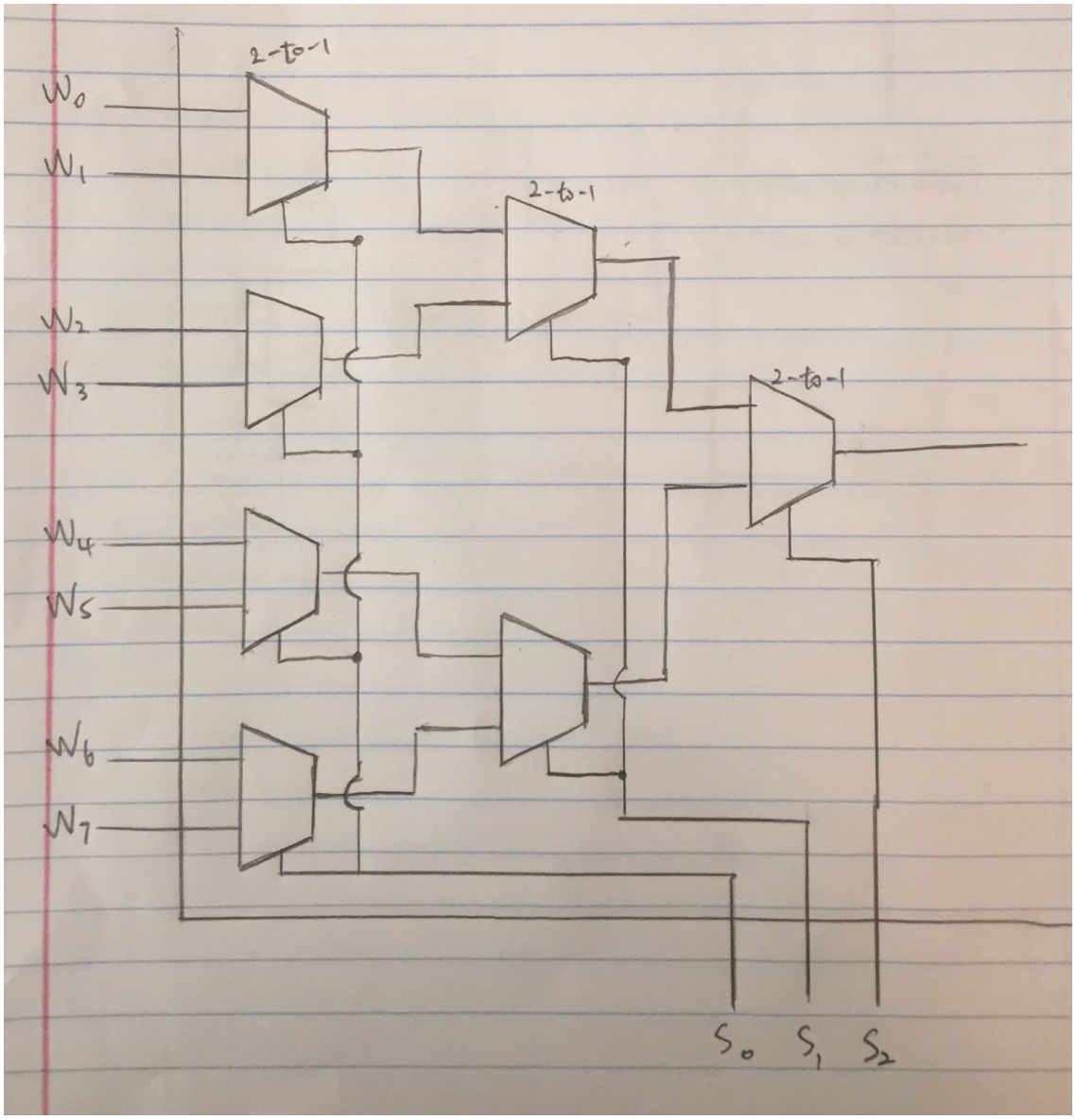
w0\w1s	00	01	11	10
0	0	0	1	0
1	1	0	1	1

Z = w1(s) + w0(s')



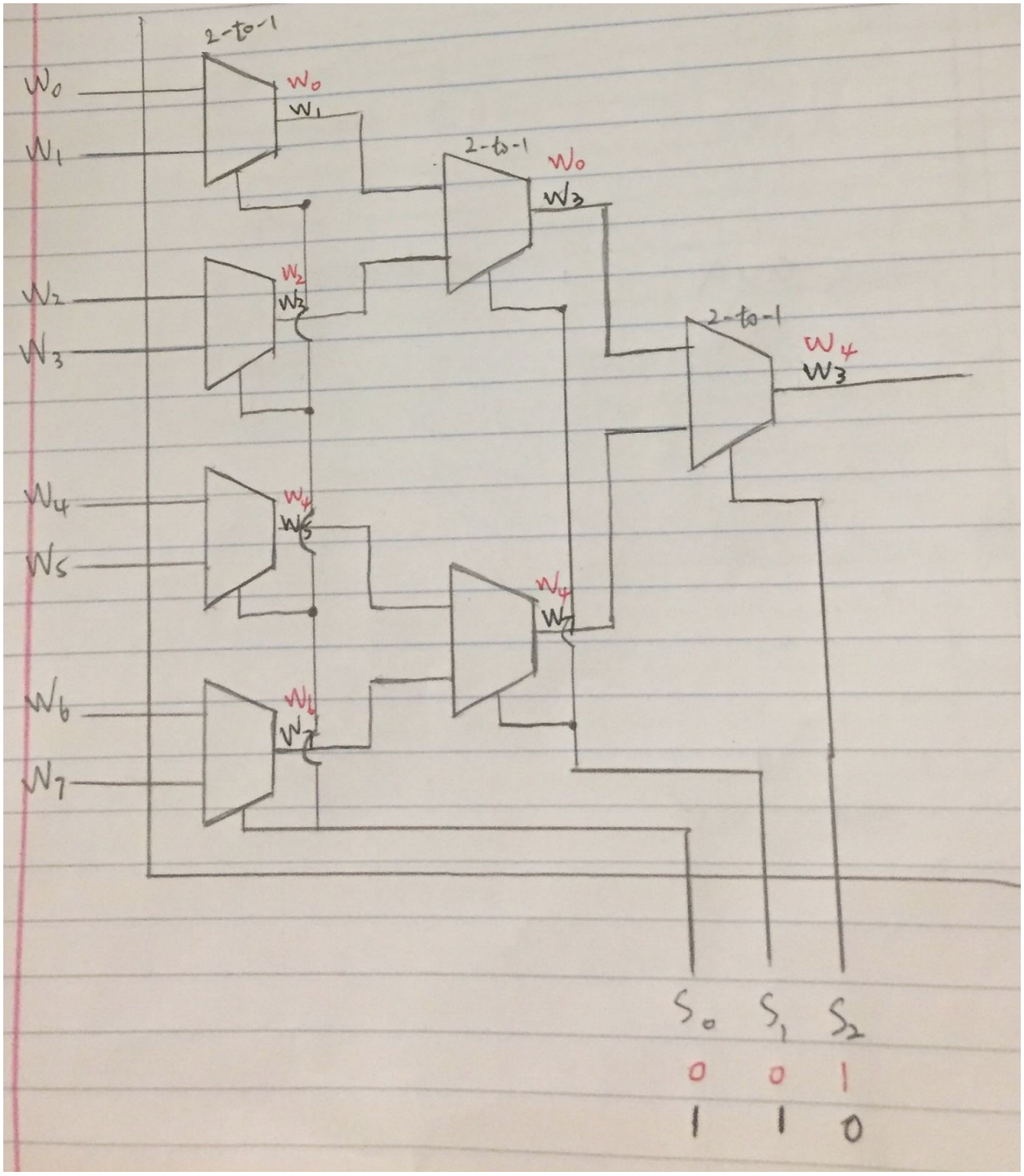
Part 2

We will need 7 2-1 mux in order to build a 8-1 mux



I have 8 data inputs w0, w1, w2, w3, w4, w5, w6, w7 and 3 select inputs s0, s1, s2 ordering from left to right.

As shown in the picture below, when s2s1s0 = 1 0 0, the output is w4; when s2s1s0 = 0 1 1, the output is w3.



Part 3

Truth Table:

A	B	C	F

0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1