SANTA CLARA UNIVERSITY	ELEN 153	Dr. S. Krishnan T.A. Sanad Kawar
Laboratory #6: Hierarchical Design Part 1– Four-Bit Adder		

I. PRE-LAB

Part A: Design

In this lab you are building a 4 bit ripple carry adder using a hierarchical methodology. You will start with

- a half adder made of logic gates (Look up some references from ELEN/COEN 21 or anywhere else).
- The next step would be to build a full adder using half adders.
- The final block would be to build a ripple carry adder using the full adders.

Submit schematics showing how you build the half adder, full adder and four-bit adder using the hierarchy above.

Use the following pin names:

- The input to the half adder are X and Y and the output are S and C
- The input to the full adder are Ai, Bi and Ci and the outputs are Si and Ci+1
- The inputs to the ripple carry adder are the two 4-bit words A3 A2 A1 A0, B3 B2 B1 B0 and Cin. The outputs of the ripple carry adder are the 4-bit output S3 S2 S1 S0 and Cout.

Part B: Testing

To test the correctness of the schematics entered, you need input stimulus. In the table below, work on unique 4-bit input vector pairs A and B to get the desired Carry and Sum outputs as described.

	A	B	C_4, S
Example	0000	1010	01010
1			10101
2			01010
3			10101
4			01010
5			10101
6			01010
7			10101
8			01010
9			10101
10			01010

Notes

1. Maximum value of a 4-bit vector is 1111. Do not exceed the maximum by using 5-bits.
2. Each unique combination of vector pairs A and B will be worth 10 points. Simply swapping A and B values will not count as two pairs. For example, the vector pair A=0000 B=1010, and A=1010 B=0000 are not unique, so is only worth 10 points.