NAME: _____

SANTA CLARA UNIVERSITY
Department of Computer Engineering

COEN 020 Final Exam Winter 2017

(Closed Book & Notes; Honor Code Applies)

NOTE: This final exam consists of two parts with a break in between. You will only be allowed to leave the room during the break. You may take your break as soon as you have completed Part 1. You will be given Part 2 of the exam when you return from your break.

Total Time Allowed: 3 hours

SCU's Academic Integrity Pledge

"I am committed to being a person of integrity. I pledge, as a member of the Santa Clara University community, to abide by and uphold the standards of academic integrity contained in the Student Conduct Code."

Signature:_____

	Points	Maximum
Part 1:		87
Part 2:		75
Total:		162

Overall: _____ %

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1. [5 pts] Convert 107_{10} to base 5.

$107_{10} = 4x5^2 + 1x5^1 + 2x5^0$ ➔ **412_5**

2. [5 pts] Convert 324_5 to base 10.

$3x5^2 + 2x5^1 + 4x5^0 = 75 + 10 + 4 =$ **89_{10}**

3. [5 pts] Convert 7.3_8 to base 4.

$7.3_8 = 111 \,.\, 011_2 = 01\ \ 11\ \ .\ \ 01\ 10_2 =$ **13.12_4**

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4. Perform the following signed number base conversions:

a. [5 pts] Convert -50_{10} to 8-bit 2's complement

$+50_{10} = 32 + 16 + 2 = 00110010$

$-50_{10} = 11001110_2$

Answer: 11001110_2

b. [5 pts] Convert -2.75_{10} to a 4.4 fixed-point real.

$+2.75_{10} = 0010.1100_2$

$-2.75_{10} = 1101.0100_2$

Answer: 1101.0100_2

c. [5 pts] Convert the 4.4 fixed-point real 1101.1100_2 to base 10

$1101.1100_2 = -0010.0100_2$

$= -2.25_{10}$

Answer: $-2.25_{10_{10}}$

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5. [5 pts] The closest representation of one-third as a Q2.6 fixed-point real is 00.010101_2. Suppose you multiply this by three. What is the decimal value of the result?

$2x = 00.101010_2$
$1x = 00.010101_2$

$3x = 00.111111_2 = 63/64 = 0.984375_{10}$

6. [6 pts] What value will be printed by each of the two following code segments?

```
int8_t prev, next ;

next = 0 ;
do {
    prev = next ;
    next = prev + 1 ;
   } while (next > prev) ;

printf("next = %d\n", next) ;
```

Answer: -128

```
uint8_t prev, next ;

next = 0 ;
do {
    prev = next ;
    next = prev + 1 ;
   } while (next > prev) ;

printf("next = %u\n", next) ;
```

Answer: 0

7. [5 pts] Assume you have two 16-bit numbers 4001_{16} and $FFFF_{16}$. Their 32-bit unsigned product is $4000BFFF_{16}$. Convert this 32-bit unsigned product into the corresponding 32-bit 2's-complement product. To do: (1) clearly show each step in your process, (2) give the final 32-bit result (in hex), and (3) give a short justification for each step in your conversion process.

FFFF is a negative value, so subtract 4001 from most-significant half:

```
 4000 BFFF
-4001
 FFFF BFFF
```

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8. Suppose you use reciprocal multiplication to divide by 5 on an 4-bit computer.

   a. [4 pts] What is the corresponding integer constant multiplier? $2^4/5 \rightarrow 3$

   b. [4 pts] What integer quotient would you get when the dividend is 20?

   $3x20 = 60_{10} = 32+16+8+4 = 00111100_2 \rightarrow 0011_2 = \mathbf{3_{10}}$

9. [10 pts] Fill-in all the carry, borrow, sum and difference bits in the following operations and indicate if overflow occurs:

1	1	1	0	0
	1	0	1	0
+	0	1	1	0
	0	0	0	0

Unsigned overflow? Yes

2's complement overflow? No

0	1	0	0	0
	1	0	1	0
–	0	1	1	0
	0	1	0	0

Unsigned overflow? No

2's complement overflow? Yes

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10. [8 pts] For each data type listed below, indicate the corresponding variation of the LDR instruction by placing an "X" in the appropriate column:

Data Type	LDR	LDRB	LDRSB	LDRH	LDRSH	LDRD
`int8_t *`	X					
`int16_t`					X	
`int32_t`	X					
`int64_t`						X
`uint8_t`		X				
`uint16_t *`	X					
`uint32_t`	X					
`uint64_t *`	X					

11. [3 pts] For each instruction listed below, indicate by how much it multiplies R0:

Instruction	Multiplier
`ADD R0,R0,R0,LSL 3`	9
`SUB R0,R0,R0,LSL 4`	-15
`RSB R0,R0,R0,LSL 5`	31

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12. [7 pts] For each addressing mode listed below, indicate the corresponding C expression by placing an "X" in the appropriate column. Assume the operand size is specified by the C identifier.

Addressing Mode	*p64	*(p16+1)	a32[k16]	None
[R1]	x			
[R1,1]				X
[R1,2]		X		
[R1,4]				X
[R1,R2,LSL 1]				X
[R1,R2,LSL 2]			X	
[R1,R2,LSL 4]				X

13. [5 pts] Without using SDIV or UDIV instruction, give a short sequence of assembly language instructions that will correctly divide the 2's complement integer held in register R0 by the constant 16 and leave the result in the same register.

```
MOV  R1,15              // get 16-1
AND  R1,R1,R0,ASR 31    // R1 = (R0 < 0) ? 15 : 0
ADD  R0,R0,R1           // R0 += (R0 < 0) ? 15 : 0
ASR  R0,R0,4            // R0 = R0 >> 4
```