

# Assignment 1 - 4:1 Multiplexer

**COEN 122L - Fall 2018**

**By:** Ryan Khodi (rkhodi@scu.edu)

**TA Office Hours:** By appointment.

**Professor:** Dr. Weijia Shang (wshang@scu.edu)

## Description

A multiplexer's job is to receive  $n$  inputs and pass one through based on the value of the select input. In this case, our 4 to 1 multiplexer will receive 4 one-bit inputs, and assign the output to the input that corresponds to the value of the select. For example, if the two-bit select reads 2 (10), then `out_data = in_data_2` (refer to figure 1).

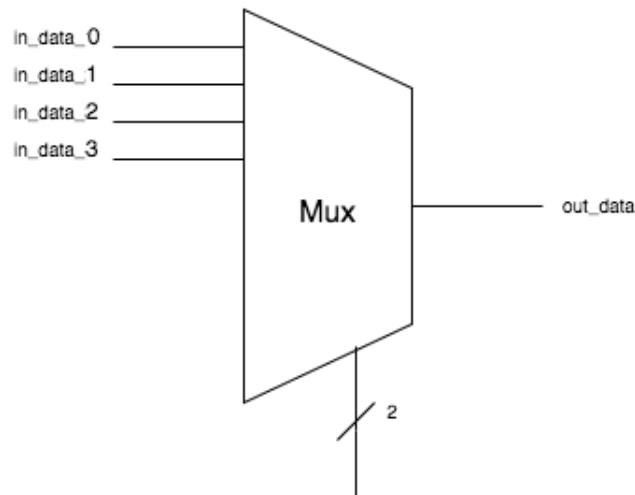


Figure 1: 4:1 Multiplexer

## Assignment

In this lab, you will create a 4:1 multiplexer using Verilog. This component should have 4 one-bit inputs, a two-bit select, and a one-bit output. The bulk of the multiplexer code can be done using various if-else statements. Based on the values of the select, assign the output to the appropriate input.

## Deliverables

To receive full credit, you will need to demo your working code. In addition, you must submit your source code (commented), your test-bench code (commented), and a screenshot of your waveform. To submit online, make sure everything is in a zipped folder (name the folder `firstname_lastname.zip`) and turn it into Camino. Please copy your code into individual .txt files and include those in the folder.