SANTA CLARA UNIVERSITY
Electrical Engineering Department

ELEN 21/COEN 21 Introduction to Logic Design – Spring 2014

Midterm Exam 2 solution
Total time: 60 minutes Total points: 30

Good luck!

Name: _____

1. [5 points] (a) Convert the decimal number -25 into signed 12-bit numbers in the following representations:

- Sign and magnitude

  100000011001

- 1's complement

  111111100110

- 2's complement

  111111100111

(b) Convert the number -25 into hexadecimal and octal.

Hexadecimal: FE7
Octal: 7747

(b) [5 points] Given two numbers X = 7 and Y = 19, perform subtraction X – Y using 2's complement arithmetic when the numbers are represented in 5 bits. Determine if overflow occurs.

7 = 00111
19 = 10011

If we take the 2's complement of 19 to perform the subtraction, we get the value 01101, which is a positive number because the most significant bit of the number is 0. This does not represent -19 correctly, which is the value 101101. Therefore, we need at least 16 bits to represent the number. Overflow occurs when 5 bits are used.

2. [5 points] Design a binary multiplier to multiply a 4-bit number with a 3-bit number.

$A_3\ A_2\ A_1\ A_0$

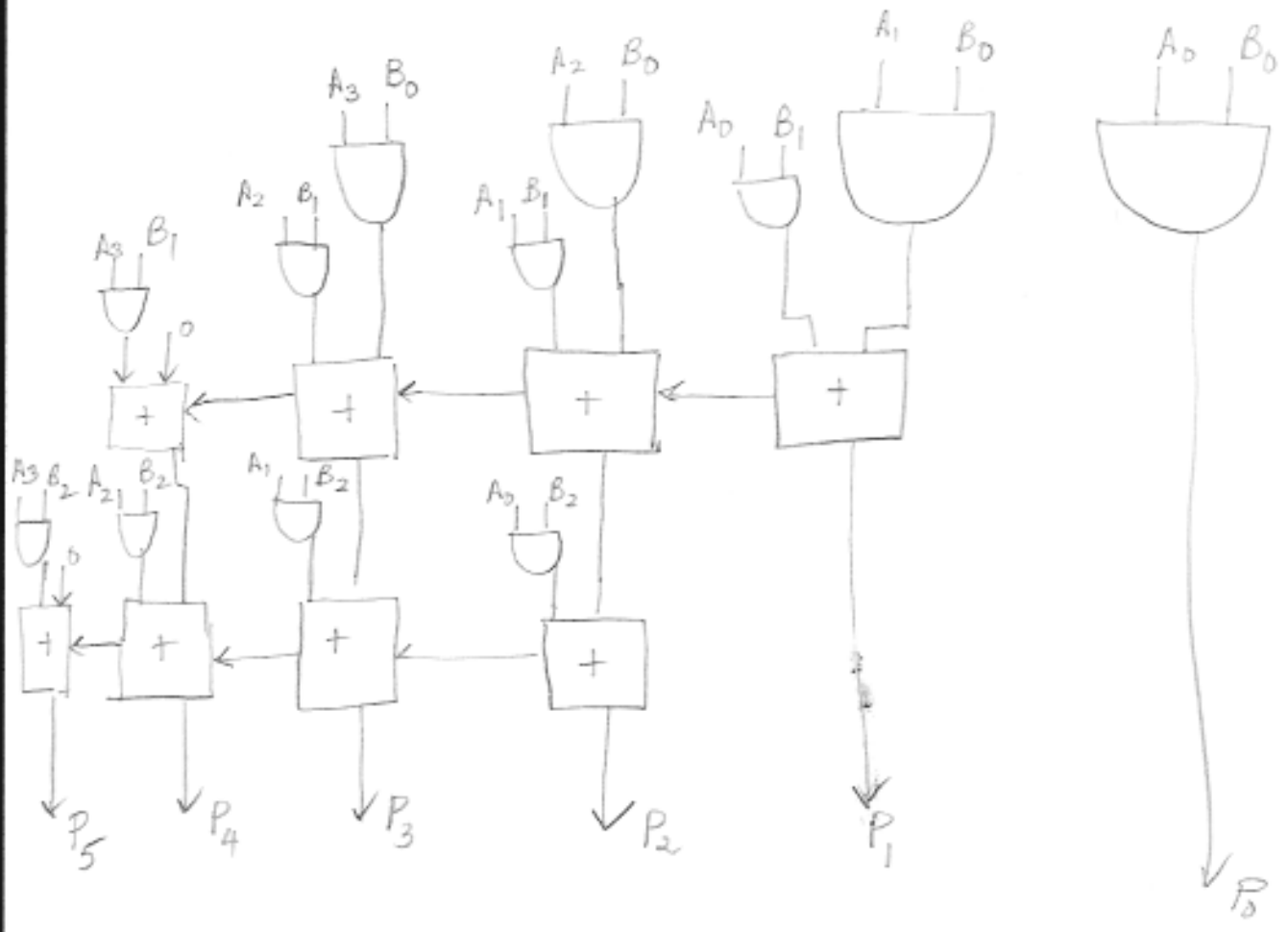
$B_2\ B_1\ B_0$

$A_3B_0 \quad A_2B_0 \quad A_1B_0 \quad A_0B_0$

$A_3B_1 \quad A_2B_1 \quad A_1B_1 \quad A_0B_1$

$A_3B_2 \quad A_2B_2 \quad A_1B_2 \quad A_0B_2$

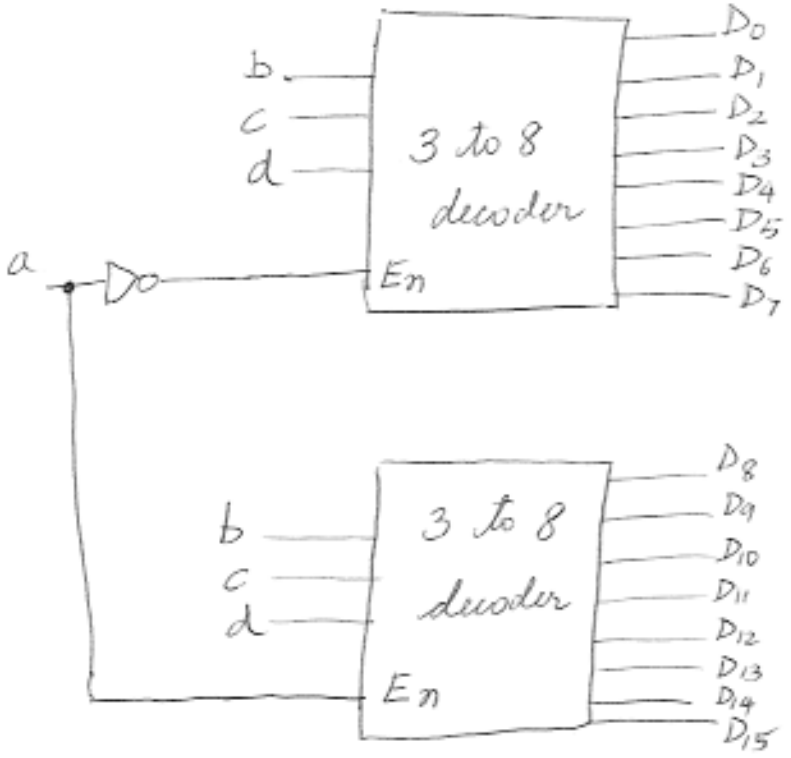
$P_5 \quad P_4 \quad P_3 \quad P_2 \quad P_1 \quad P_0$



3. Give the truth table for a 4-to-16 decoder. Design the 4-to-16 decoder using 3-to-8 decoders and 2-to-4-decoders.

Truth table

a	b	c	d	D_0	D_1	D_2	D_3	...	D_{14}	D_{15}
0	0	0	0	1	0	0	0	...	0	0
0	0	0	1	0	1	0	0	...	0	0
0	0	1	0	0	0	1	0	...	0	0
⋮						⋮				
1	1	1	1	0	0	0	0	...	0	1



4. [5 points] Design a combinational circuit with three inputs x, y, and z, and three outputs A, B, and C. When the binary input is 0, 1, 2, or 3, the binary output is one greater than the input. When the binary input is 4, 5, 6, or 7, the binary output is one less than the input.

Step 1: Design the truth table from the problem description.

x	y	z	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	1	0	0
1	0	0	0	1	1
1	0	1	1	0	0
1	1	0	1	0	1
1	1	1	1	1	0

Step 2: Find the logic equations using Kmaps.

A

x \ yz	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$A = xy + xz + yz$

B

x \ yz	00	01	11	10
0	0	1	0	1
1	1	0	1	0

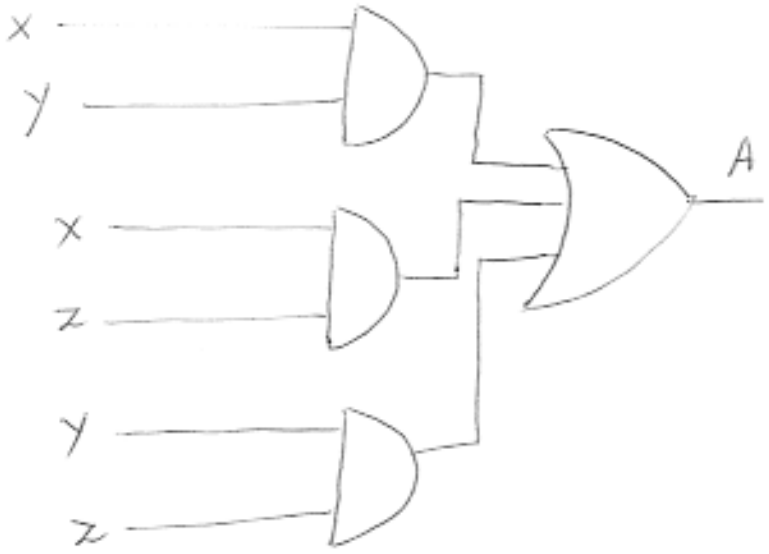
$B = x \oplus y \oplus z$

C

x \ yz	00	01	11	10
0	1	0	0	1
1	1	0	0	1

$C = z'$

Step 3: Draw the logic circuit:



5. [5 points] Design a SR latch with NOR gates and give its truth table. Draw the state diagram.

See slides 7 and 8 of lectures 13-14