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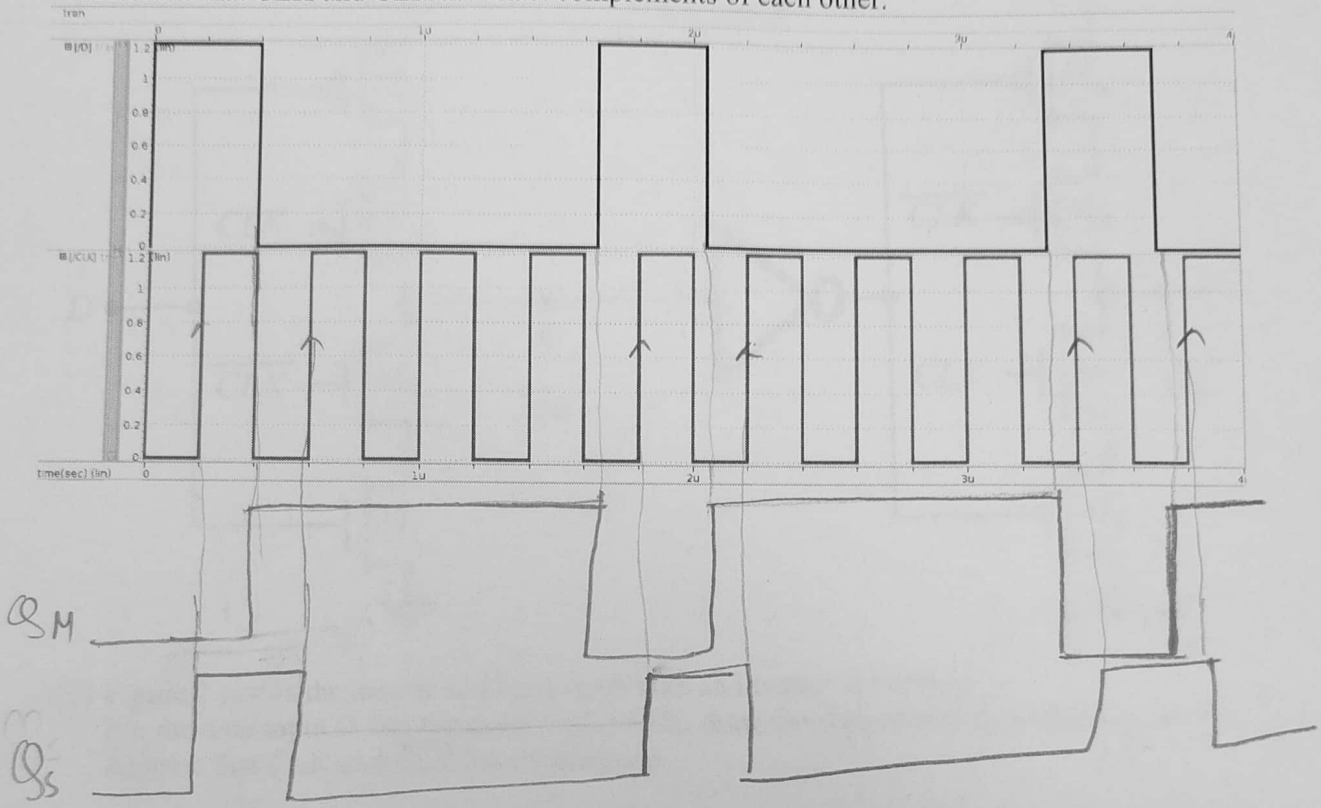
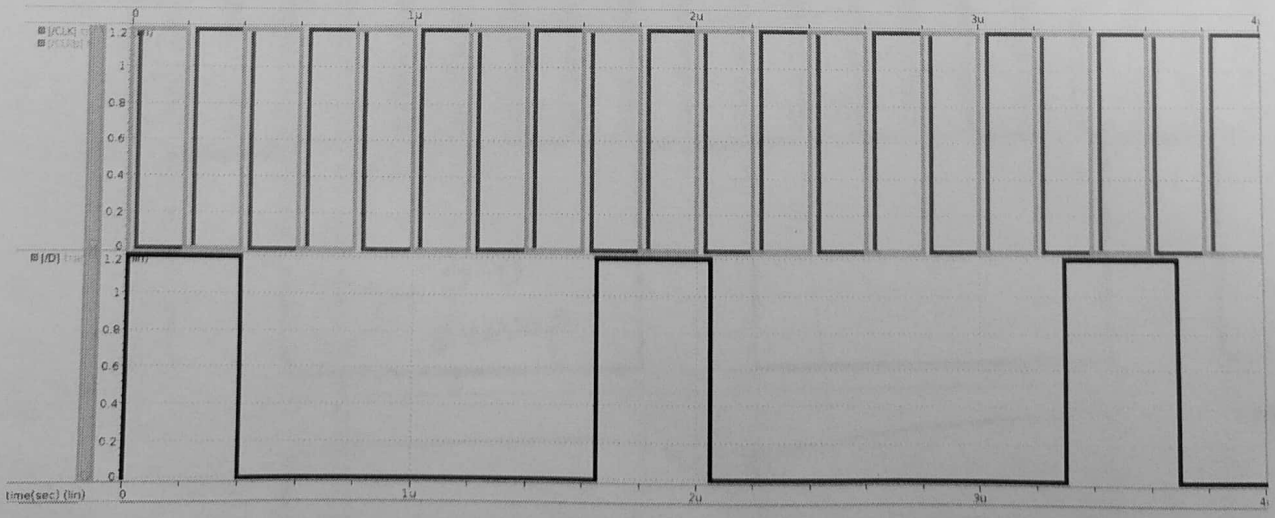
Complete the timing diagrams below for the schematic.

(a) For the data input D and the clock signal CLK, draw the corresponding outputs Q_M and Q_S. Assume that CLK and $\overline{CLK}$ are exact complements of each other.



(b) For the data input D and the clock signal CLK, draw the corresponding outputs Q_M and Q_S. This time assume that CLK and $\overline{CLK}$ have an overlap. CLKB is the same as $\overline{CLK}$ in Figure 1.



same as (a). C²MOS is immune to clock overlaps.

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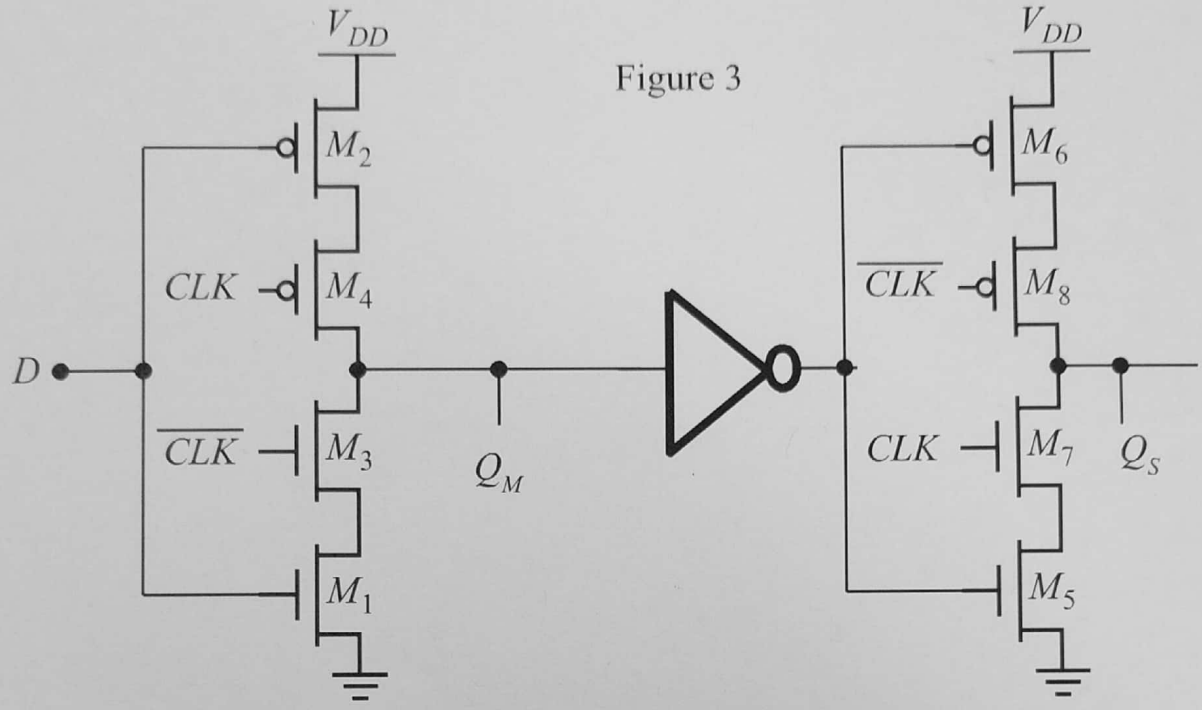
Figure 3



(c) Figure 3 shows the master and slave latch with an inverter in between.
For the data input D and the clock signal CLK, draw the corresponding outputs Q_M and Q_S.
Assume that CLK and $\overline{CLK}$ have an overlap.