SANTA CLARA UNIVERSITY	ELEN 153 Fall 2017	Dr. S. Krishnan
Pre-Lab #5: Layout of Three Input NAND gate		

For the MOS devices in 90nm technology use the parameters listed below.
NMOS: V_{tn0}= 0.39V, k_n' = 200μA/V^2, γ_n= 0, λ_n=0
PMOS: V_{tp0}= 0.27V, k_p' = 60μA/V^2, γ_p= 0, λ_p=0

For a three input NAND gate, draw a stick diagram clearly showing how the layout of the gate can be done. Make sure you indicate the layers clearly.
Show what steps you have taken to make an efficient layout with respect to area, power and speed for the gate. Explain these steps.