ELEN 21 Lab Three: Two Level Circuit Design

ELEN 21L Logic Design: T 2:15pm
Group 3
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I. Objectives:

The primary objective of this experiment was to design and implement a circuit based on a real world scenario application. The equivalent circuit designed was required to meet the specifications for a highway entrance ramp in order to efficiently control the flow of traffic. Through this analysis, a problem statement was translated to algebraic representations and a functional circuit. Furthermore, the objectives of this lab were to successfully use K-maps to find the minimum logic solutions and finally to implement and test the circuit on an Altera FPGA board..

II. Introduction:

The goal of this experiment is to design a highway entrance ramp in order to meter the flow of traffic amongst three lanes. The three different lanes include a carpool lane, left lane, and right lane with their respective sensors CS, LS, and RS. Additionally a round robin signal, RR, is utilized to determine priorities between the left and right lanes. The sensors in each lane are used to indicate when a car is present or waiting and each lane has its own light. A logic of 0 indicates a red light for stop and a logic of 1 indicates a green light for go. The carpool lane is given priority over the other two lanes to go and the round robin signal is used to alternate between the left and right lanes when there is no car in the carpool lane. There are three controller outputs in this circuit including the carpool light (CS), left lane light (LL), and right lane light (RL). There are several specifications to consider for in this circuit which are summarized in the truth table shown in Table 1.

Table 1: Truth Table Demonstrating the Design Specifications

Inputs				Outputs		
CS	LS	RS	RR	CL	LL	RL
0	0	0	0	0	0	1
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0

1	0	1	1	1	0	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

III. Procedure:

In order to develop the desired circuit, the team referred to the design specifications, the problem statement, and Table 1 to determine how the system is supposed to respond based on various inputs. The truth table was utilized in order to implement a schematic in Quartus II for analysis, demonstrated in Figure 1. Upon completion of the circuit, the program could be used in order to simulate the functionality of the circuit. Successful simulation of the circuit in the program leads to the ability to upload and implement the circuit onto the Altera FPGA board. The circuit on the board was then used to insure that the resulting outputs correlated with the various inputs. Finally, after successful implementation of this circuit, a new output ZZ was added to the circuit to be a 1 when no cars are waiting in any of the lanes in order to better monitor and manage traffic.

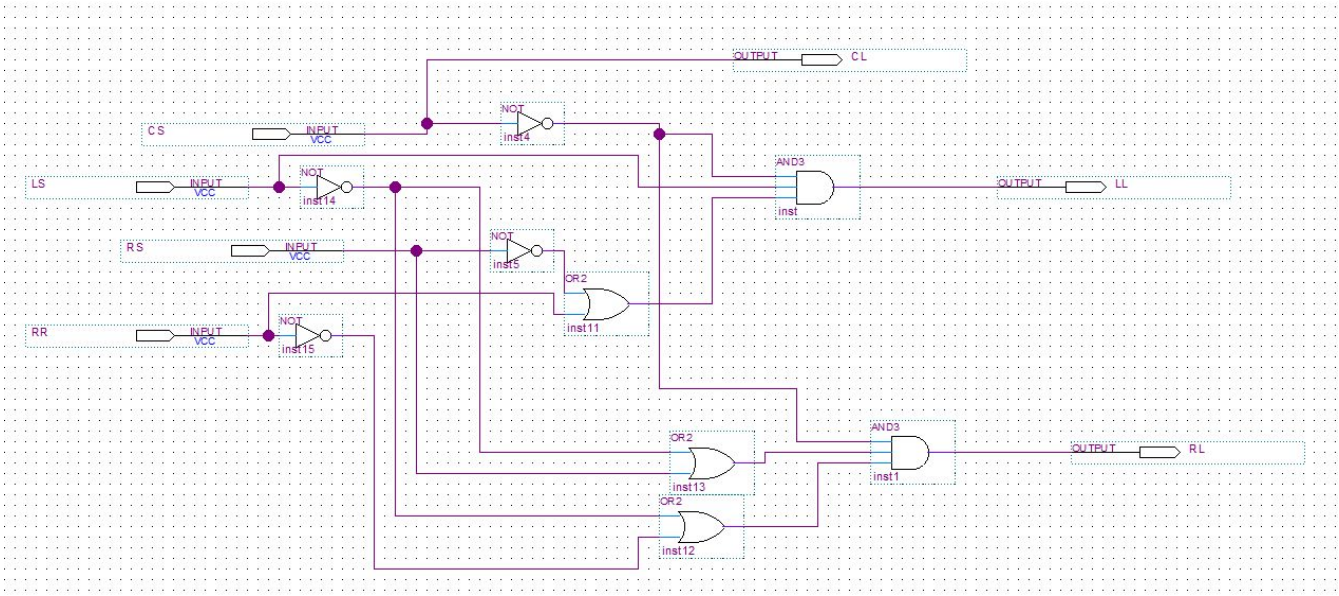

Figure 1. The schematic constructed in Quartus II to meet the design specifications.

IV. Results

The Quartus II program in accordance with the Altera FPGA board were used to test and implement the circuit. After successful compilation in Quartus II, the circuit was compiled and a simulation waveform was created to compare to Table 1; the result is shown in Figure 2.

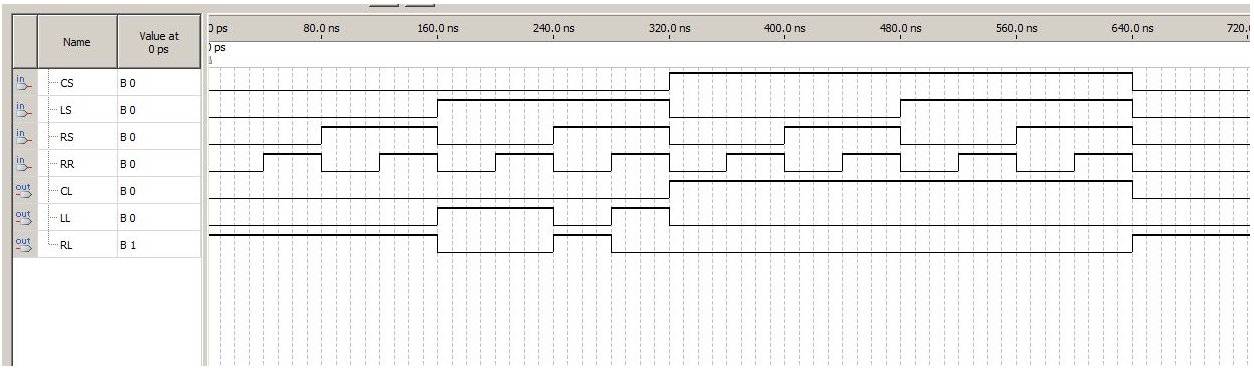

Figure 2. The simulation waveform created in Quartus II.

Figure 2 demonstrates that the simulation worked as desired for the circuit. The circuit was then compiled and downloaded to the FPGA board. After testing the circuit for all possible inputs and cross referencing with the truth table, it was determined that the circuit worked as desired and met the design specifications.

After successfully implementing the previous desired circuit, the new output ZZ was added to the circuit. After the modification, the circuit in Quartus II looks like what is shown in Figure 3.

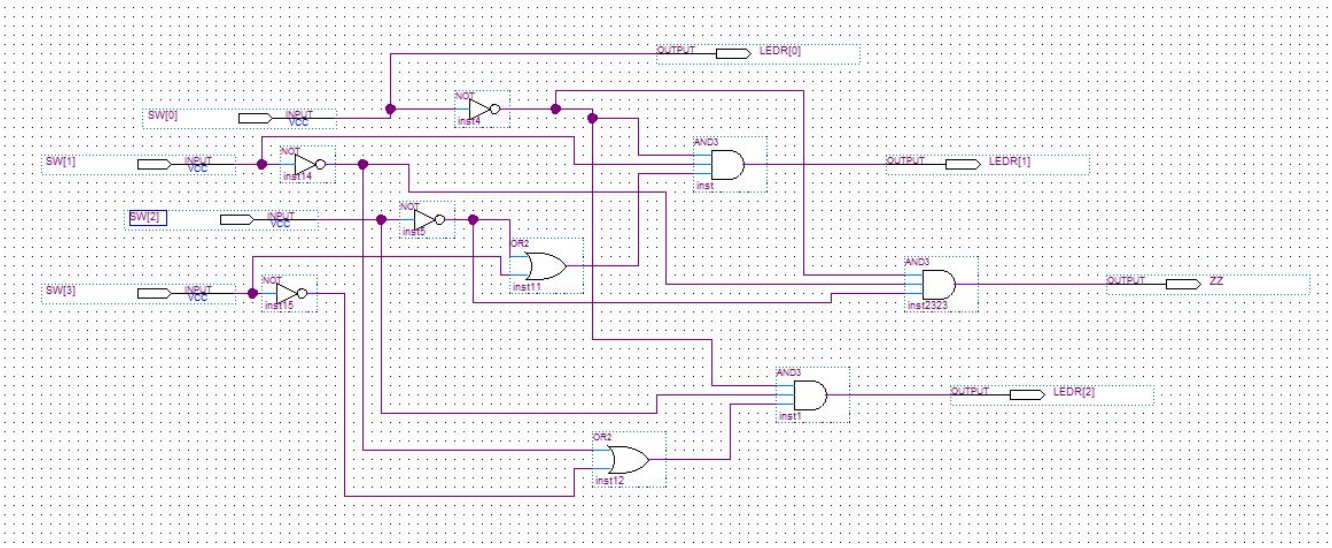

Figure 3. Schematic with an extra output ZZ

After modifying the circuit, adding an output, we compile the program and create a waveform according to the circuit in Figure 3. The result of the waveform matches the given condition that ZZ will be 1 when there are no cars waiting in any of the lanes.

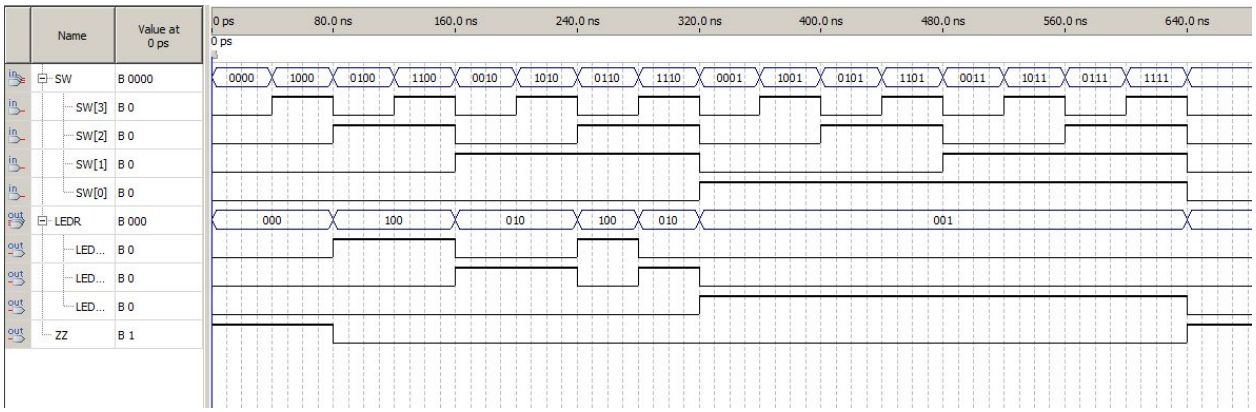

Figure 4. Waveform of the circuit in Figure 3

FPGA Implementation

After testing the circuit without the extra output ZZ, we assign pins for the inputs and outputs as shown in Figure 4. The circuit was then compiled and downloaded onto the FPGA board. After testing all possible input conditions, it was determined that the circuit met all the required design specifications in accordance with the truth table.

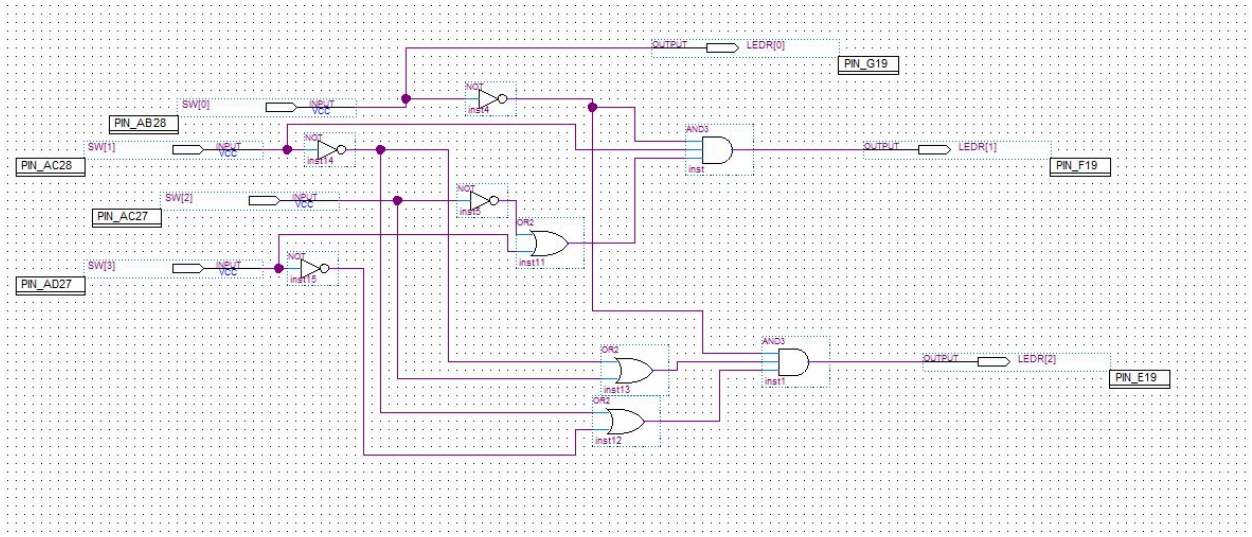

Figure 5. Schematic with pin assigned

V. Lessons Learned from Mistakes

1. After we built a basic circuit according to the circuit that we got from the K-map, we found that we can have a NOT gate right besides the input so we will only need 4 NOT gate instead of needing a NOT gate constantly. The modification need a lot of space, and when we were moving the wire and the input around, there may be some extra wire connecting the gate with nowhere, which could cause error.
2. Sometimes the device is not the one that we want it to be, which is the sixth one counting from the bottom.
3. Sometimes we will have unwanted nodes.

VI. Final question:

Describe how you would modify your circuit to include a fifth input TM, a timer that is turned on at intervals controlled by the traffic density. When TM is "1", the circuit operates exactly as specified in the problem statement. When TM is "0", all output lights are red.

So after we have the new input TM, we will have five input, where TM is the most significant one. When TM is "1", the circuit operates as in the problem statement, and the truth table of the inputs and outputs will look like Figure 1. When TM is "0", all output lights are red, which means all outputs will have 0, which will look like Figure 2.

TM	CS	LS	RS	RR	CL	LL	RL
1	0	0	0	0	0	0	1
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	1
1	0	0	1	1	0	0	1
1	0	1	0	0	0	1	0
1	0	1	0	1	0	1	0
1	0	1	1	0	0	0	1
1	0	1	1	1	0	1	0
1	1	0	0	0	1	0	0
1	1	0	0	1	1	0	0
1	1	0	1	0	1	0	0
1	1	0	1	1	1	0	0
1	1	1	0	0	1	0	0
1	1	1	0	1	1	0	0
1	1	1	1	0	1	0	0
1	1	1	1	1	1	0	0

Figure 6. Truth table when TM is 1

TM	CS	LS	RS	RR	CL	LL	RL
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0
0	0	0	1	0	0	0	0
0	0	0	1	1	0	0	0
0	0	1	0	0	0	0	0
0	0	1	0	1	0	0	0
0	0	1	1	0	0	0	0
0	0	1	1	1	0	0	0
0	1	0	0	0	0	0	0
0	1	0	0	1	0	0	0
0	1	0	1	0	0	0	0
0	1	0	1	1	0	0	0
0	1	1	0	0	0	0	0
0	1	1	0	1	0	0	0
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0

Figure 7. Truth table when TM is 0

The new circuit with an additional input TM will be the following:

f(CL) = TMCS

f(LL) = TM((CS')LS(RS') + (CS')LS(RR))

f(RL) = TM((CS')(LS') + (CS')(RS)(RR'))

We will need an AND2 gate connecting TM and each of the former outputs so we can have new circuits for them.

IV. Conclusion

The real world problem statement was successfully translated into an algebraic expression and then converted into a functioning circuit. Further understanding was developed in how to use Quartus II and the FPGA board to design a complicated schematic and test it with the waveform editor. Additionally, the

team was able to use K-maps to simplify the functions. Overall, all of the necessary objections were successfully implemented in order to design a functioning and efficient highway entrance ramp control.

V. **Reference lists:**

- Dr. Sally Wood, Dr. Samiha Mourad, Dr. Radhika Grover. *Laboratory #3: Two Level Circuit Design* . Spring 2017. Print
- ftp.altera.com/up/pub/Altera_Material/12.1/Tutorials/Schematic/Quartus_II_Introduction.pdf
- ftp.altera.com/up/pub/Altera_Material/13.1/Tutorials/Verilog/Quartus_II_Simulation.pdf
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