Yutong Li

ELEN 153L
Wedn 2:15 - 5:00 pm
2017/9/27

Lab 1: Introduction to Synopsys

1. Objective

- To learn how to setup and use Synopsys Custom Compiler to create and simulate schematics.
- To simulate the I-V characteristics of an NMOS transistor.
- To construct and simulate a simple voltage divider network and an RC network

2. Procedure

Part A. Synopsys Tutorial and NMOS I-V Curves

From the NMOS practice, we learn how to create a simple file in detail.

1. I created a folder “Tutorial” to hold the file.
2. I created a cell “NMOS” and a view “schematic”.
3. Inside the schematic, I chose specific instances and change some of the attributes due to the introduction.
4. After consoling, I opened SAE and set up models.
5. After that, I selected source for sweep variable and selected output.
6. By using parametric analysis, I was able to get multiple curves in the waveform due to the number of total points.

Part B. Voltage Divider

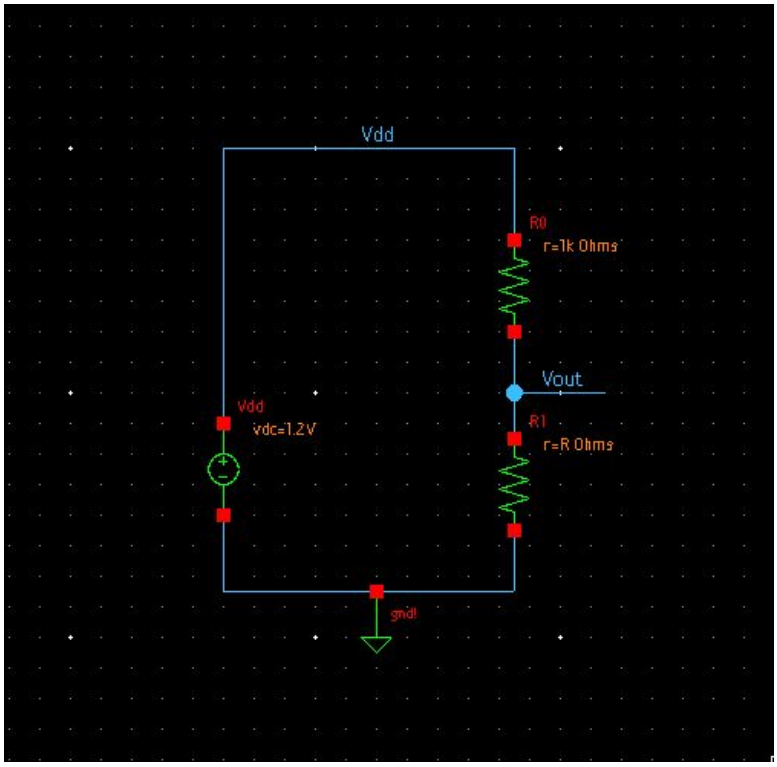

Figure 1. Schematic of Voltage Divider

Source sweep:

In order to sweep source, we need to set source, vdd as sweep variable, and set up is shown in Figure 2.

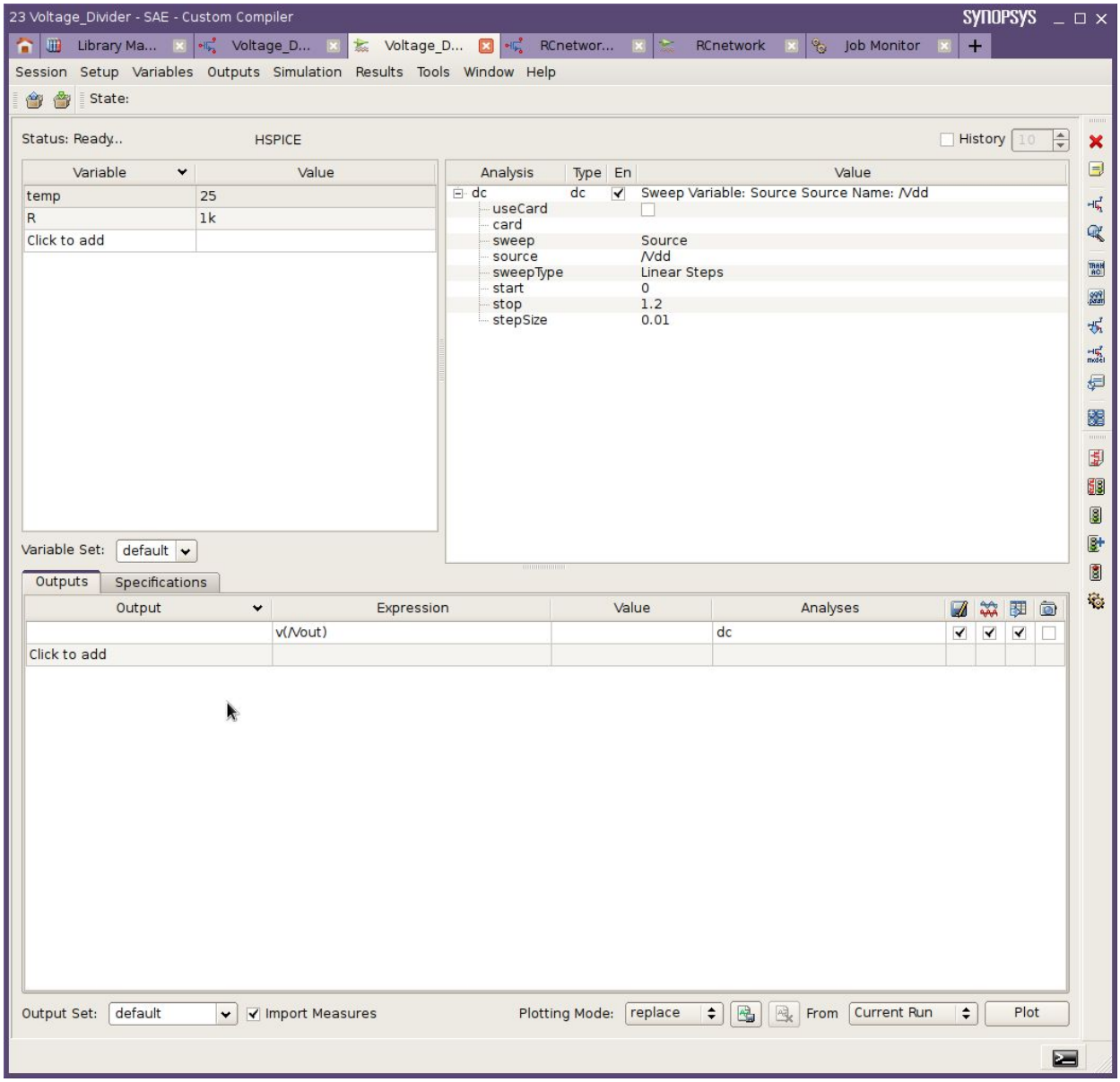

Figure 2. SAE of Source sweep

The simulation of source sweep is shown in Figure 3.

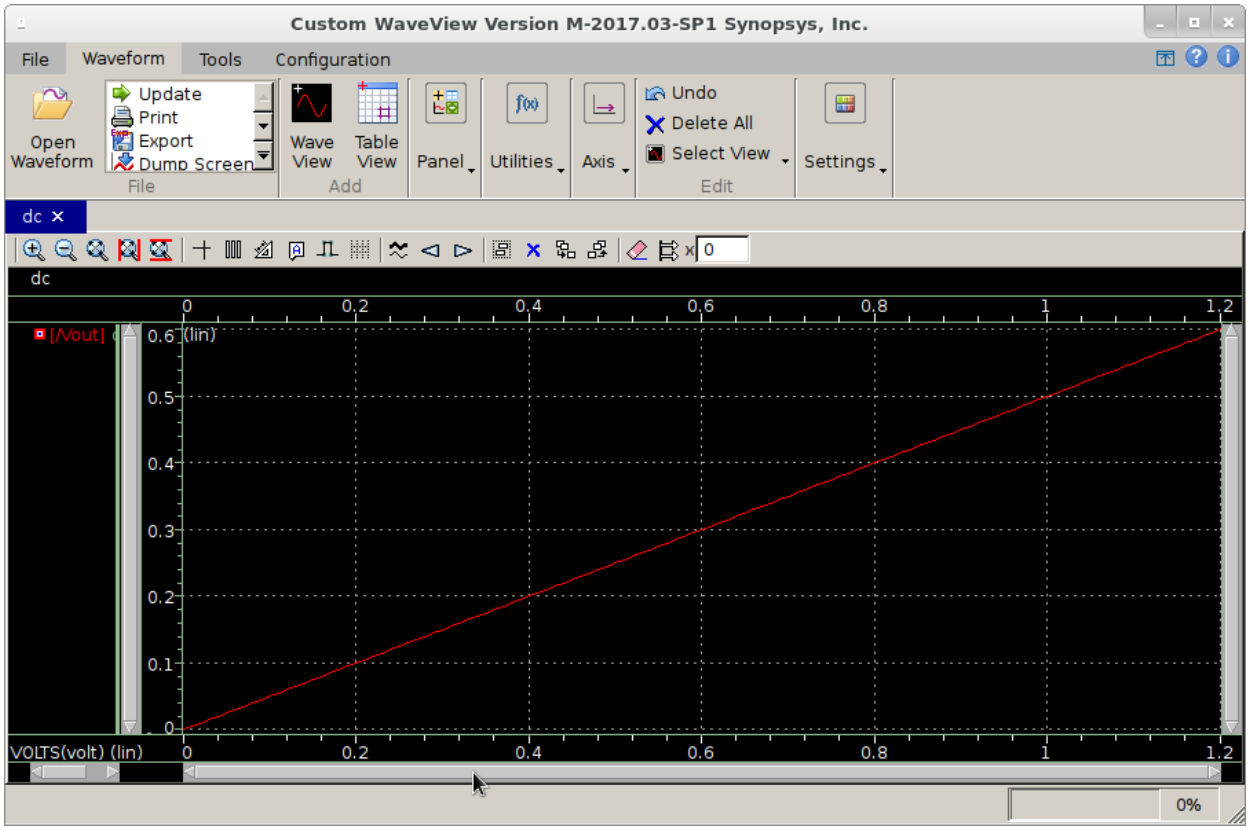

Figure 3. Waveform of source sweep

We can see that the relationship between Vdd and Vout is linear, because the values of R0 and R1 are fix, just like what the equation shows:

$$\text{Vout} = \text{Vdd} * \frac{R1}{R1 + R0} = \text{Vdd} * \frac{1k}{1k + 1k} = 0.5\text{Vdd}$$

Question: What is Vout when Vdd=0.6V? 1.2V?

From Figure 3, because the line is on grid, we can tell that Vout = 0.3V when Vdd = 0.6V and Vout = 0.6V when Vdd = 1.2V.

Also, from the equation we can tell that Vout is half of Vdd.

Resistance sweep:

In order to sweep resistance, we need to set resistance of R1, R as sweep variable, and set up is shown in Figure 4.

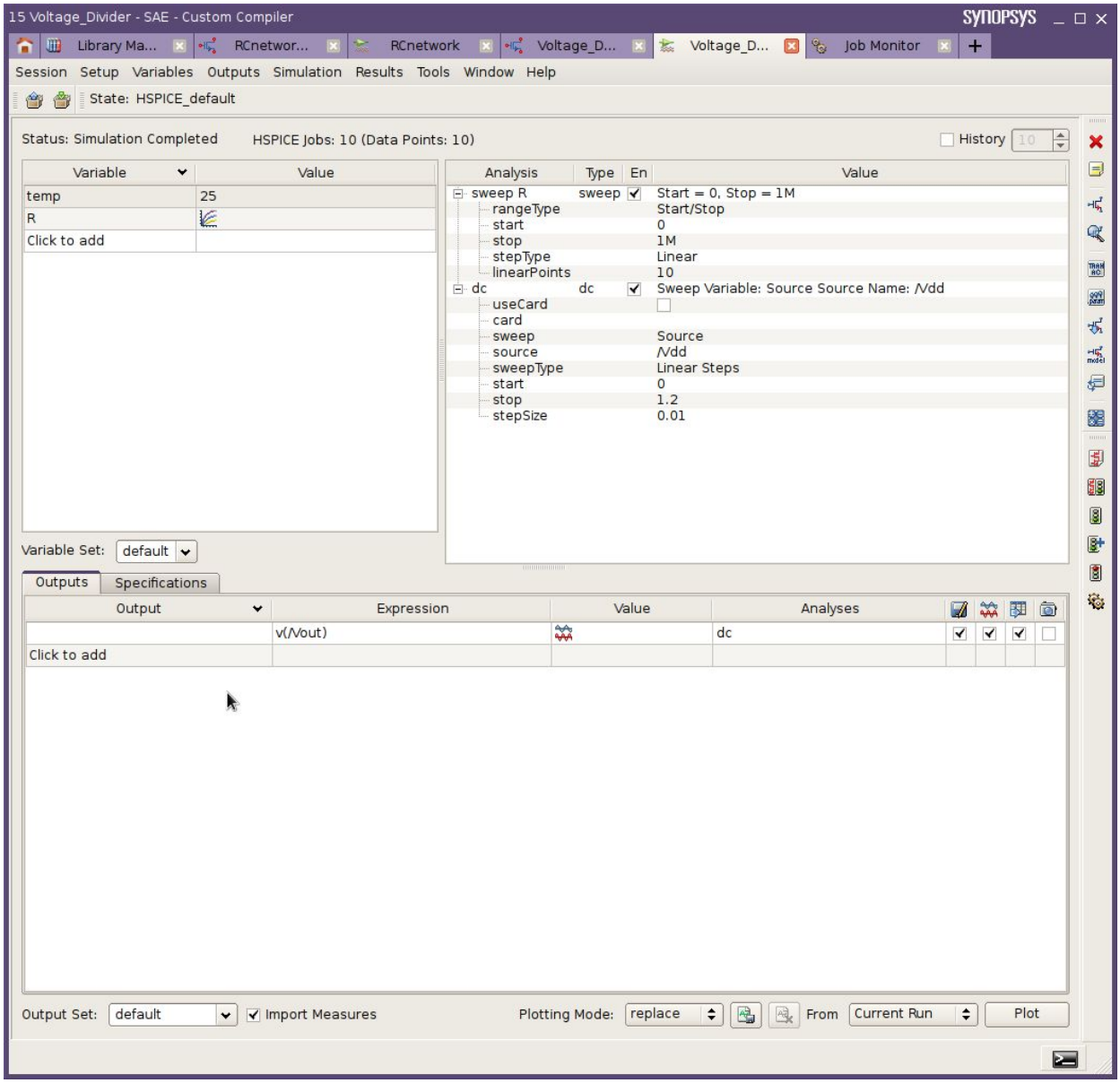

Figure 4. SAE of resistance sweep

The reason that Figure 4 is different from the picture in the lab introduction is that I can only get a single curve following the instruction. Following Figure 4, I was able to obtain the desired waveform.

The simulation of resistance sweep is shown in Figure 5.

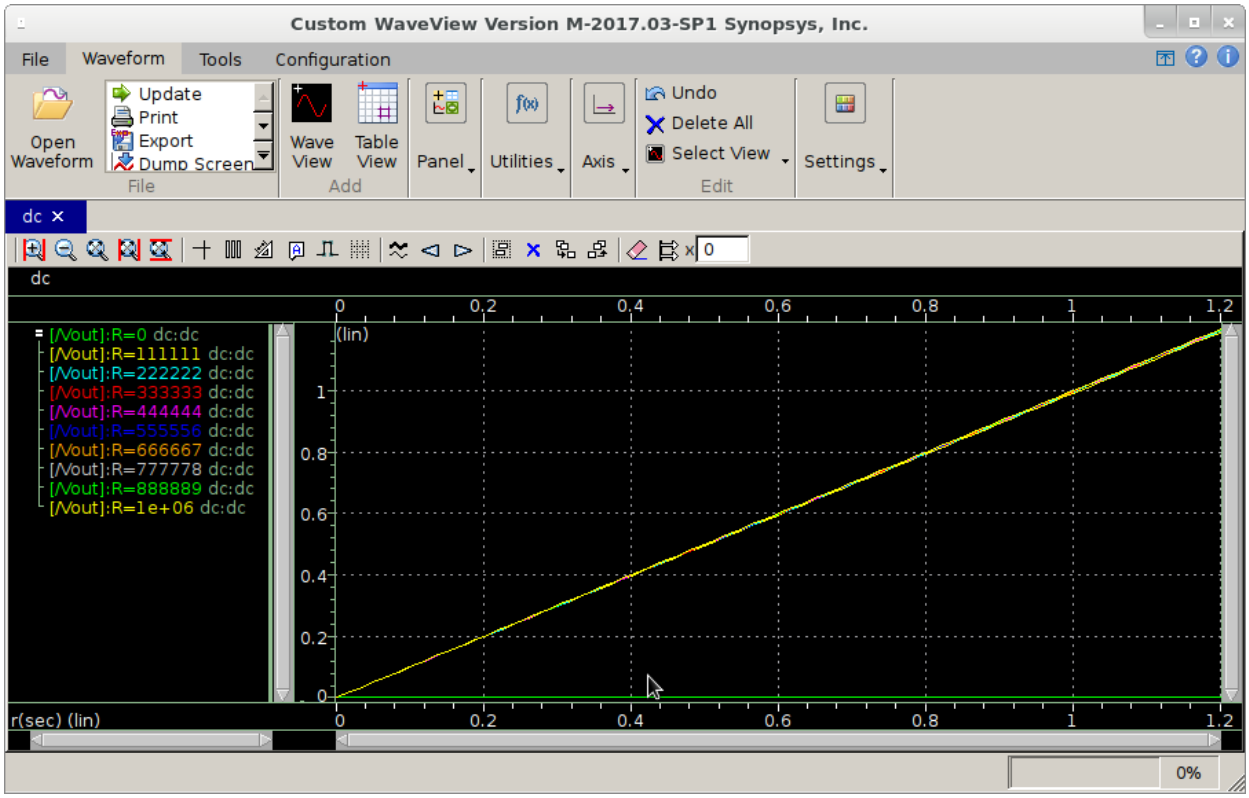

Figure 5. Waveform of resistance sweep

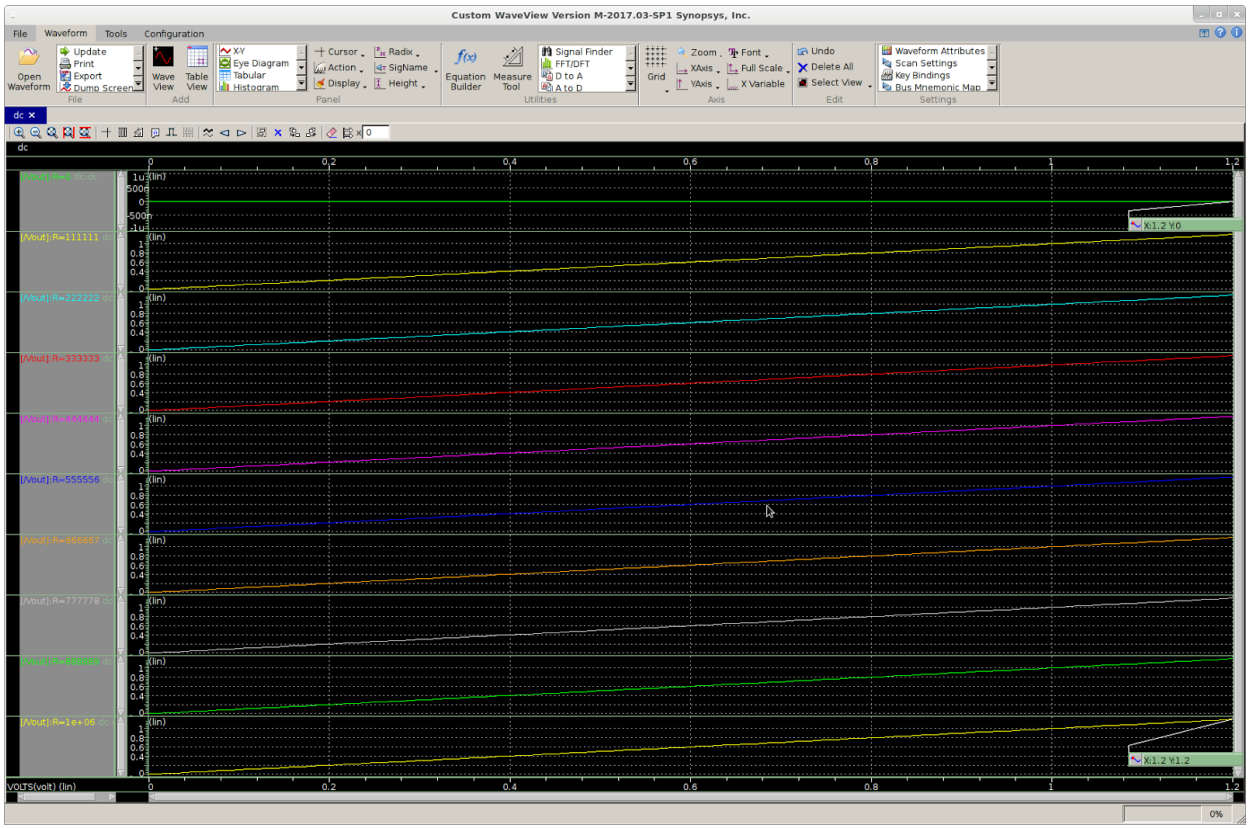

Figure 6. Ungrouped waveform

Question: What is Vout when R=0? What is it when R=1MΩ?

When R = 0, Vout = 0.

When R = 1MΩ, Vout = 1.2V.

We can both observe the value of Vout in the waveform and calculate it with the equation after Figure 3.

Part C. Simple RC Network

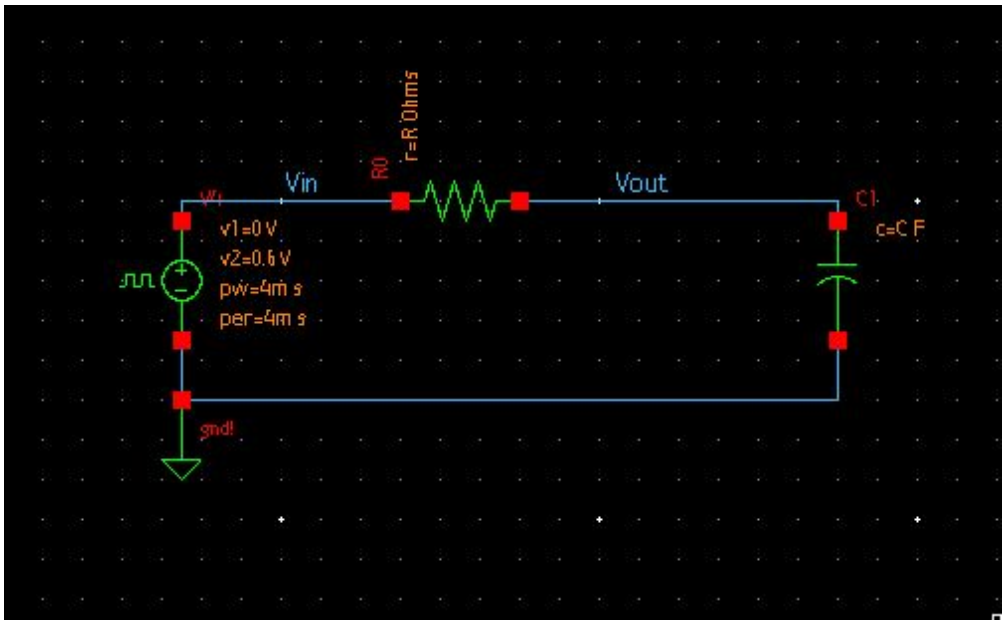

Figure 7. Schematic of RC Network

Resistance

Setup design variable C and R and transient simulation as shown in Figure 8, C is constant and R is sweeping.

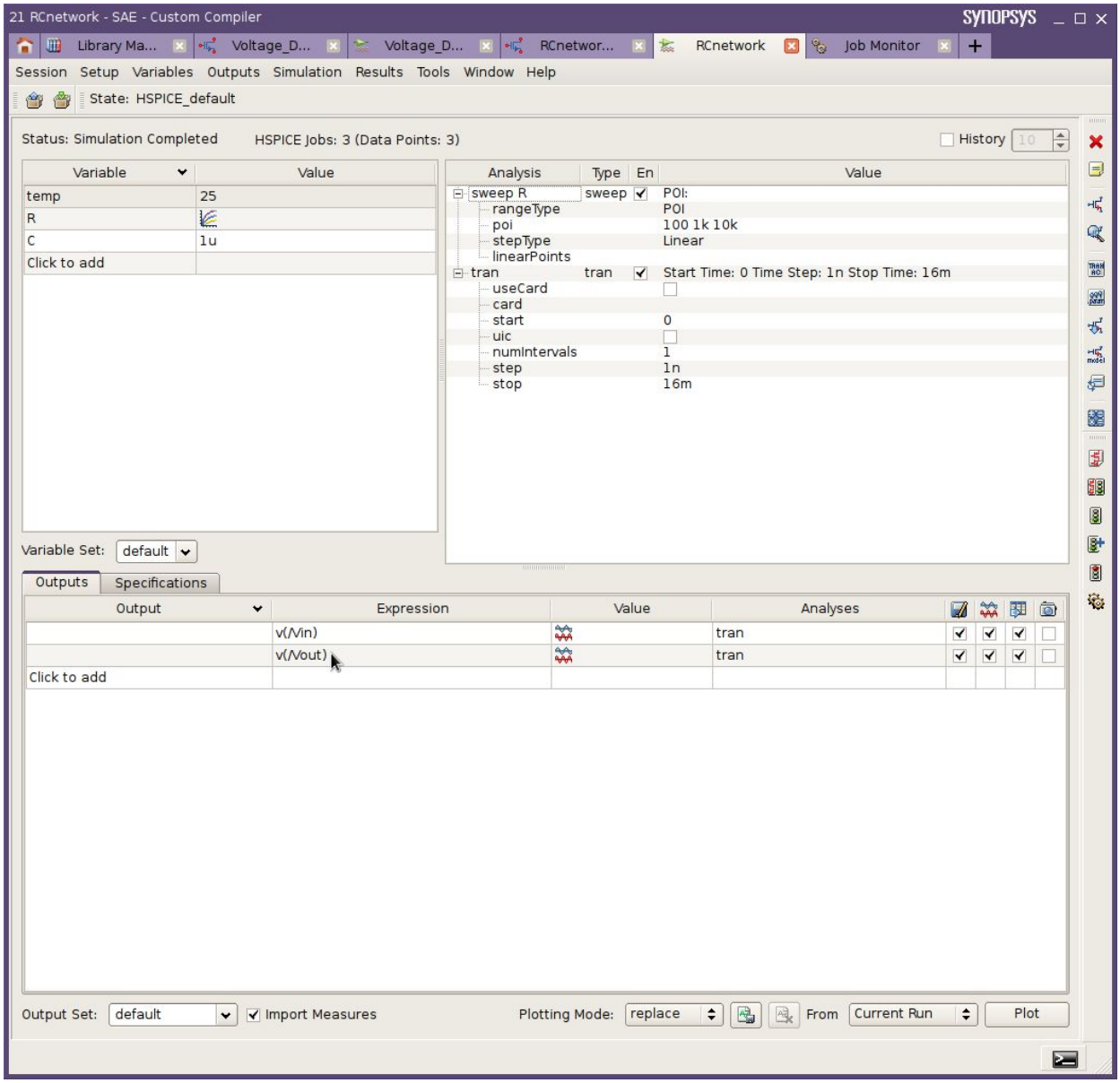

Figure 8. ASE of resistance sweep

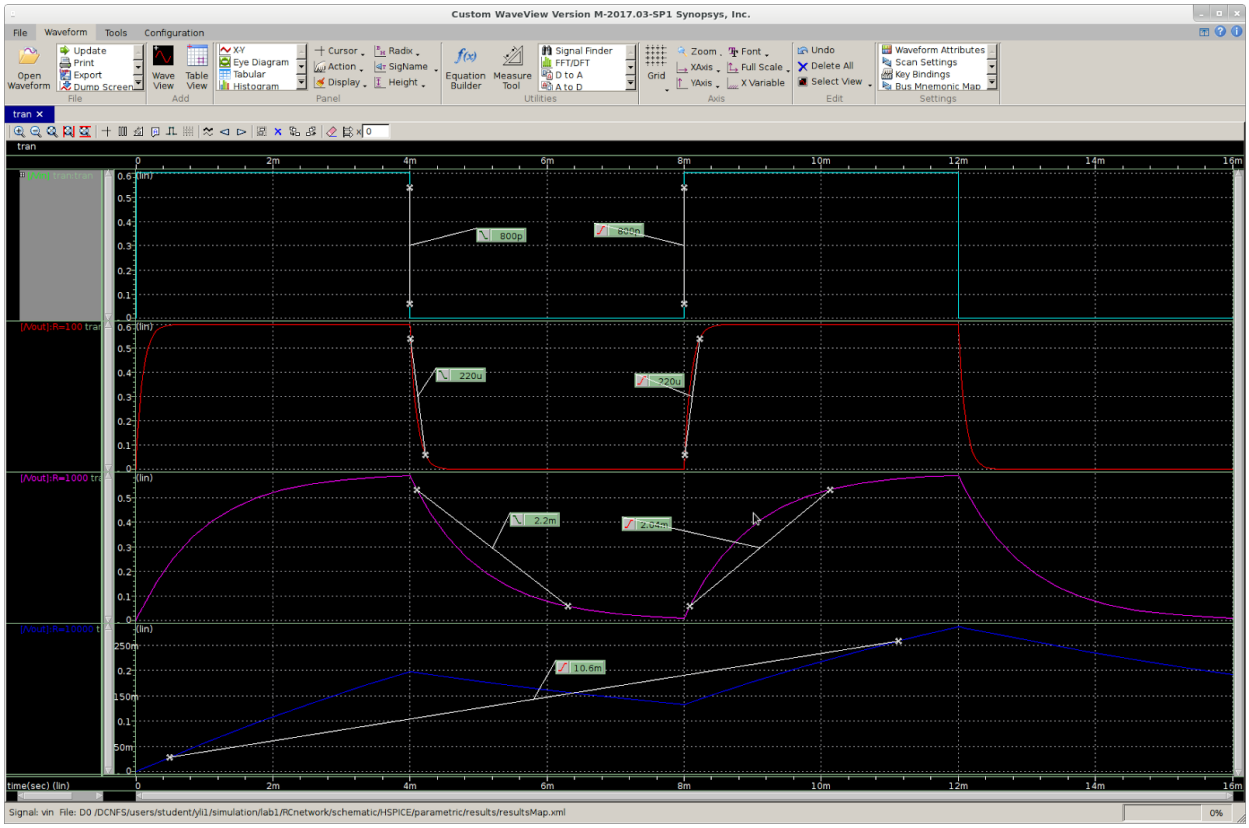

Figure 9. Waveform of resistance sweep with rise and fall time.

R(Ω)	Fall time	Rise time
100	220 us	220 us
1k	2.2 ms	2.04 ms
10k	10.6m	

When R = 10k, Vout is not able to rise and full periodically like when R = 100 Ω and R = 1k Ω , because Vin is changing so fast (almost instantly) that Vout starts to decrease before reaching 90% of the maximal voltage, and likewise, Vout starts to increase before reaching 10% of the minimum.

Capacitance

Setup design variable C and R and transient simulation as shown in Figure 10, R is constant and C is sweeping.

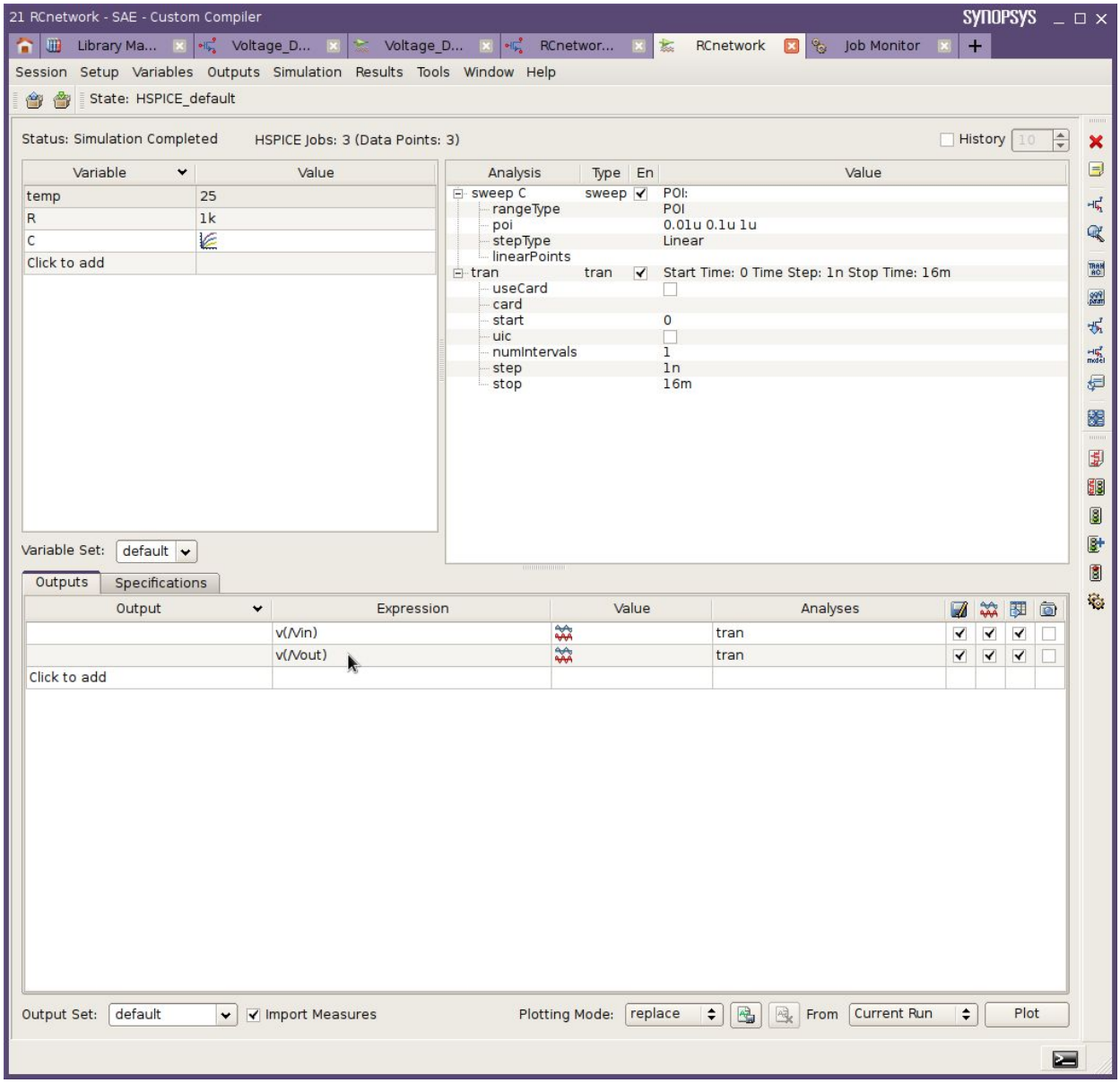

Figure 10. SAE of capacitance sweep

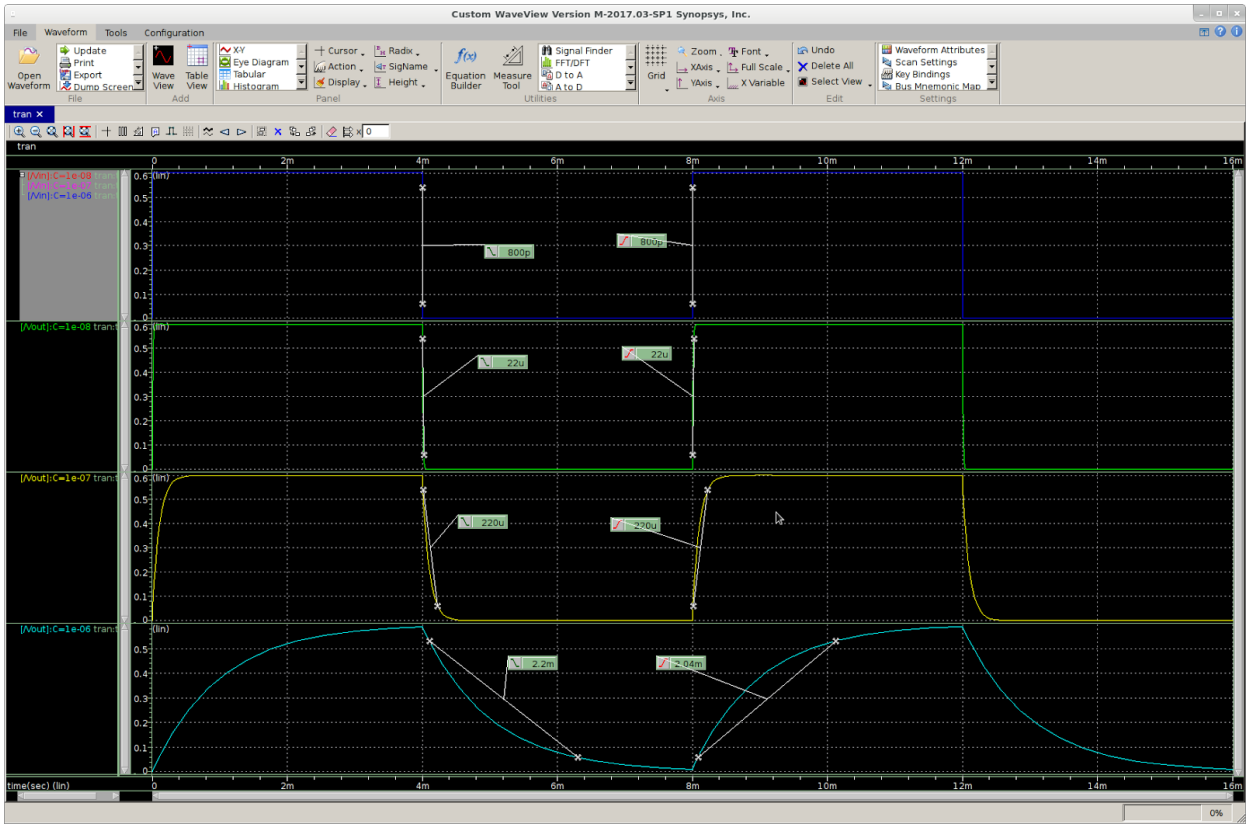

Figure 11. Waveform of capacitance sweep with rise and fall time.

C(uF)	Fall time	Rise time
0.01	22 us	22 us
0.1	220 us	220 us
1	2.2 ms	2.04ms

3. Conclusion

From this lab, I learn how to use Synopsys, and I have to say that this is a really complicated program, which may imply that we can do a lot of things with it. In my opinion, he example of building NMOS is very helpful, I learn how to create a cell and view under it, and how to add instances and change their attributes, and how to sweep variables, and how to draw multiple curves using parametric analysis.

The waveform and data obtained from it prove the correctness of the conjecture that I made in prelab about the behavior of Vout in voltage divider depending on the variation of R0, R1, and Vdd, and about the behavior of Vout in RC network depending on the variation of R and C.

Hopefully I can get more familiar with Synopsys and stop making minor or even hilarious mistakes in the future.