SANTA CLARA UNIVERSITY	ELEN 153	Dr. S. Krishnan T.A. Sanad Kawar
Laboratory #5: 3-Input NAND Layout		

I. OBJECTIVES

- To create a layout for the NAND gate and verify it with DRC and LVS
- To perform parasitic extraction and post-layout simulations.

II. LAB PROCEDURE

1. NAND Layout

- Open the Library that you created last week for the 3-input NAND gate.
- Create a layout view for your 3-input NAND gate. Remember that your layout view should be within the same NAND cell that you created the schematic view in.
- Use the tutorial as a reference for different steps. Also, refer to the Design rules Excel sheet provided by your T.A.

2. DRC and LVS

- Perform a Design Rules Check (DRC) as well as a Layout vs. Schematic (LVS) test
- Adjust your layout if necessary to fix any errors.
- Refer to your tutorial as a reference for different steps. Also note that the tutorial includes a troubleshooting guide.

Question: What you have you done to reduce area and improved performance?

III. REPORT

Write a short laboratory report that details all the work done. Describe the objective and procedures of this lab with your own words. The lab report should contain the following:

a) All schematics and layouts used in your lab.
b) Screenshots showing your design passed DRC and LVS
c) Answer any questions in the lab assignment
d) Conclusions