47363 ELEN 21L

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Laboratory #5

Jusman Singh, Yuan Wang

Introduction

By the end of lab, we should learn how to do hierarchical design and how to use busses for multi-bit inputs. We also should learn design a 4-bit carry adder using half adders and full adders as building blocks. Then we should use 7-segment displays to show inputs and outputs of the design.

Procedure

Because we have done the full-adder and half adder in the pre-lab, we started to test truth table of the two adders to see if there could be a problem. In Figure 1 and 2, the waveform showed our full-adder and half adder were correct.

Then we designed a 4-bit ripple carry adder by connect 4 full adder together. For input, we used bus tool to set a 4 bit input and connected each of bit to each full adder. Then for output, we connected all Sum out to a 4-bit output. In figure 3, it clearly showed our designed circuit.
Then we tested the truth table of this circuit by input different numbers. For first case, we input 0111, 0011 and 0 Cin. Then we got 1010 and 0 Cout. For second case, we input 0011, 1000 and 1 Cin. Then we got 1100 and 0 Cout. For third case, we input 1111, 0001, and 1 Cin. Then we got 0001 and 1 cout. For last case, we input 1000, 1000 and 0 Cin. Then we got 0000 and 1 Cout. Therefore, we could conclude our inputs, carry-in, carry-out and sum work correctly.

We created a file in order to set a seven segment display of our inputs and outputs. In the file, we set 16 different values. Then we connected the display symbol to inputs and outputs in our circuit, and we connect LEDs to carry in and carry out.

Overall, we set switches to input values and let the values to be displayed in a readable form on the board. Then by going through our 4-bit ripple adder, those inputs could be added and sum of these inputs could be displayed in 7 segment form.

Conclusion

Today we used full adders that we designed in pre-lab to implement a 4-bit ripple carry adder. We also were familiar with buses tools to set multiple inputs and outputs. Then in the end, we learned to set display of output on the FPGA board, which is a more convenient way to see results.

Questions

1. LED for carry out should be turned on and 7-segment displays should be off, because we didn't implement 7-segment display for values greater than 15.
2. 20 gates.
3. I don't think we can combine two 4-bit adder and we should use 8 full-adders and connect them in the same way that I build 4-bit adder.
4. 40 gates.

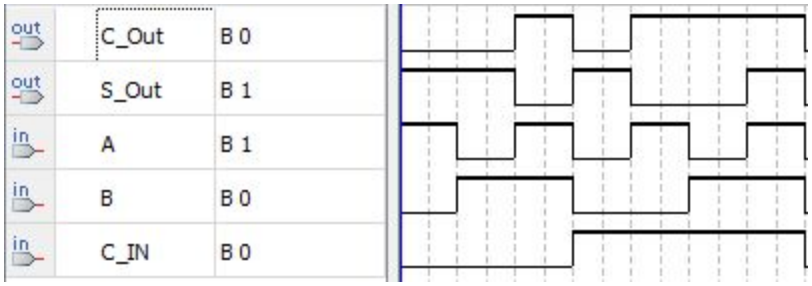

Figure 1 : The simulation of the Full Adder.

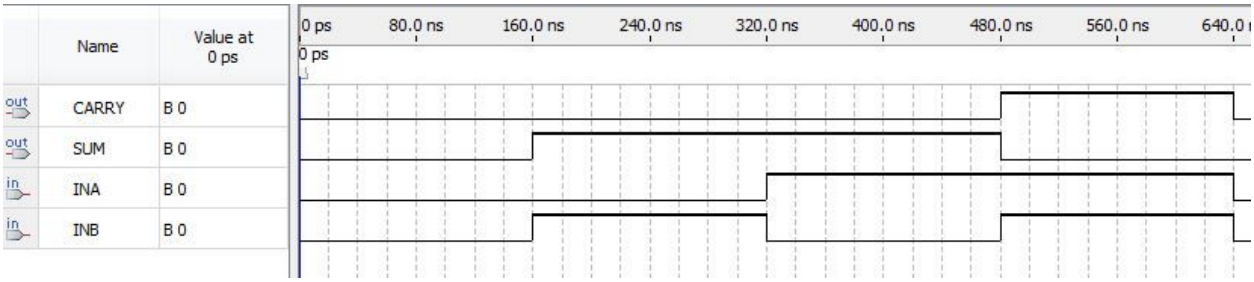

Figure 2 : The simulation of the Half Adder.

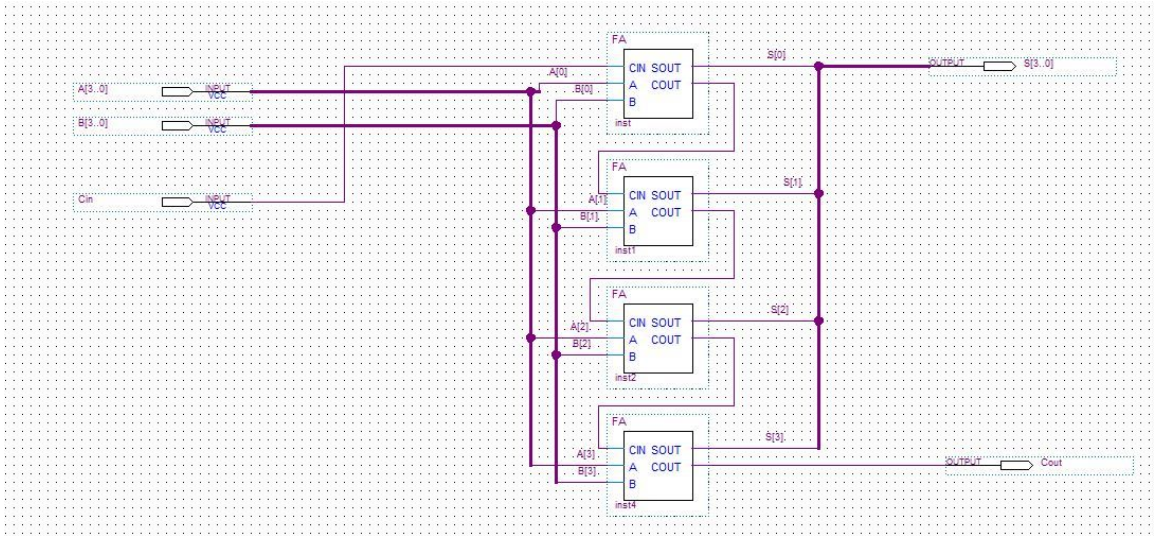

Figure 3 : The 4-Bit Ripple Carry Adder implemented in the schematics file.

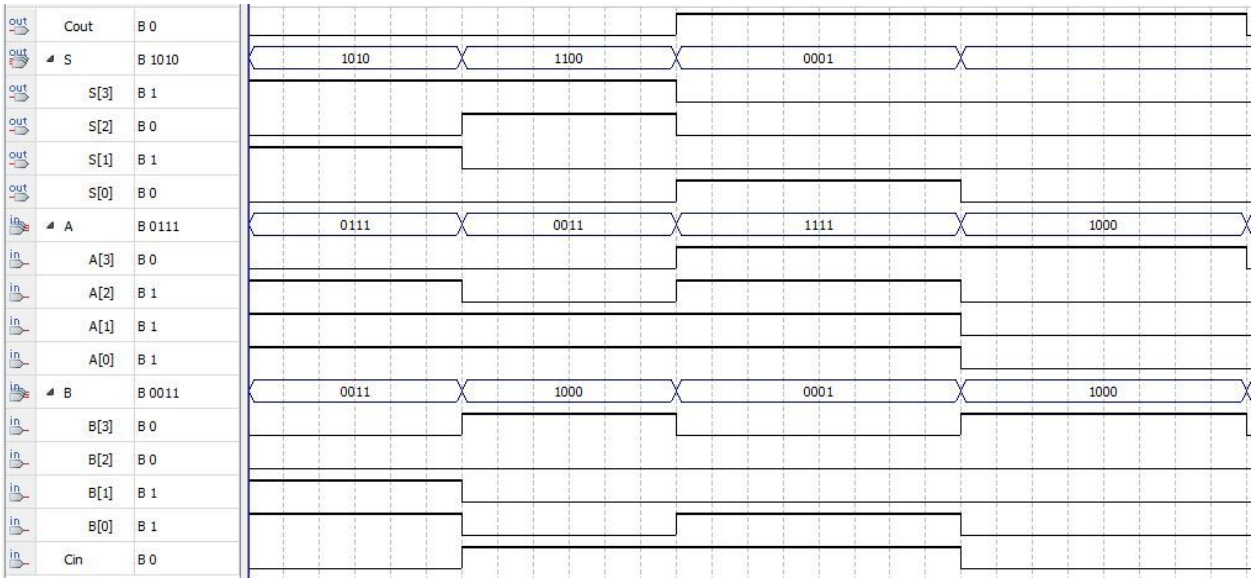

Figure 4 : The truth table for 4-Bit Ripple Carry Adder

```
1   module bin_7seg(bi_digit,seg);
2   input [3:0] bi_digit;
3   output [6:0] seg;
4   reg [6:0] seg;
5   // seg = {g,f,e,d,c,b,a};
6
7
8   always @ (bi_digit)
9   case (bi_digit)
10          4'h0: seg = ~7'b0111111;
11          4'h1: seg = ~7'b0000110;            // ---a----
12          4'h2: seg = ~7'b1011011;            // |      |
13          4'h3: seg = ~7'b1001111;            // f      b
14          4'h4: seg = ~7'b1100110;            // |      |
15          4'h5: seg = ~7'b1101101;            // ---g----
16          4'h6: seg = ~7'b1111101;            // |      |
17          4'h7: seg = ~7'b0000111;            // e      c
18          4'h8: seg = ~7'b1111111;            // |      |
19          4'h9: seg = ~7'b1100111;            // ---d----
20          4'ha: seg = ~7'b1110111;
21          4'hb: seg = ~7'b1111100;
22          4'hc: seg = ~7'b1011000;
23          4'hd: seg = ~7'b1011110;
24          4'he: seg = ~7'b1111001;
25          4'hf: seg = ~7'b1110001;
26  endcase
27
28  endmodule
29
```

Figure 5: The 7-Segment Display file and implementation of the defined characters.

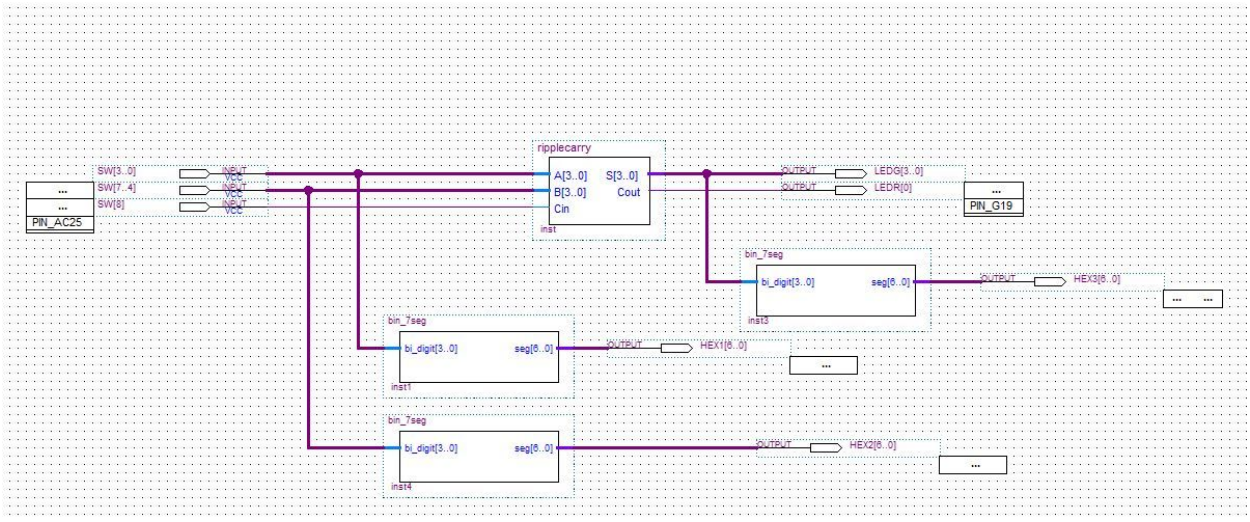

Figure 6 : The 4-Bit Ripple Carry Adder with 7-Segment Display file integrated in the project.

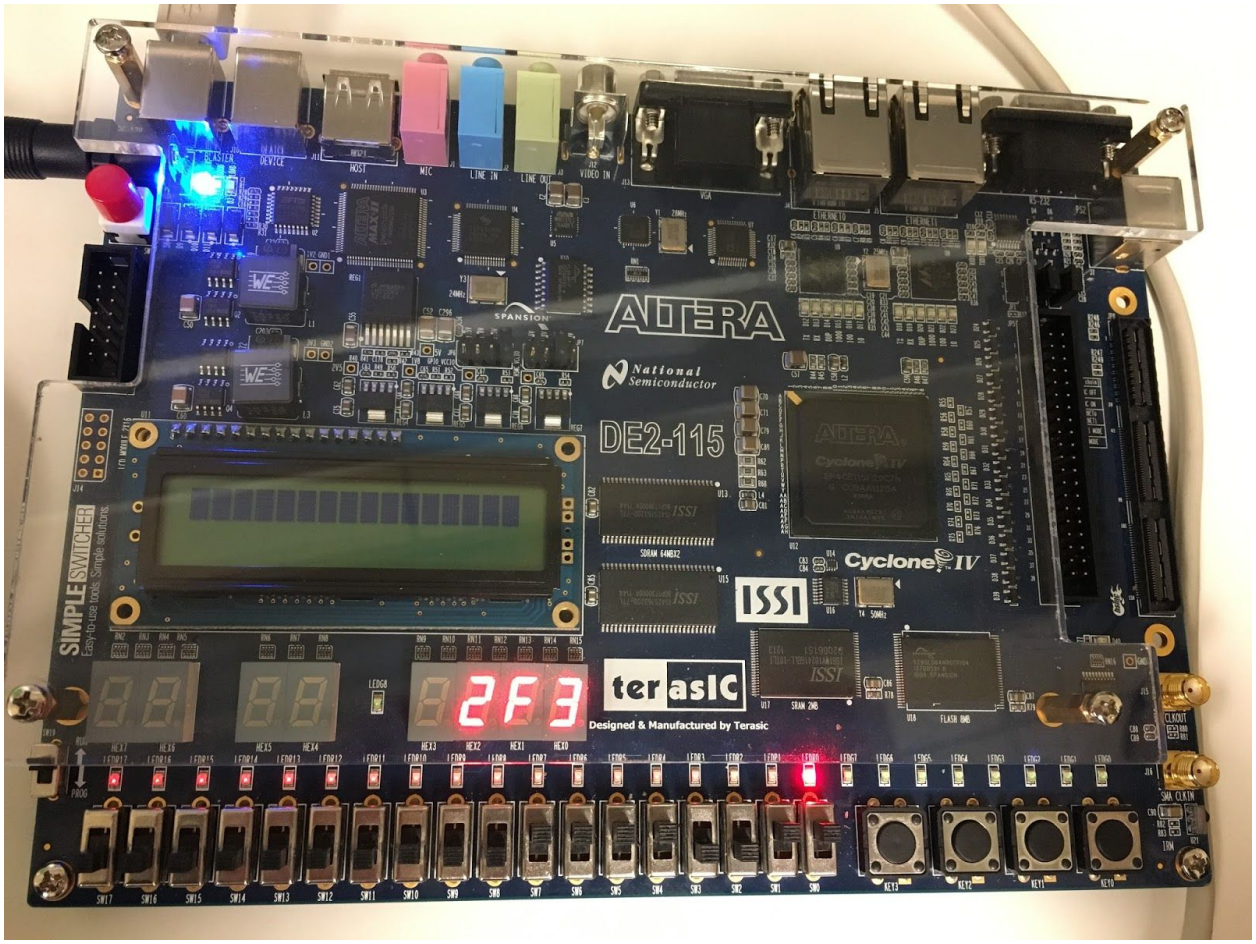

Figure 7 : Shows the 7-Segment Display in work as well as the Carry-Out (displayed as a red LED Light).