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Laboratory #3: Two Level Circuit Design

For lab sections April 25-28, 2017

I. OBJECTIVES

- To design, test, and implement a circuit based on a functional specification.
- To translate a problem statement into an algebraic representation.
- To simplify the algebraic representation using Kmaps to find the minimized logic implementation.
- To Implement and test the circuit on an Altera FPGA

PROBLEM STATEMENT

In this laboratory assignment, you will design a highway entrance ramp metering controller with the following specifications for controlling the release of traffic from an entrance ramp onto a highway:

There are three metered entrance lanes: one carpool lane and two others for cars that are not carpool. Each lane has its own light ("red" for stop and "green" for go) and its own sensor to detect a waiting car. The carpool lane is given priority for a green light over the other two lanes. Otherwise, a "round robin" scheme is used in which the green lights alternate between the left and right lanes.

The controller has these four inputs:

CS	car pool lane car sensor	All three sensors are a "1" when a car is present, and a "0" when no car is present.
LS	left lane car sensor	
RS	right lane car sensor	
RR	round robin signal	RR is "1" or "0" to select the left and right lanes, respectively

The three controller outputs are:

CL	car pool light	All three lights are a "1" for green, and a "0" for red.
LL	left lane light	
RL	right lane light	

The controller operates as follows:

1. If there is a car in the car pool lane, CL is 1.
2. If there are no cars in the car pool lane and the right lane, and there is a car in the left lane, LL is 1.
3. If there are no cars in the carpool lane and in the left lane, and there is a car in the right lane, RL is 1.
4. If there is no car in the car pool lane and there are no cars in the left and right lanes, then RL is 1.
5. If there is no car in the car pool lane, there are cars in both the left and right lanes, and RR is 1, then LL = 1.
6. If there is no car in the car pool lane, there are cars in both the left and right lanes, and RR is 0, then RL is 1.

If any of CL, LL, or RL is not specified to be 1 in conditions 1 to 6 above, then it has value 0 for that condition.

II. PRE-LAB

The Design process:

- Review lecture material on K-maps and logic design.
- Read the problem statement and clearly identify the inputs and outputs for the circuit you are designing.
- From the problem statement, write algebraic expressions for the traffic controller outputs
- Create K-maps for the functions and find the minimized SOP implementation using AND and OR logic gates with as many inputs as needed.
- Find minimized logic function in POS form.
- Compare the cost of the POS form and the SOP form when the cost is measured by the sum of the number of logic gates and the number of inputs to all logic gates.

III. LAB PROCEDURE

Reminder about relevant links from Lab 2:

The following Altera tutorial is what you will work through to get familiar with schematic entry and compilation (pages 3-20), pin assignment (page 24), and programming and testing (pages 31-41):
ftp://ftp.altera.com/up/pub/Altera_Material/12.1/Tutorials/Schematic/Quartus_II_Introduction.pdf

The below link gives details on waveform simulation methods (pages 3-12):
ftp://ftp.altera.com/up/pub/Altera_Material/13.1/Tutorials/Verilog/Quartus_II_Simulation.pdf

The below link gives details on pin assignment tables (pages 35-38 and pages 48-49):
ftp://ftp.altera.com/up/pub/Altera_Material/12.1/Boards/DE2-115/DE2_115_User_Manual.pdf

Schematic Entry and Simulation:

1. Draw the schematic for your design using the schematic editor in the Quartus II program. Refer to the tutorials if needed. Do a screen capture of your schematic.
2. Simulate your design for various inputs and verify that it functions correctly.
3. Add a new output ZZ to your circuit that will be 1 when there are no cars waiting in any of the lanes. This could be used by a regional traffic management system.

FPGA Implementation:

4. Assign pins for the inputs and outputs. Note that two nodes may be connected either by drawing a wired connection between them or by assigning the same name to both nodes.
    a. Connect the inputs of your circuit to switches on the board.
    b. Connect the traffic controller outputs to the LEDs on the board.
5. Download the circuit onto the FPGA board.
6. Test your design for all possible input conditions and, when it is working, demonstrate it to your lab instructor. Make sure you demonstrate the complete functioning of your circuit.

IV. REPORT

To be completed with your lab group and turned-in at the beginning of the next lab.

- Write an introduction about what your group accomplished during the lab.
- Include your graded Pre-labs
- Include your schematic, simulation results, and proof of successful download and functioning on the FPGA.
- Describe how you would modify your circuit to include a fifth input TM, a timer that is turned on at intervals controlled by the traffic density. When TM is "1", the circuit operates exactly as specified in the problem statement. When TM is "0", all output lights are red.