

數位系統導論實驗

Lab8 Vivado & Nexys4 FPGA

Outline

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- 操作範例
- 作業說明及評分方式
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課程目標

- 熟悉 Vivado 開發套件 & Nexys4 DDR FPGA 開發板
- 以 FPGA 實現加法器與 Lab 之生日顯示器

Nexys 4 FPGA Board

- FPGA (Field-Programmable Gate Array) 為可重複程式設計的晶片，可幫助使用者建立自己所需要的系統；其架構包括正反器、查找表、乘法器等。
- Nexys 4 是基於 Xilinx Artix-7 FPGA 的嵌入式系統開發平台，擁有外部記憶體、USB 插槽與乙太網路等其他 I/O 接口。

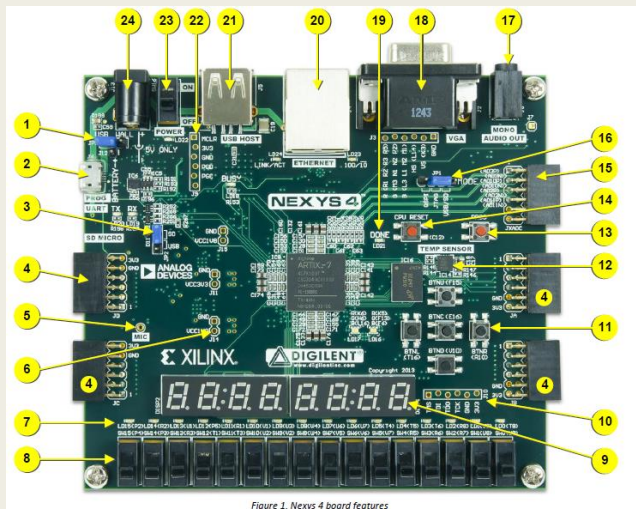
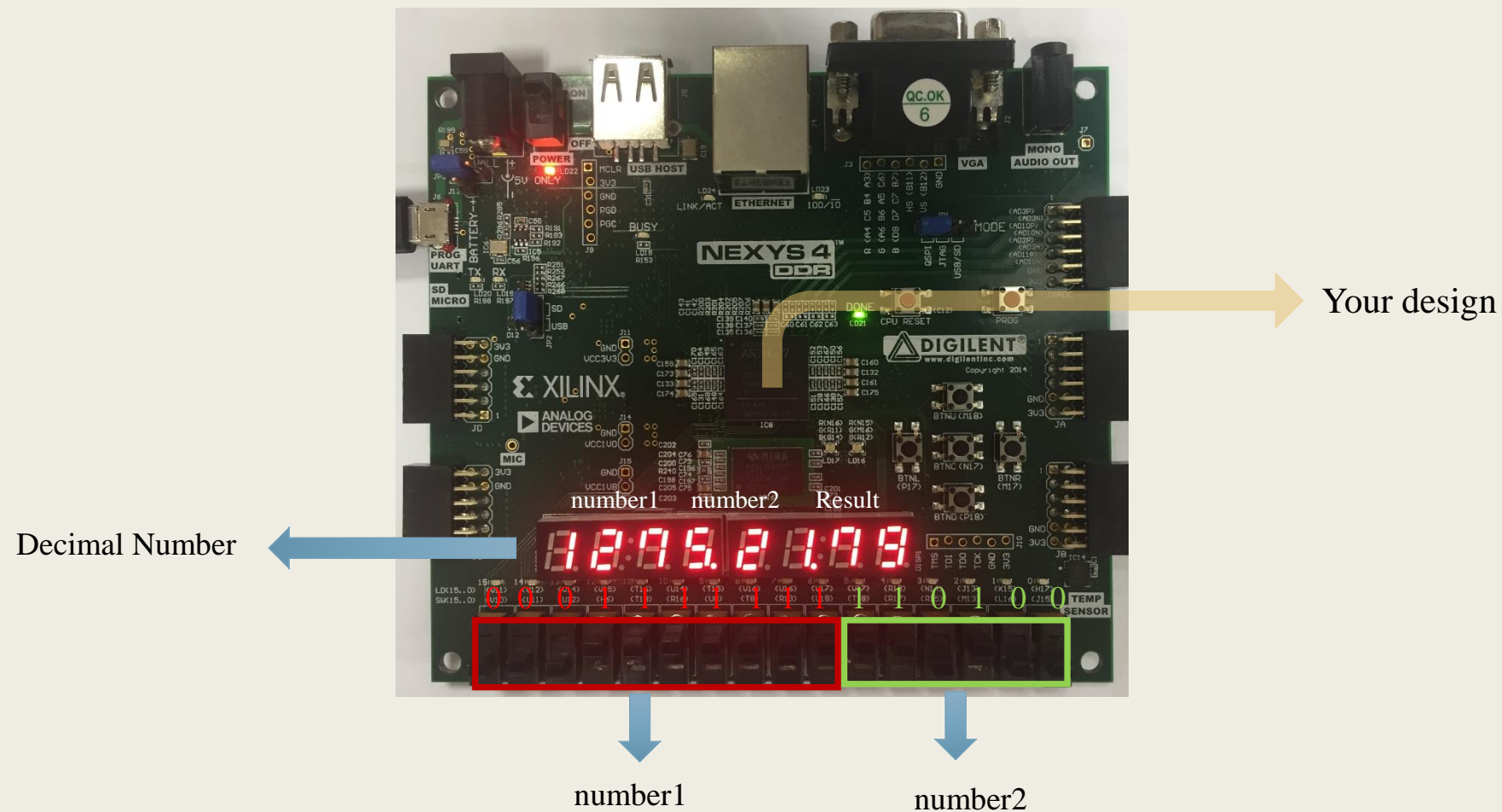


Figure 1. Nexys 4 board features

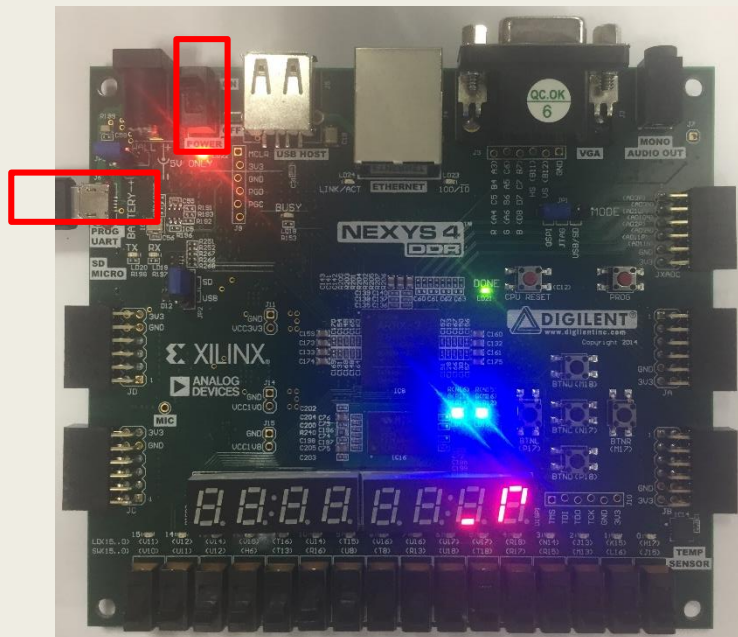
| Callout | Component Description | Callout | Component Description |
|---------|--|---------|--------------------------------------|
| 1 | Power select jumper and battery header | 13 | FPGA configuration reset button |
| 2 | Shared UART/ JTAG USB port | 14 | CPU reset button (for soft cores) |
| 3 | External configuration jumper (SD / USB) | 15 | Analog signal Pmod port (XADC) |
| 4 | Pmod port(s) | 16 | Programming mode jumper |
| 5 | Microphone | 17 | Audio connector |
| 6 | Power supply test point(s) | 18 | VGA connector |
| 7 | LEDs (16) | 19 | FPGA programming done LED |
| 8 | Slide switches | 20 | Ethernet connector |
| 9 | Eight digit 7-seg display | 21 | USB host connector |
| 10 | JTAG port for (optional) external cable | 22 | PIC24 programming port (factory use) |
| 11 | Five pushbuttons | 23 | Power switch |
| 12 | Temperature sensor | 24 | Power jack |

操作範例



Step1 - Nexys 4 開機

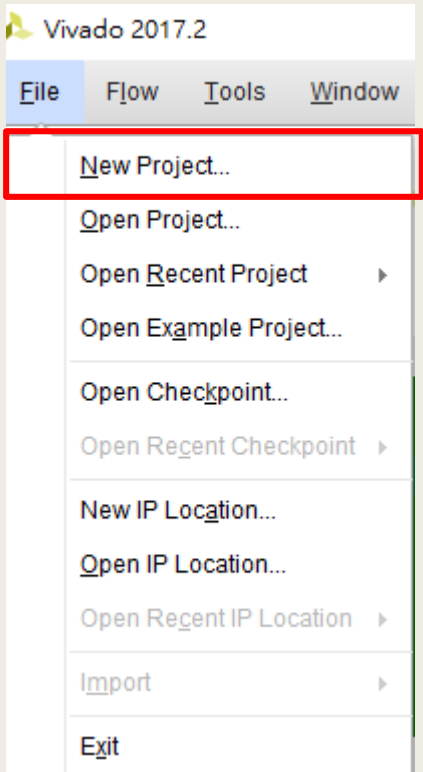
- 使用 USB 線接上 UART 再連接到電腦
- 開啟電源開關 (Power switch)

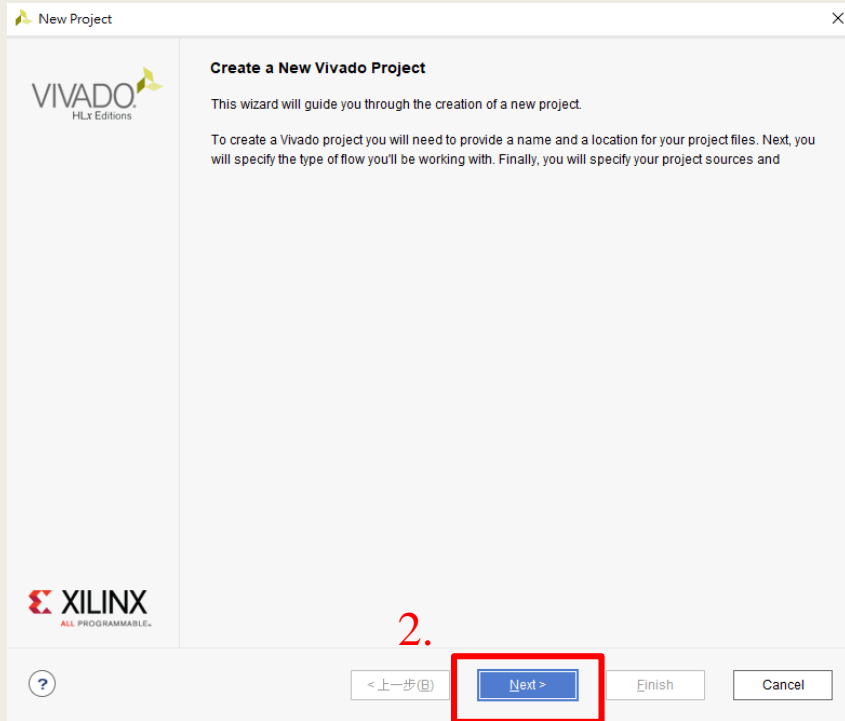


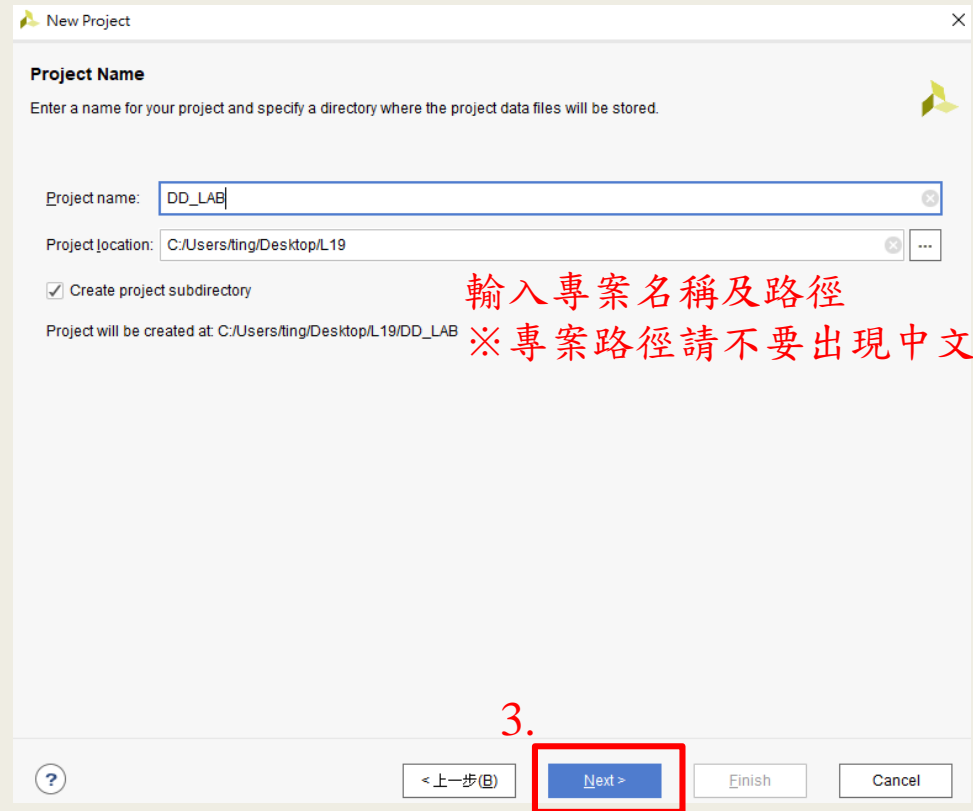
Step2 – 安裝 Vivado

- 使用 google 搜尋 Vivado 進入官網，根據課程檔案中的安裝教學依序執行。

Step3 – 建立專案 (1/2)

1.  Vivado 2017.2 File menu. The 'New Project...' option is highlighted with a red box.

2.  'New Project' wizard screen. The 'Next >' button is highlighted with a red box.

3.  'New Project' wizard screen. The 'Project Name' field is set to 'DD_LAB' and the 'Project location' is 'C:/Users/ting/Desktop/L19'. The 'Next >' button is highlighted with a red box.

輸入專案名稱及路徑
※專案路徑請不要出現中文

Step3 – 建立專案 (2/2)

New Project

Project Type
Specify the type of project to create.

☒ **RTL Project**
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.
☒ Do not specify sources at this time

☐ **Post-synthesis Project**
You will be able to add sources, view device resources, run design analysis, planning and implementation.
☐ Do not specify sources at this time

☐ **I/O Planning Project**
Do not specify design sources. You will be able to view part/package resources.

☐ **Imported Project**
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**
Create a new Vivado project from a predefined template.

4.

New Project

Default Part
Choose a default Xilinx part or board for your project. This can be changed later.

Select:

Filter

Product category: All Speed grade: -3

Family: Artix-7 Temp grade: All Remaining

Package: csg324

Reset All Filters

Search: Q-

| Part | I/O Pin Count | Available IOBs | LUT Elements | FlipFlops | Block RAMs | Ultra RAMs | DSPs | Gb Transceivers | GTPE2 Transceiv |
|-----------------|---------------|----------------|--------------|-----------|------------|------------|------|-----------------|-----------------|
| xc7a15tcs324-3 | 324 | 210 | 10400 | 20800 | 25 | 0 | 45 | 0 | 0 |
| xc7a35tcs324-3 | 324 | 210 | 20800 | 41600 | 50 | 0 | 90 | 0 | 0 |
| xc7a50tcs324-3 | 324 | 210 | 32600 | 65200 | 75 | 0 | 120 | 0 | 0 |
| xc7a75tcs324-3 | 324 | 210 | 47200 | 94400 | 105 | 0 | 180 | 0 | 0 |
| xc7a100tcs324-3 | 324 | 210 | 63400 | 126800 | 135 | 0 | 240 | 0 | 0 |

5.

New Project

New Project Summary

VIVADO
HLx Editions

XILINX
ALL PROGRAMMABLE.

To create the project, click Finish

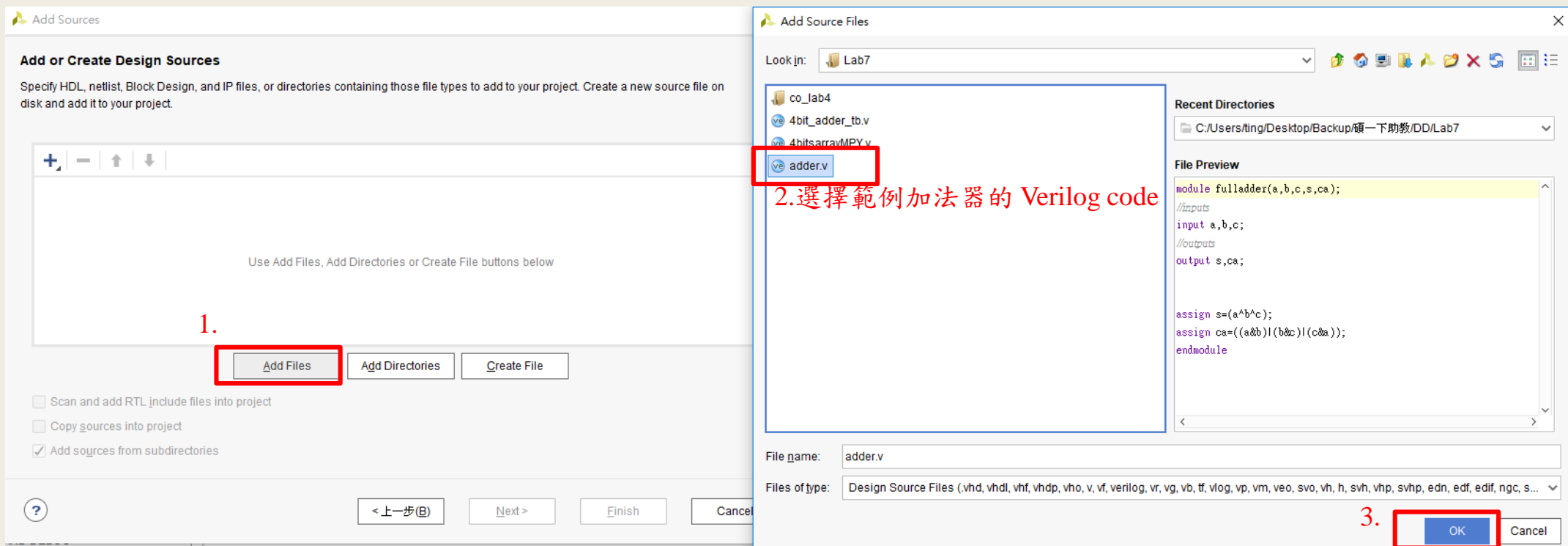
6.

Step4 – 加入原始碼 (1/2)

- 點擊 + 號新增檔案
- 選擇檔案類型
 - *constraints* 可以新增 .xdc 檔
 - *design sources* 可以新增 .v 檔
- .xdc 用來描述.v與實體線路的連接關係
- .v 用來描述硬體行為

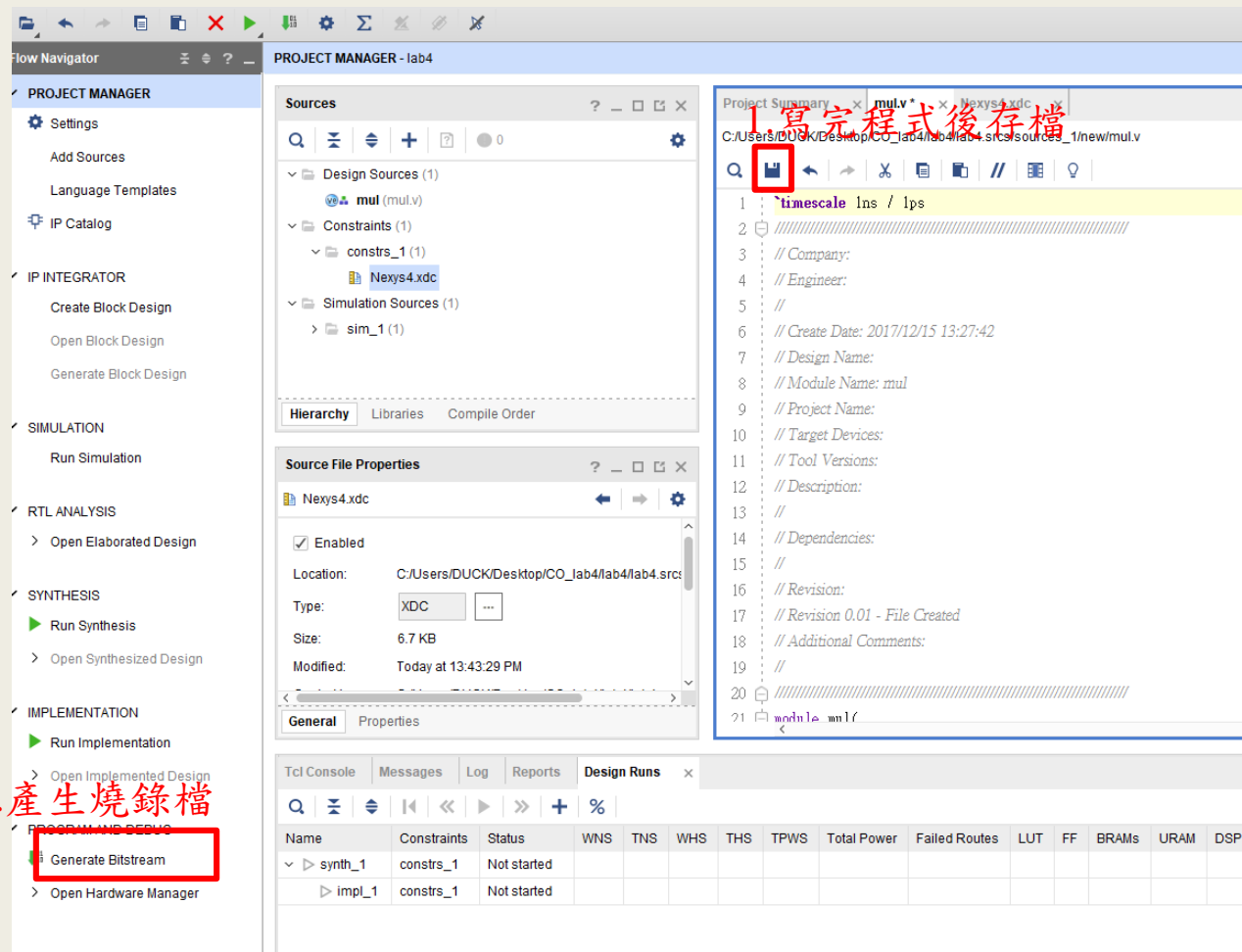


Step4 – 加入原始碼 (2/2)



Step5 – Generate Bitstream

1. 寫完程式後存檔



2. 產生燒錄檔

| Name | Constraints | Status | WNS | TNS | WHS | THS | TPWS | Total Power | Failed Routes | LUT | FF | BRAMs | URAM | DSP |
|---------|-------------|-------------|-----|-----|-----|-----|------|-------------|---------------|-----|----|-------|------|-----|
| synth_1 | constrs_1 | Not started | | | | | | | | | | | | |
| impl_1 | constrs_1 | Not started | | | | | | | | | | | | |

Bitstream Generation Completed

Bitstream Generation successfully completed.

Next

☐ View Reports

☒ Open Hardware Manager

☐ Generate Memory Configuration File

☐ Don't show this dialog again

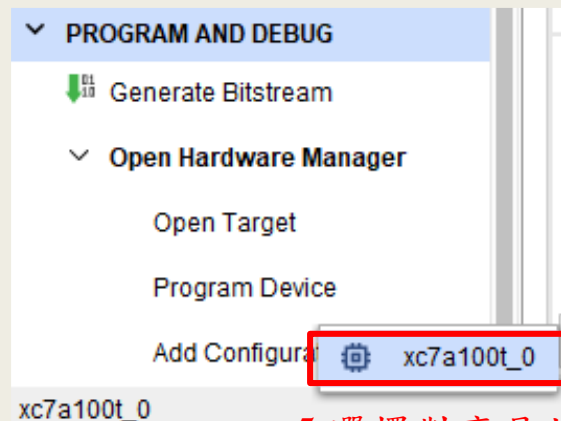
OK Cancel

3. 打開 Hardware Manager 連結 Nexys 4

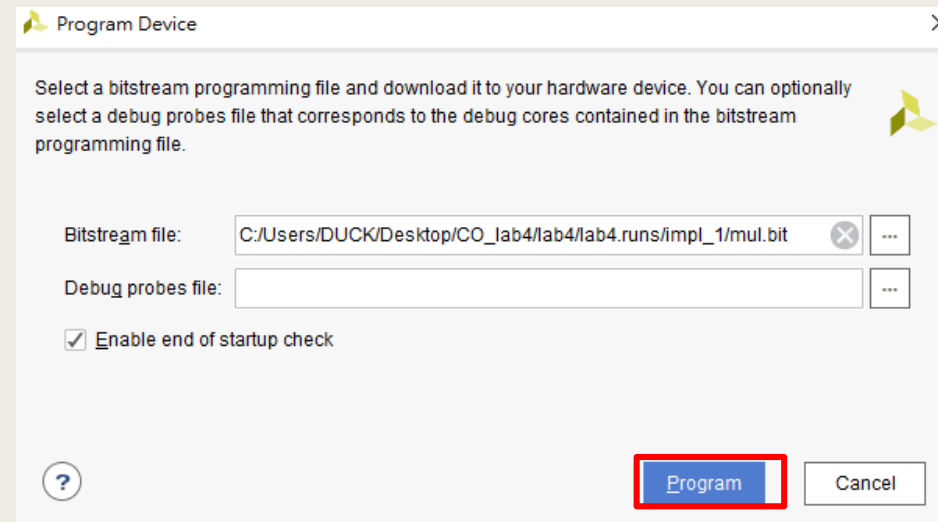
Step6 – Program FPGA



4.自動連接板子



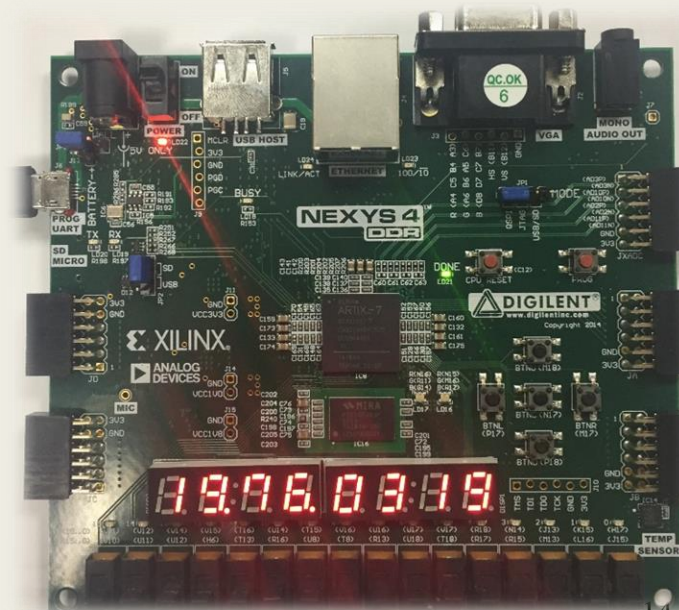
5.選擇對應晶片



6.燒錄程式

作業說明及評分方式

- 作業Part1 : Demo 時按造步驟正確呈現範例練習的結果
- 作業Part2 :
 - 使用 Lab6 的生日產生器在 Nexys 4 七段顯示器顯示你的生日
 - xdc 檔使用課程提供的 Nexys4.xdc
- 課堂抽問 : Demo時助教隨機抽問問題
- 請同學 Demo 時帶著 Part1 及 Part2 的專案檔



作業說明及評分方式

- Demo時間：測驗時間共分四梯次，分別為19:20、19:40、20:00與20:20
- Demo梯次：與 Lab1 相同
- Demo地點：資工館 501A
- 評分方式：part1 30%，part2 40%，課堂抽問 30%

附錄

- 不能同時讓八個七段顯示器顯示出不同的數字
- 利用視覺暫留，讓七段顯示器顯示數值
- 接線部分可以參考.xdc檔

