DSD Final Project Scores (RISC-V)

1. Baseline

(1) Area: 261036 (um^2)

截圖:

```
Number of ports:                         2166
Number of nets:                         21765
Number of cells:                        20168
Number of combinational cells:          15537
Number of sequential cells:              4622
Number of macros/black boxes:               0
Number of buf/inv:                       5773
Number of references:                       8

Combinational area:             141939.983929
Buf/Inv area:                    34795.002348
Noncombinational area:          119096.375593
Macro/Black Box area:                0.000000
Net Interconnect area:         2467512.625977

Total cell area:                 261036.359522
Total area:                     2728548.985499
1
```

(2) Total Simulation Time of given hasHazard testbench: 9197(ns)

截圖:

```
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 9197850 PS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
ncsim> exit
[b06190@cad29 src]$
```

(3) Area*Total Simulation Time: (um^2 * ns)

2.4*10^9

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): 4.0(ns)

2. BrPred

(1) Total execution cycles of given I_mem_BrPred: 667 cycles

截圖: tb cycle = 10ns

```
Branch Part A is complete.

Branch Part B is complete.

Branch Part C is complete.

------------------------- Simulation FINISH !!-------------------------
=============================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

=============================================================================
Simulation complete via $finish(1) at time 6675 NS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
ncsim> exit
[b06190@cad30 ~/src]$
```

(2) Total execution cycles of given I_mem_hasHazard: 1758 cycles

截圖: tb cycle = 10ns

```
------------------------- Simulation FINISH !!-------------------------
=============================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

=============================================================================
Simulation complete via $finish(1) at time 17585 NS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
ncsim> exit
[b06190@cad30 ~/src]$
```

(3) Synthesis area of BPU (Total area of BrPred minus baseline design, two design clock cycle need to be same): (um^2)

10702 um^2

Sdc cycle = 5ns

3. L2 Cache

(1) Average memory access time: (ns)

Cycle=5(ns)

Time for a hit=1 cycle ; Miss penalty when accessing data in L2=1 cycle ; Miss penalty when accessing data from slow memory=6 cycle

AMAT=1+0.394*1+0.394*0.25*6=1.985 clock cycles

Average memory access time=1.985*5=9.925 (ns)

(2) Total execution time of given I_mem_L2Cache: 6441 (ns)

截圖:

```
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 6441750 PS + 0
./Final_tb.v:158              #(`CYCLE) $finish;
ncsim> exit
[b06190@cad29 src]$
```

4. Compressed instructions

(1) Area (Total area of compressed design minus baseline design, two design clock cycle need to be same): (um^2)

截圖:

```
Number of ports:                          2358
Number of nets:                          21114
Number of cells:                         19173
Number of combinational cells:           14533
Number of sequential cells:               4629
Number of macros/black boxes:                0
Number of buf/inv:                        3355
Number of references:                       10

Combinational area:             157493.256975
Buf/Inv area:                    29987.965912
Noncombinational area:          120366.030857
Macro/Black Box area:                0.000000
Net Interconnect area:         2430132.454071

Total cell area:                 277859.287832
Total area:                     2707991.741903
```

277859.287832 um^2

(2) Total Simulation Time of given I_mem_compression: (ns)

截圖:

```
------------------------- Simulation FINISH !!-------------------------
================================================================================

 \(^o^)/ CONGRATULATIONS!!  The simulation result is PASS!!!

================================================================================
Simulation complete via $finish(1) at time 2286900 PS + 0
./Final_tb.v:171              $finish;
ncsim> exit
```

2286.9 ns

(3) Area*Total Simulation Time: (um^2 * ns)

635436405.3430008

(4) Clock cycle for post-syn simulation (cycle in sdc, not cycle in testbench): (ns)
5.4 ns