HAUTE ÉCOLE D'INGÉNIERIE ET DE GESTION DU CANTON DE VAUD

Prof. Yann Thoma

Formal verification
Verification of a math computer
CERN training - July 2025

Module to verify

We want to verify a module able to do calculation of $a+a+b-c$. The three values are available as inputs, and a result is presented at the output after a certain time. The control protocol is pretty simple : a valid and a ready signal. If both are at `'1'` then the data is transmitted. This protocol is valid for both the input port and the output port.
As you will see in the code, the `math_computer` uses records as input/output. As it is not that convenient for writing assertions, the `.psl` files embeds aliases to help you with it.
The module has been built with two different architectures : datapath-control, and pipeline.
The assertions can be placed in three different files, depending on what architecture they can be applied on :

- `math_computer.psl` : Applied to both designs
- `math_computer_only_datapath.psl` : Applied only to the datapath-control version
- `math_computer_only_pipeline.psl` : Applied only to the pipeline version

As we have a pipeline version that would be very nice to check that the i^{th} result corresponds to the i^{th} started computation. Feel free to have a look at the FIFO examples in the `course/code` and do some copy-paste to help.