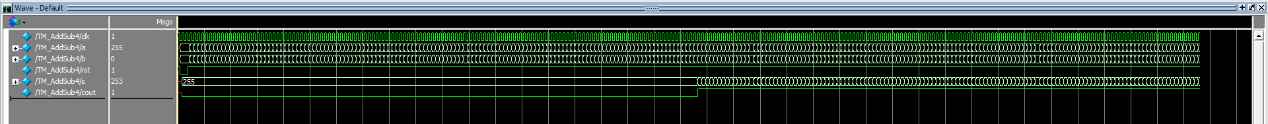
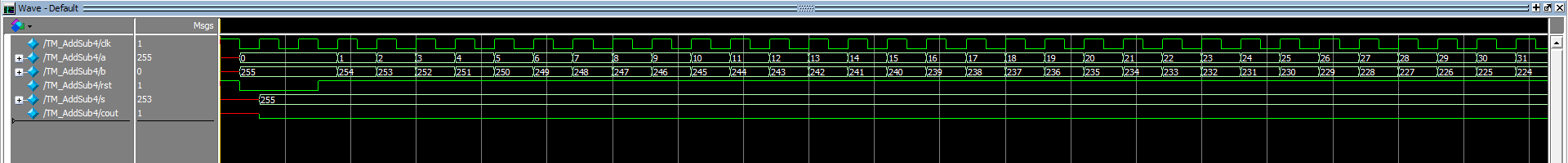
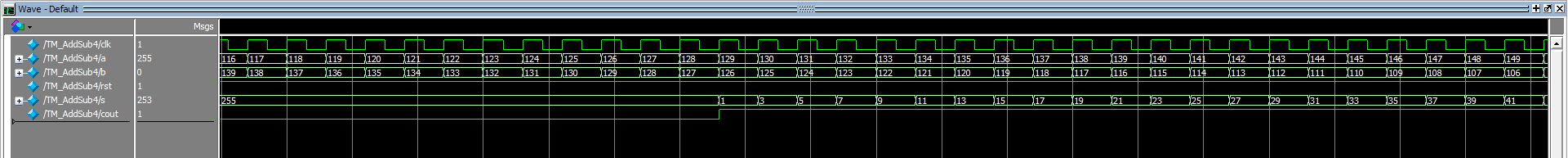
* Simulation waveform



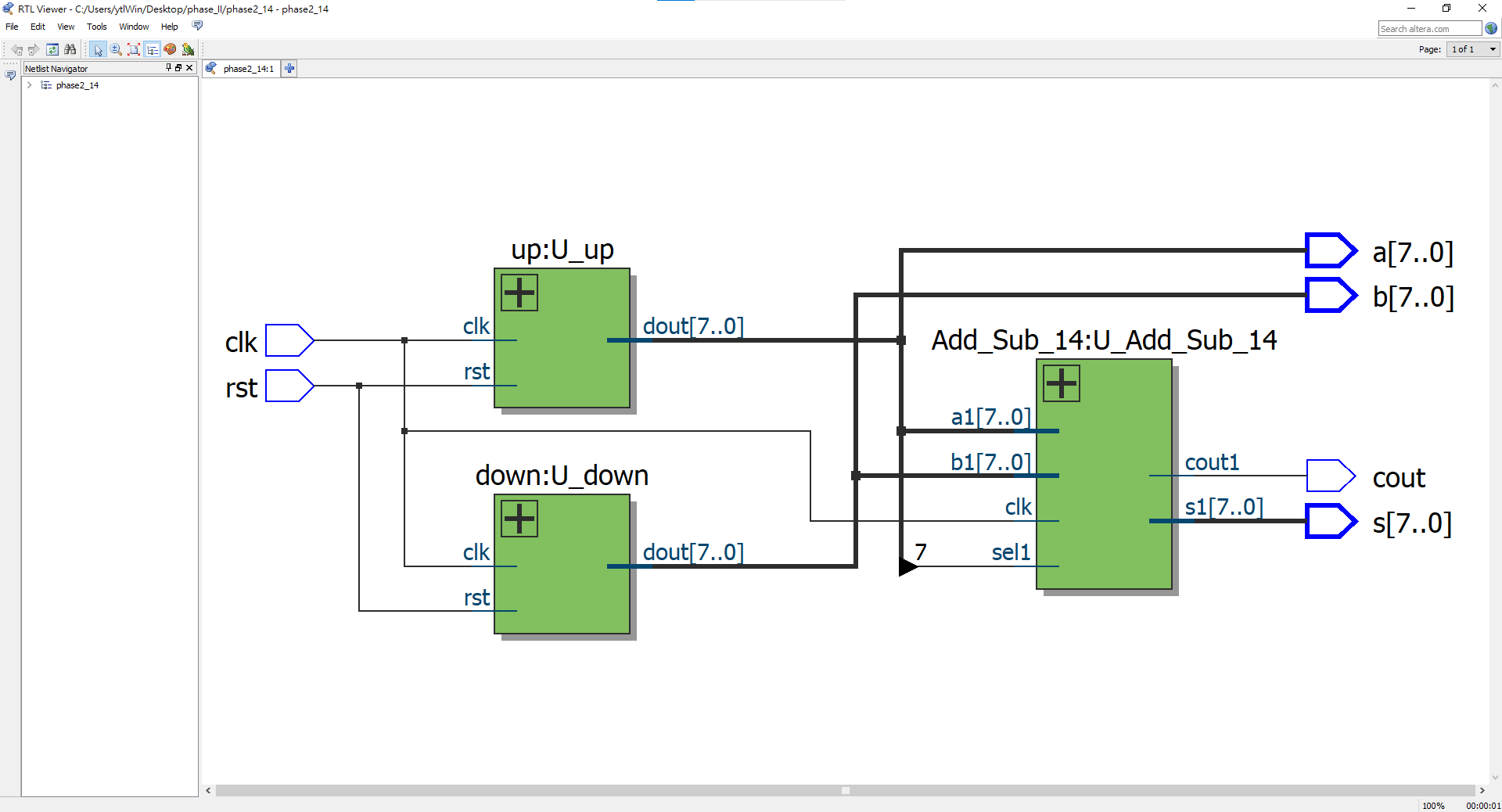
* 加法



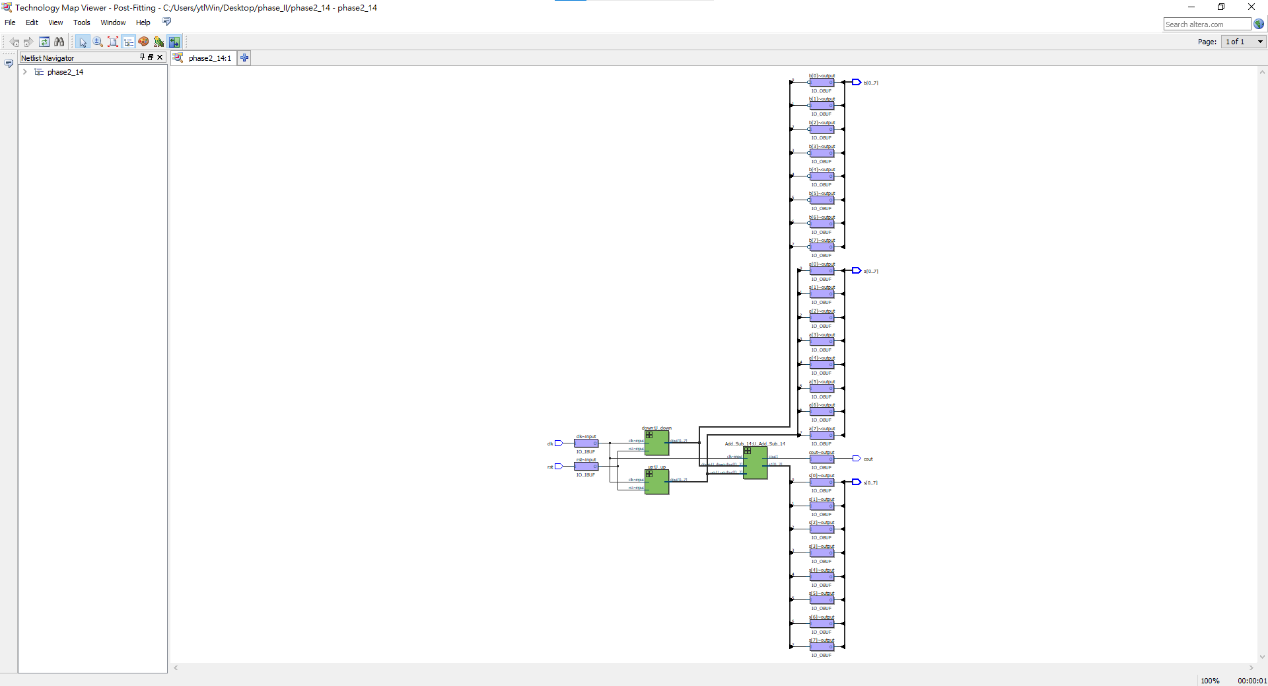
* 減法



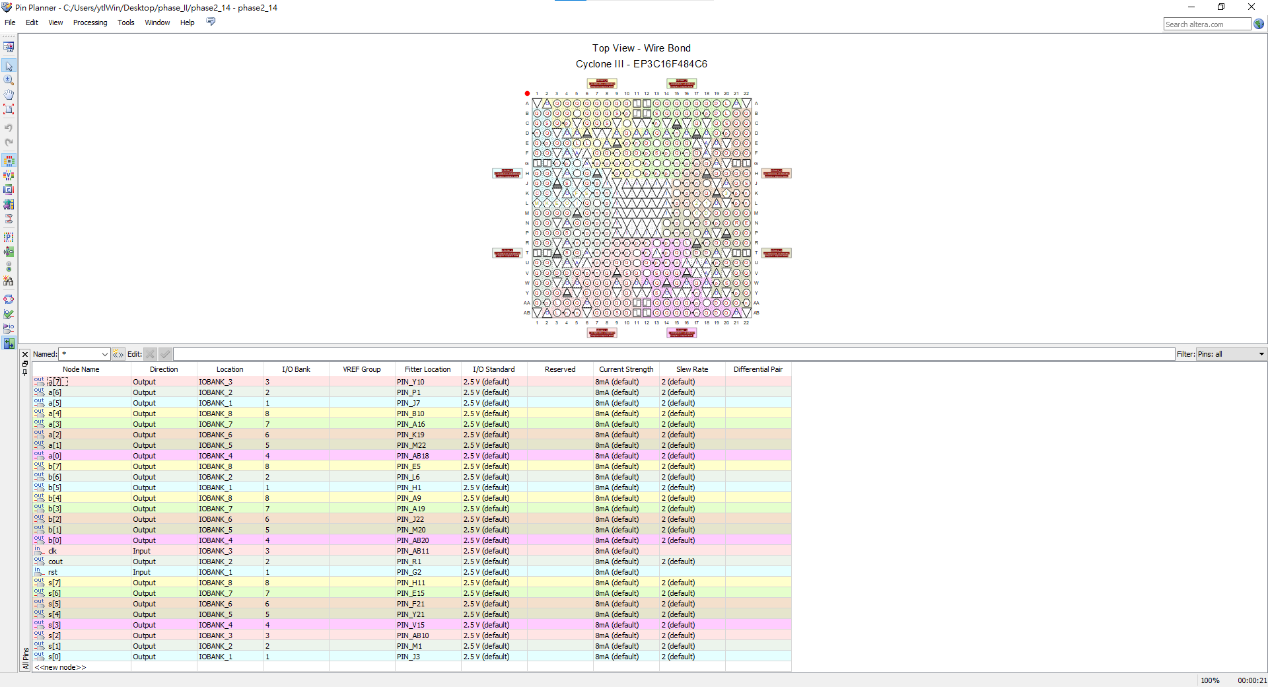
* RTL schematic



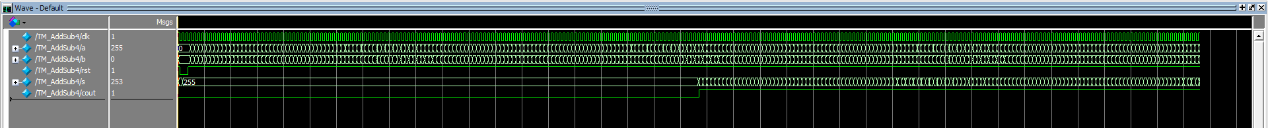
* Technology schematic



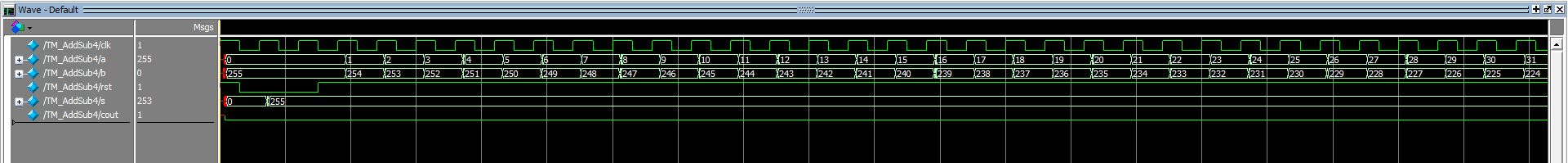
* Pin assignment



* Post-Simulation waveform



* 加法(timing delay)



* 減法(timing delay)

