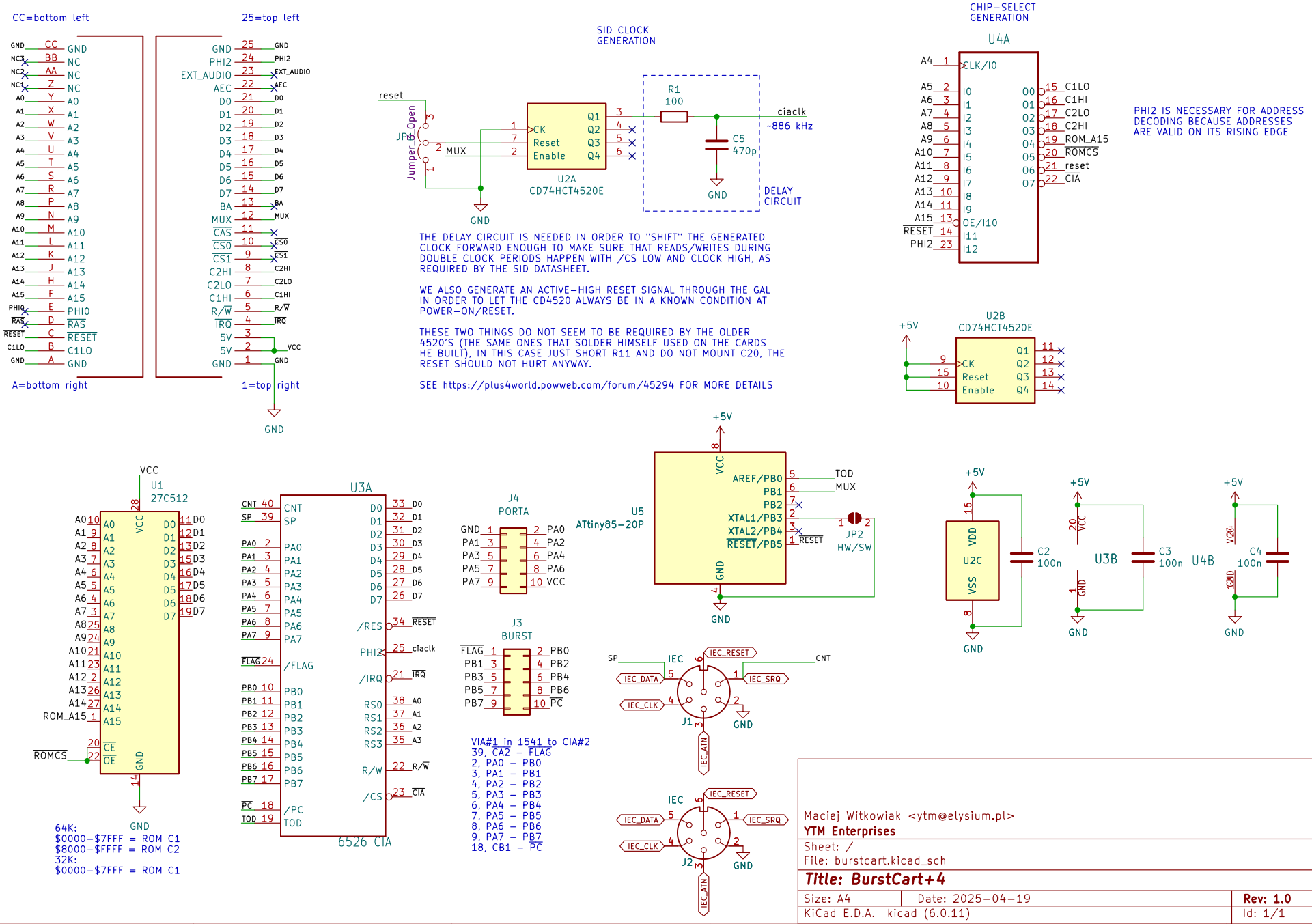
CC=bottom left
25=top left
A=bottom right
1=top right
SID CLOCK GENERATION
reset
JP3
Jumper_3_Open
MUX
U2A
CD74HCT4520E
R1
100
C5
470p
ciaclk
~886 kHz
DELAY CIRCUIT
GND
THE DELAY CIRCUIT IS NEEDED IN ORDER TO "SHIFT" THE GENERATED CLOCK FORWARD ENOUGH TO MAKE SURE THAT READS/WRITES DURING DOUBLE CLOCK PERIODS HAPPEN WITH /CS LOW AND CLOCK HIGH, AS REQUIRED BY THE SID DATASHEET.
WE ALSO GENERATE AN ACTIVE-HIGH RESET SIGNAL THROUGH THE GAL IN ORDER TO LET THE CD4520 ALWAYS BE IN A KNOWN CONDITION AT POWER-ON/RESET.
THESE TWO THINGS DO NOT SEEM TO BE REQUIRED BY THE OLDER 4520'S (THE SAME ONES THAT SOLDER HIMSELF USED ON THE CARDS HE BUILT), IN THIS CASE JUST SHORT R11 AND DO NOT MOUNT C20, THE RESET SHOULD NOT HURT ANYWAY.
SEE https://plus4world.powweb.com/forum/45294 FOR MORE DETAILS
CHIP-SELECT GENERATION
U4A
PHI2 IS NECESSARY FOR ADDRESS DECODING BECAUSE ADDRESSES ARE VALID ON ITS RISING EDGE
U2B
CD74HCT4520E
VCC
U1
27C512
ROMCS
64K:
$0000-$7FFF = ROM C1
$8000-$FFFF = ROM C2
32K:
$0000-$7FFF = ROM C1
U3A
6526 CIA
J4
PORTA
J3
BURST
VIA#1 in 1541 to CIA#2
39, CA2 - FLAG
2, PA0 - PB0
3, PA1 - PB1
4, PA2 - PB2
5, PA3 - PB3
6, PA4 - PB4
7, PA5 - PB5
8, PA6 - PB6
9, PA7 - PB7
18, CB1 - PC
U5
ATtiny85-20P
TOD
MUX
JP2
HW/SW
IEC
J1
J2
U2C
U3B
U4B
C2
100n
C3
100n
C4
100n
Maciej Witkowiak <ytm@elysium.pl>
YTM Enterprises
Sheet: /
File: burstcart.kicad_sch
Title: BurstCart+4
Size: A4
Date: 2025-04-19
Rev: 1.0
KiCad E.D.A. kicad (6.0.11)
Id: 1/1