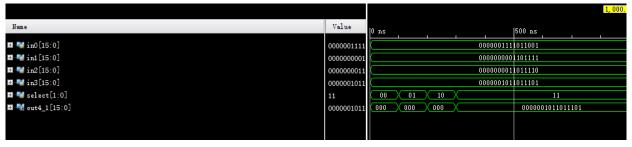
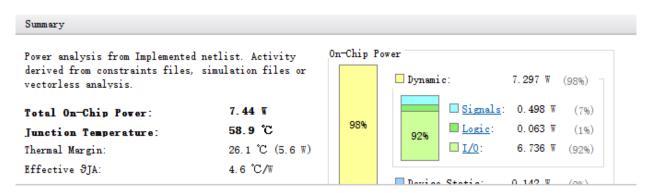
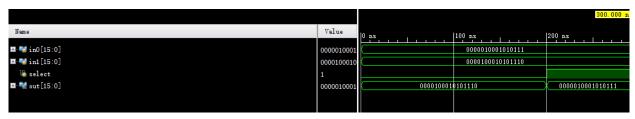
1. 四选一多路选择器 (four_to1)与二选一多路选择器(two_to1)的波形仿真以及资源 消耗对比



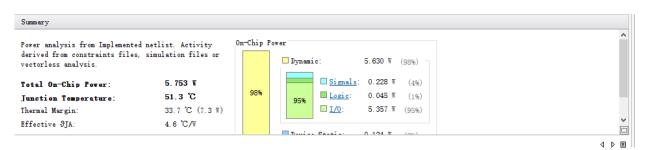
四选一多路选择器仿真



四选一多路选择器资源消耗

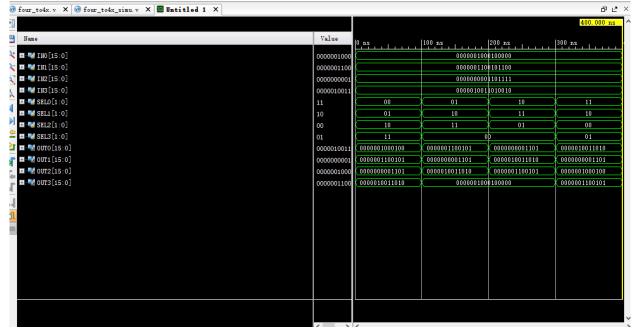


二选一多路选择器波形仿真

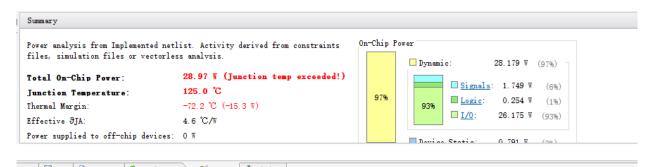


二选一多路选择器资源消耗

2. 4x4 路交叉开关 (four_to4x)与2x2路交叉开关(two_to2)的波形仿真以及资源消耗对比



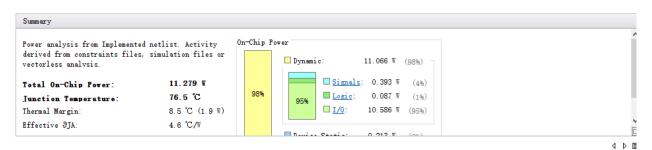
4X4路交叉开关波形仿真



4X4路交叉开关资源消耗

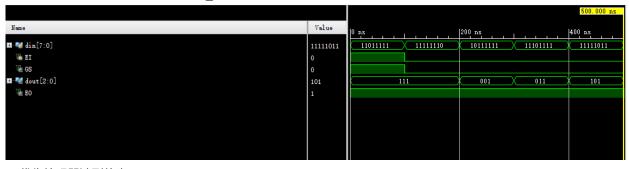


2X2路交叉开关波形仿真

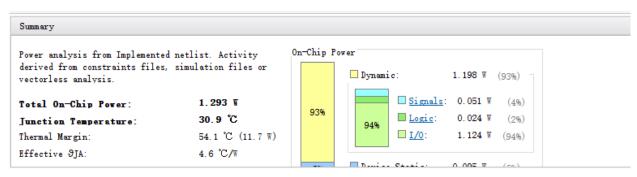


2X2路交叉开关资源消耗

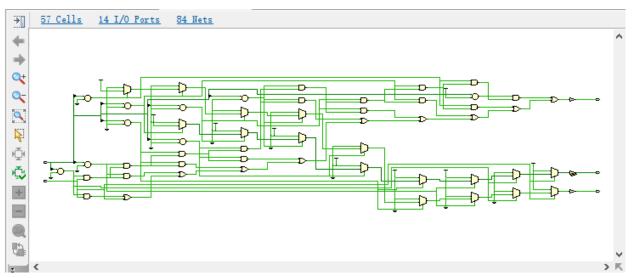
3. 83优先编码器 (Pri_Encoder)



83优先编码器波形仿真



83优先编码器资源消耗



83优先编码器原理图

4. 3-8译码器(decoder_38)与4-16译码器(decoder_416)

									1, 000	000 ns
Name	Value	0 ns				500 ns				
□ data_in[2:0] large enable	111 1	000	001	010	011	100	101	X 110	X	111
□-¶ data_out[7:0]	10000000	00000001	000	000	000	000	001	X 010	100	00000

3-8译码器波形仿真

Summary

Power analysis from Implemented netlist. Activity derived from constraints files, simulation files or vectorless analysis.

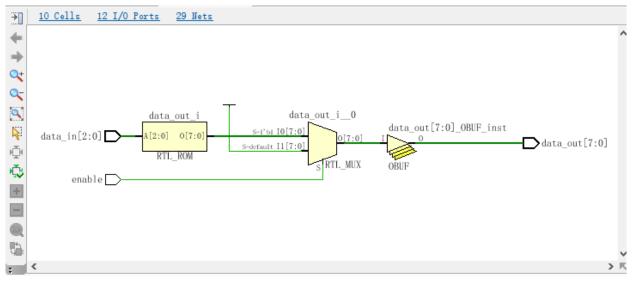
Total On-Chip Power: 2.394 W Junction Temperature: 35.9 °C

Thermal Margin: 49.1 °C (10.6 W)

Effective 9JA: 4.6 °C/W

96% Dynamic: 2.294 W (96%) Signals: 0.044 W (2%) Logic: 0.023 W (1%) 1/0: 2.227 W (97%)

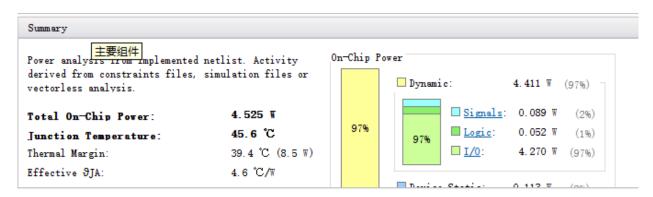
3-8译码器资源消耗



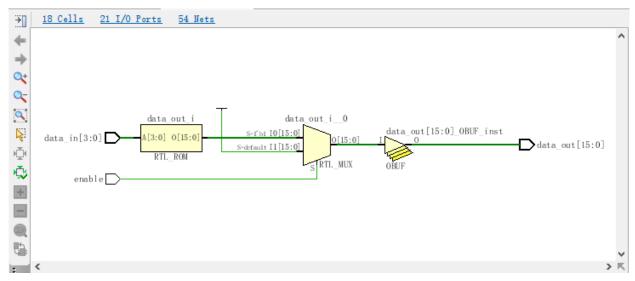
3-8译码器原理



4-16译码器波形仿真



4-16译码器资源消耗



4-16译码器原理图

5. 4位加法器 (add4)与8位加法器(add8)输出延迟对比



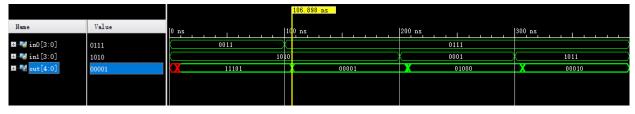
4位加法器延迟7.234ns左右



8位加法器延迟7.883ns左右

6. 4位补码加法器 (comp_add4) 8位补码加法器 (comp_add8)

在当两个输入信号的和大于7或小于-8时计算结果会出错,



7. 带流水线的加法器, 一级 (pipadd8 1), 二级 (pipadd8 2)

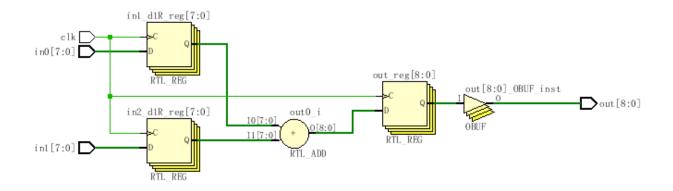
1.不改变流水线的级数,把加法器的输入信号改成8比特位宽,编译,波形仿真,和不带流水线的情况对比一下,你有什么结论?

2.在8比特输入位宽的情况下,在输入上再添加一级流水线,观察编译和仿真的结果,你有什么结论?

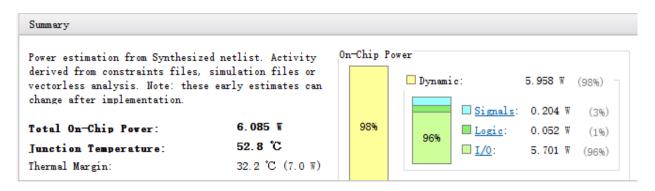


一级流水线波形仿真,毛刺变短,输出延迟增长至39.728ns

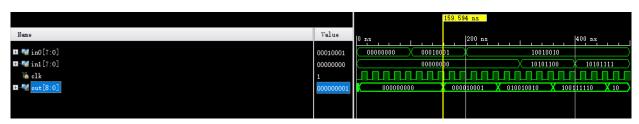
35 Cells 26 I/O Ports 60 Nets



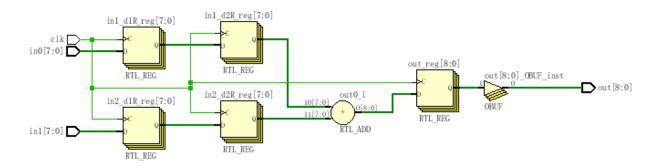
一级流水线原理图



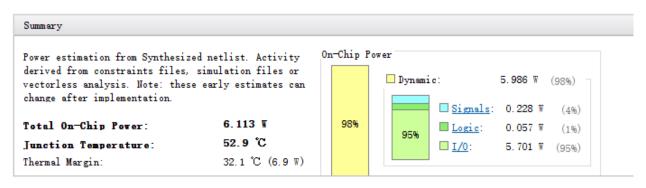
一级流水线功耗



二级流水线, 毛刺时间进一步缩短, 输出延迟进一步增大



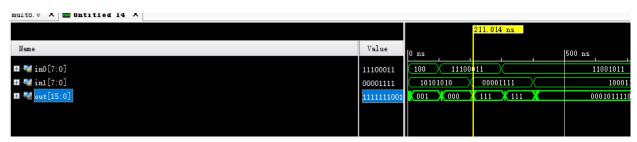
二级流水线原理图



二级流水线功耗

8. 乘法器

- 1.改变乘法器的输入位宽为8比特,编译,波形仿真,观察信号毛刺的时间长度。
- 2.选一款没有硬件乘法器的FPGA芯片 (例如Cyclone EP1C6) 对比8比特的乘法器和加法器两者编译之后的资源开销(Logic Cell的数目)
- 3.编写一个输入和输出都有D触发器的流水线乘法器代码,编译后波形仿真,观察组合逻辑 延迟和毛刺的时间,和不带流水线的情况下对比。



8位乘法器毛刺时长约4ns,输出延迟约11ns



```
Flow Status
                                    Successful = Sun Nov 11 00:07:22 2018
Quartus II Version
                                    9 0 Build 235 06/17/2009 SP 2 SJ Web Edition
Revision Name
Top-level Entity Name
                                    top
Family
                                    Cycline III
                                   E23C16F484C6
Device
Timing Models
                                    Final
                                   N/A
Met timing requirements
Total logic elements
                                   8 / 15,408 ( < 1 % )
    Total combinational functions 8 / 15,408 ( < 1 % )
                                   0 / 15.408 ( 0 % )
    Dedicated logic registers
Total registers
Total pins
                                   11 / 347 ( 3 % )
Total virtual pins
Total memory bits
                                   U / 516,096 ( U % )
Embedded Multiplier 9-bit elements 0 / 112 ( 0 % )
                                    0/4(0%)
Total PLLs
```

3-8译码器资源开销

```
Successful - Sun Nov 11 00:08:09 2018
Flow Status
Quartus II Version
                                   9.0 Build 235 06/17/2009 SP 2 SJ Web Edition
Revision Name
                                   top
Top-level Entity Name
                                   top
                                   Cyclone III
Family
Device
                                   EP3C16F484C6
Timing Models
                                   Final
Met timing requirements
                                  N/A
Total logic elements
                                   16 / 15,408 ( < 1 % )
   Total combinational functions 16 / 15,408 ( < 1 % )
   Dedicated logic registers
                                   0 / 15,408 ( 0 % )
Total registers
Total pins
                                   20 / 347 (6%)
Total virtual pins
Total memory bits
                                   0 / 516,096 ( 0 % )
Embedded Multiplier 9-bit elements 0 / 112 ( 0 % )
Total PLLs
                                   0/4(0%)
```

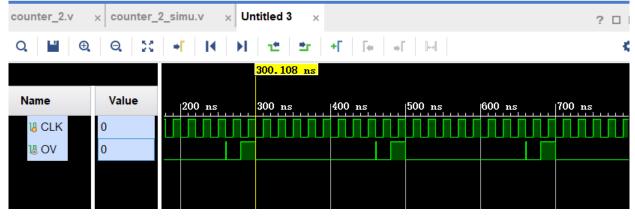
4-16译码器资源开销

9. 计数器

- 1.设计一个最简单的计数器 (counter_2),只有一个CLK输入和一个Overflow输出,当计数到最大值的时钟周期CLK输出1
- 2.设计复杂的计数器(counter_1),和本例相似,带有多种信号,其中同步清零CLR的优先级最高,使能EN次之,LOAD最低。



简单计数器 (counter)从0到7计数, 若到达7, 则回归0。

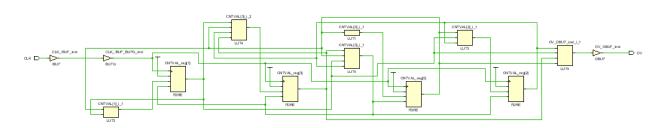


简单计数器 (counter_2), 每10次时钟下降沿输出为1, 毛刺市场为0.2ns,

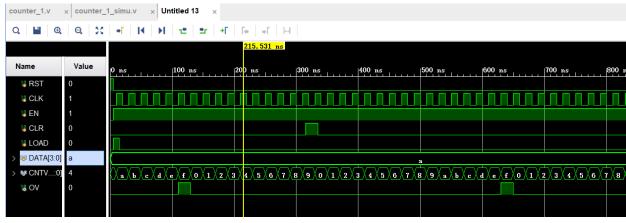
Summary



简单计数器 (counter_2)功耗

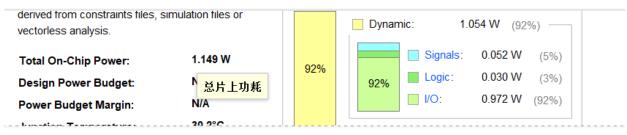


简单计数器 (counter_2)原理图

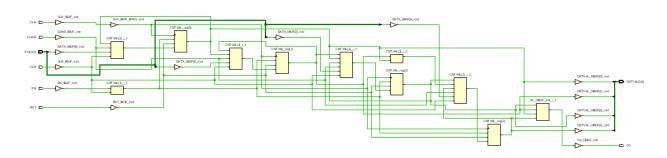


复杂计数器(counter_1)实现了clear, load等功能

Summary



复杂计数器功耗



复杂计数器原理图

10. 状态机(check_1011)

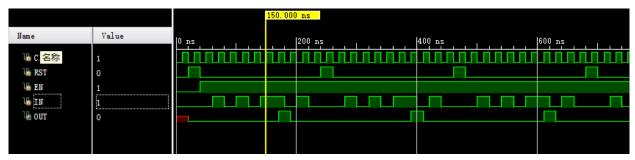
1.设计一个用于识别2进制序列"1011"的状态机

基本要求:

电路每个时钟周期输入1比特数据,当捕获到1011的时钟周期,电路输出1,否则输出0 使用序列101011010作为输出的测试序列

扩展要求:

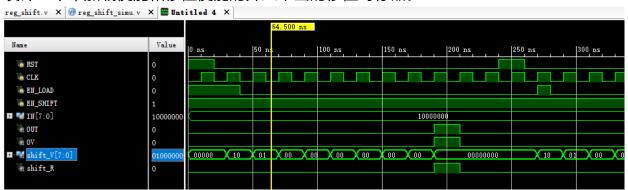
给你的电路添加输入使能端口,只有输入使能EN为1的时钟周期,才从输入的数据端口向内部获取1比特序列数据。



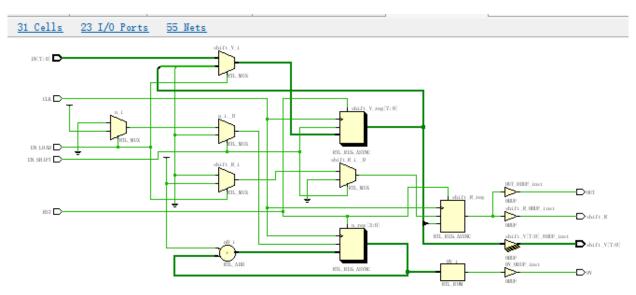
1011序列检测波形仿真

11. 移位寄存器(reg shift)

设计一个带加载使能和移位使能的并入串出的移位寄存器。



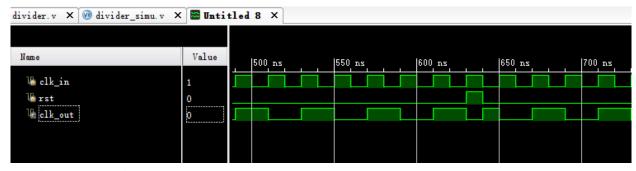
移位寄存器波形仿真



移位寄存器原理图

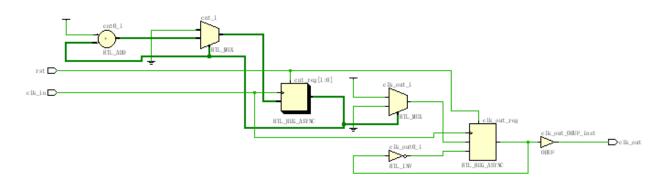
12. 时钟分频器

偶分频器($clk_divider_even$),假设为N分频,则计数到N/2 - 1,然后时钟翻转、计数清零,如此循环可以得到N(偶)分频。



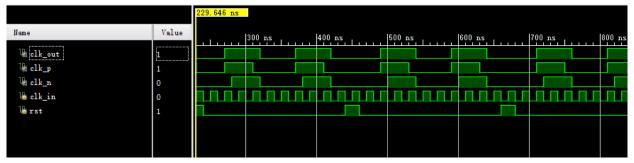
当偶分频器N=2波形仿真

8 Cells 3 I/O Ports 14 Nets

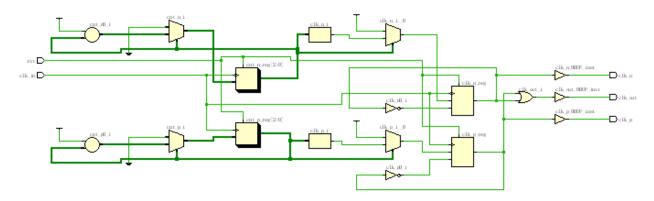


偶分频器原理图

奇分频器(clk_divider_odd),分别用上升沿计数到 (N-1)/2,再计数到N-1;用下降沿计数到 (N-1)/2,再计数到N-1,得到两个波形,然后把它们相或即可得N分频。



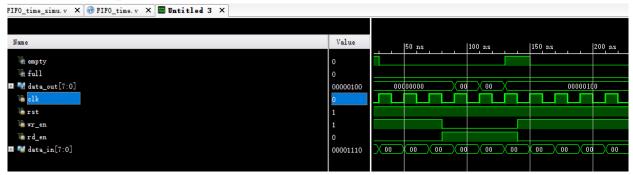
奇分频器N=5波形仿真



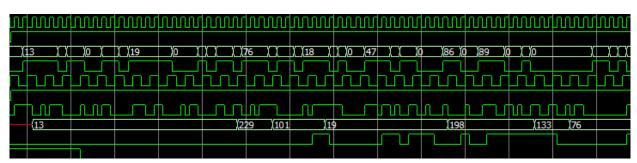
奇分频器原理图

13. FIFO

同步FIFO(FIFO_time)的实现



同步FIFO波形仿真



异步FIFO波形仿真