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Introduction to Mainframe Hardware



Agenda

- WHO uses Mainframes? And Why?
- WHY the Mainframe delivers
- ARCHITECTURE & Hardware Platform
- HIGHLIGHTS of zEC12
- zEC12 Book Concept
- zEC12 Processor Unit Design
- zEC12 Memory
- zEC12 Connectivity
- zEC12 RAS
- BACKUP Slides



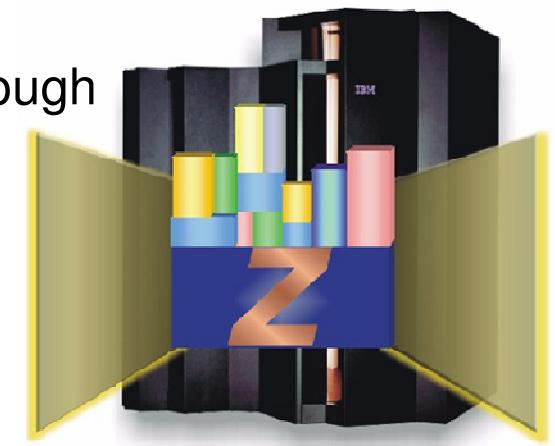
Definition of Mainframe

The Mainframe is a computer system designed to continuously run very large, mixed workloads at high levels of utilization, meeting user-defined service level objectives.

A Mainframe is what businesses use to host their commercial databases, transaction servers, and applications that require a greater degree of security and availability than is commonly found on smaller-scale machines.

What is a Mainframe?

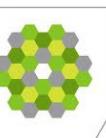
- A *style* of operation, applications, and operating system facilities.
- Computers that can support thousands of applications and input/output devices to simultaneously serve thousands of users.
- A mainframe is the central data repository, or *hub*, in a corporation's data processing center, linked to users through less powerful devices such as workstations, terminals or media devices.
- Can run multiple, but isolated operating systems concurrently.
- Centralized control of resources.
- Optimized for I/O in all business-related data processing applications supporting high speed networking and terabytes of disk storage.



WHO uses Mainframes? And Why?



Sample of Customers Large and Small from Around the World

BANKS	OTHER FINANCIAL INST.	RETAILERS	HEALTHCARE	UTILITIES / ENERGY
 Banco Itau  BARCLAYS  Bank of NZ  Bank of Montreal  [Peru] BCP  Bank of China  Central Bank of Russia  FNB First National Bank Namibia  [India] HDFC BANK  Industrial Bank of Korea  Philippines Savings Bank  [Germany] Postbank  [Vietnam] VietinBank	DTCC <i>The Depository Trust & Clearing Corporation</i> Allianz  PROVINZIAL <i>Die Versicherung der Sparkassen</i> GOVERNMENTS  [Brazil]  [Kazakhstan]  [USA] Land Registry 	  <i>HIER BIN ICH MENSCH HIER KAUF ICH EIN</i> TRANSPORTATION   [Belarusian Railways]   Russian Railways	  	  [Slovenia]
			HOSTING PROVIDERS  BRZ Deutschland Bauinformationstechnologie   EFIS FINANCIAL SOLUTIONS  	OTHERS  [Gaming] [Brazil]  Federal Services for Hydrometeorology and Environmental Monitoring [Russian Hydrometeorological Research Institute]  [Manufacturer/USA]

Mainframe is the platform of choice for the top 25 global banks

- Based on asset size, 96 out of the top 100 worldwide banks use System z.¹
 - ✓ 50 out of the top 50 worldwide banks use System z.
 - ✓ 72 out of the top 75 worldwide banks use System z.
- For the latest generation of Mainframe:
 - ✓ \$1.5 billion in R&D investment for z196
 - ✓ 5,000+ IBMers worked more than three years, 31 million hours, 24-hour development process across 18 IBM labs worldwide.
 - ✓ More than 40 IBM Fellows and Distinguished Engineers led this effort.
 - ✓ The zEnterprise 196 is the world's fastest and most scalable enterprise system. ²

¹ Based on 'The Banker', System z install base and financial records

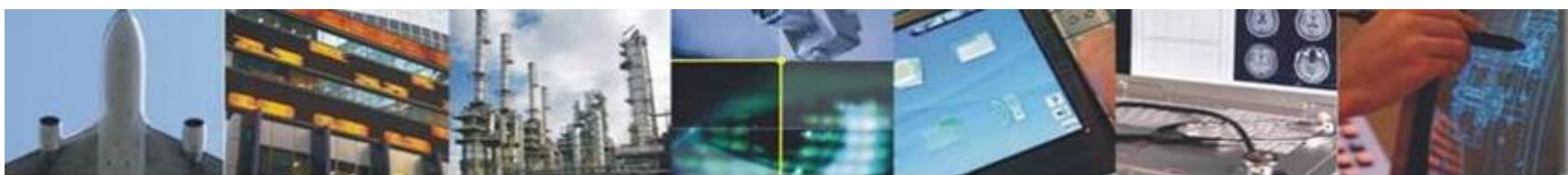
² Based on 5.2GHz core processor speed

Workloads That Customers Run on Mainframe

Banking	Insurance	Retail	Healthcare	Public Sector
Core Banking	<i>Internet Rate Quotes</i>	<i>On-line Catalog</i>	<i>Patient Care Systems</i>	<i>Electronic Tax Processing</i>
<i>Wholesale Banking – Payments</i>	<i>Policy Sales & Management (e.g. Life, Annuity, Auto)</i>	<i>Supply Chain Management</i>	<i>On-line Claims Submission & Payments</i>	<i>Web based Social Security</i>
<i>Customer Care & Insight</i>	<i>Claims Processing</i>	<i>Customer Analysis</i>		<i>Fee payments</i>

What is a workload?

The relationship between a **group** of applications and/or systems that are related across several business functions to satisfy one or more business processes.



Academic Initiative

- 1,067 Schools enrolled in the IBM System z Academic Initiative program, reaching students in 67 countries (more than half outside the US).
- Mainframe contests continue to draw high school, college, and university student participation around the world with 43,825 students from 32 countries.
- 3,246 students from 40 countries have taken the The IBM System z Mastery Test. This test is offered to students globally in 2011 at no cost.

<http://www-05.ibm.com/tr/industries/education/mainframe-index.html>

- IBM Academic Initiative System z resources (system access, course materials, education) are available globally for universities and colleges.
- Systemzjobs.com (Job board) is a no-fee service that connects students and experienced professionals seeking System z job opportunities with IBM System z clients, partners, and businesses.



WHY the Mainframe delivers



The Differentiation of Mainframe: Why the Mainframe Is Just Another Computer, but a Different Kind of Computer?

No other platform offers reliability, availability, scalability, **resiliency**, security, and **management** features comparable to Mainframe, including:

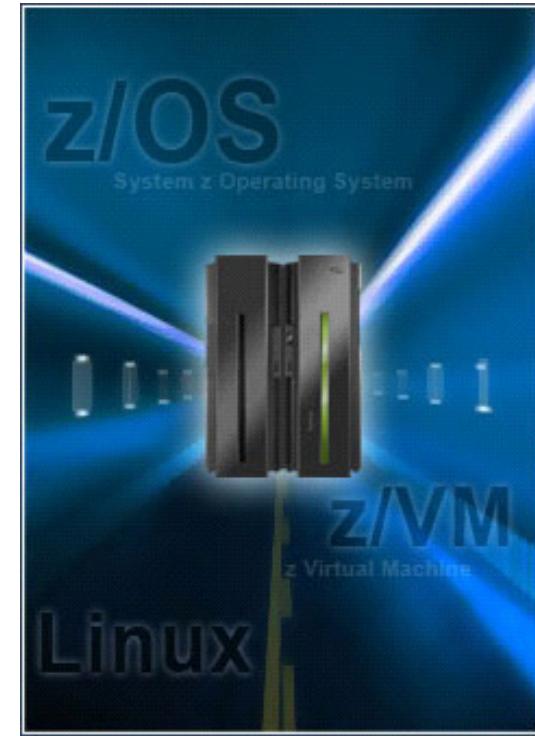
- High levels of application and data **availability**
- Solid **security** and **privacy**
- Massive horizontal and vertical **scalability**
- **Optimized** operating environment
- Advanced **virtualization** capabilities
- Intelligent **workload management**
- Utilization of **open** and **industry standards**
- Unmatched platform for **heritage (legacy) applications** and data
- **Specialty engines** that integrate with existing assets
- World-class **support**
- **Centralized** control
- Continuing **compatibility**



Mainframe Operating System Heritage

- **OS/360 -> OS/VS -> MVS -> MVS/SP -> MVS/XA -> MVS/ESA -> OS/390
-> z/OS**

z/OS, IBM's premier zSeries operating system, is a highly secure, scalable, high-performance enterprise operating system on which to build and deploy traditional and Java-enabled applications, providing a comprehensive and diverse application execution environment.



- **DOS/360 -> DOS/VS -> VSE/SP -> VSE/ESA -> z/VSE**

z/VSE enables proven, robust, and cost-effective solutions. z/VSE provides sturdy batch and industrial strength on-line transaction processing (CICS) capabilities. z/VSE can fit comfortably into a legacy of thrifty, dependable z/VSE solutions.

- **ACP -> TPF-> z/TPF**

TPF is the platform driving the business-critical systems for many of IBM's largest and most sophisticated users of online transaction processing - airlines, railroads, hotels, financial services, government, credit card and banking industries.

- **CP/67 -> VM/370 -> VM/SP -> VM/XA -> VM/ESA -> z/VM**

z/VM provides a highly flexible test and production environment for enterprises deploying the latest e-business solutions. z/VM helps enterprises meet their growing demands for multi-user server solutions with support for a broad range of operating systems.

Mainframe Software

- **Customer Information Control System (CICS®)** - a transaction processing environment that allows applications to share information and to satisfy customer requirements for information.
- **Information Management System Transaction Manager (IMS TM)** – a transaction processing environment and an application server
- **Information Management System Database Server (IMS DB)** - a database system that is capable of extremely high performance.
- **DB2** - a full, functional relational database that leverages all of the features of Mainframe and z/OS to provide high availability and high performance.
- **WebSphere Application Server (WAS)** – an application server that runs on z/OS, and provides true application portability between Mainframe and distributed systems



Maximizing Utilization of Resources

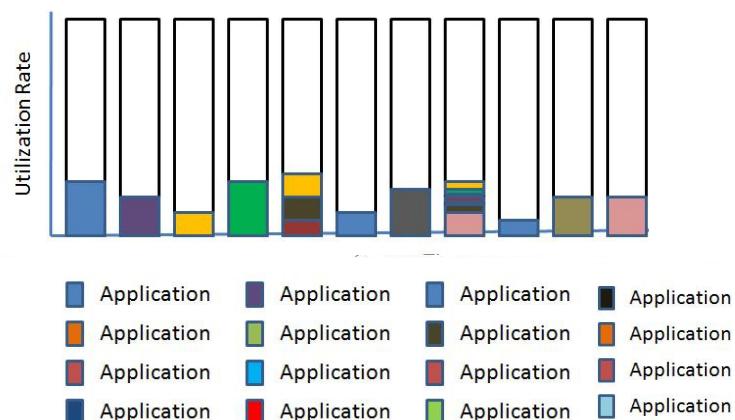
- Up to 100% server utilization compared to 10-20% distributed server utilization¹
- Shared everything infrastructure allows for maximum utilization of resources
 - CPU, Memory, Network, Adapters, Cryptography, Devices

Lowers power consumption for each work unit



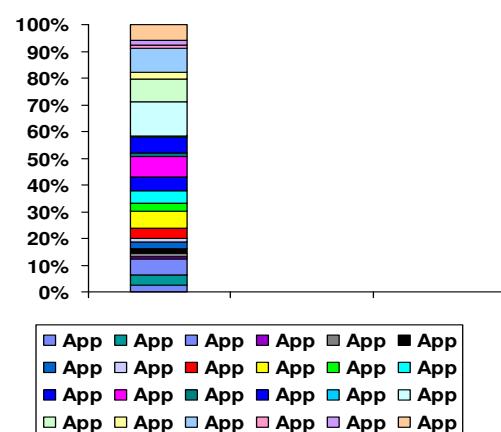
Customer savings

Underutilized distributed servers



Typically single application per server

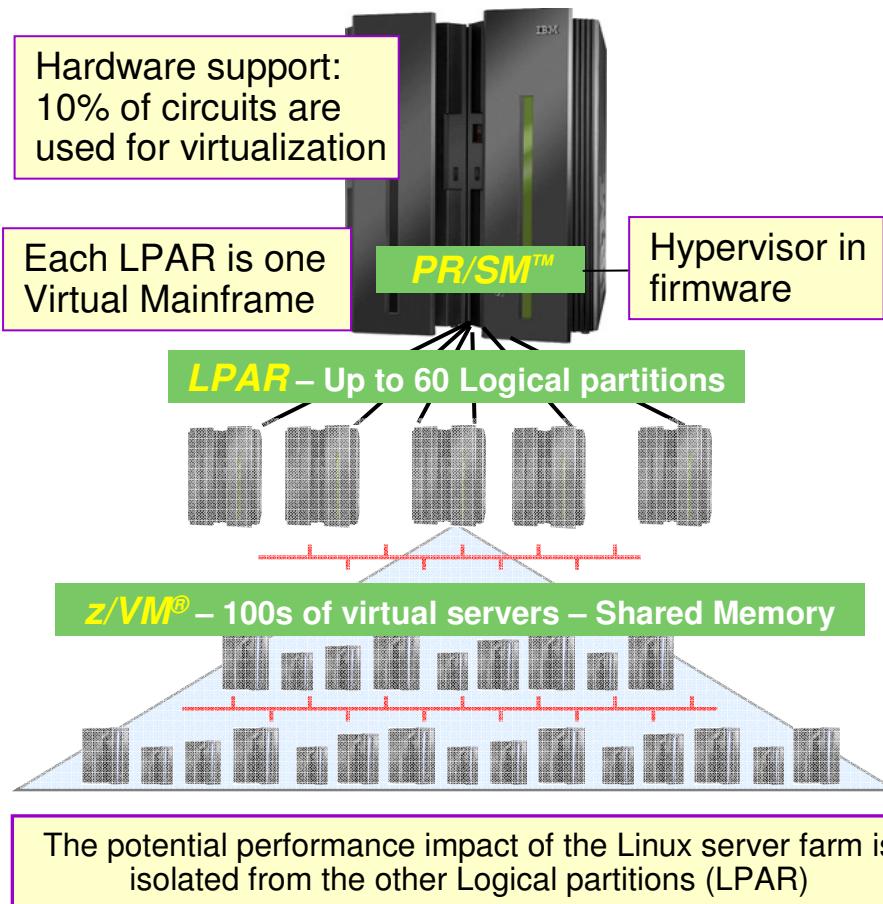
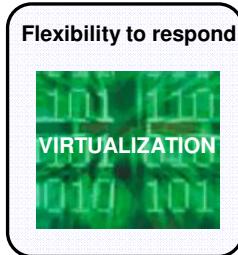
Up to 100% utilized Mainframe server



Multiple applications on one Mainframe server

Mainframe's Extreme Virtualization

– Built into the architecture not an “add on” feature



Mainframe

Deploy virtual servers **in seconds**

Highly **granular** resource sharing (<1%)

Add physical resources without taking system down, scale out to **1000s** of virtual servers

Do more with less: More virtual servers per core, Share more physical resources across servers

Extensive virtual server **life-cycle management**

Hardware-enforced isolation

Distributed Platforms

Limited per-core virtual server scalability

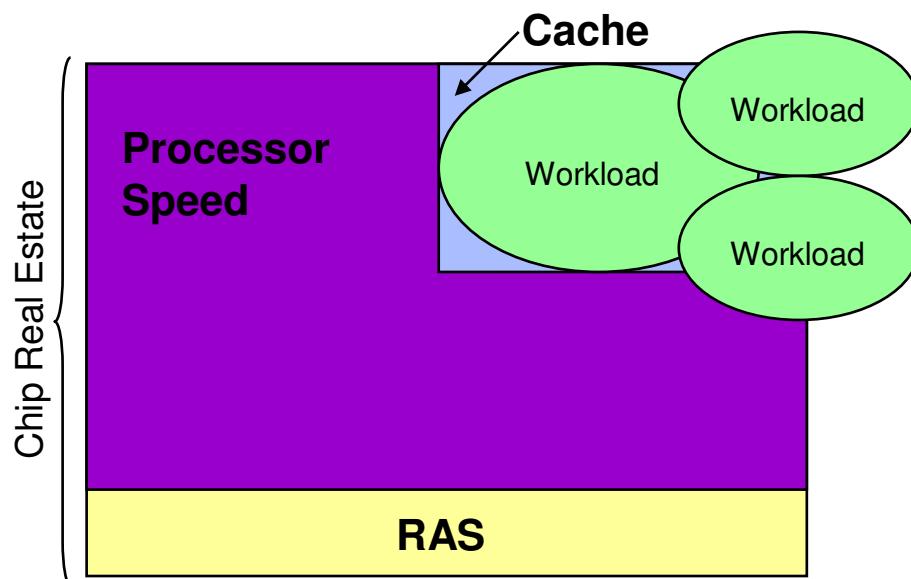
Physical server sprawl is needed to scale

Operational complexity increases as virtual server images grow

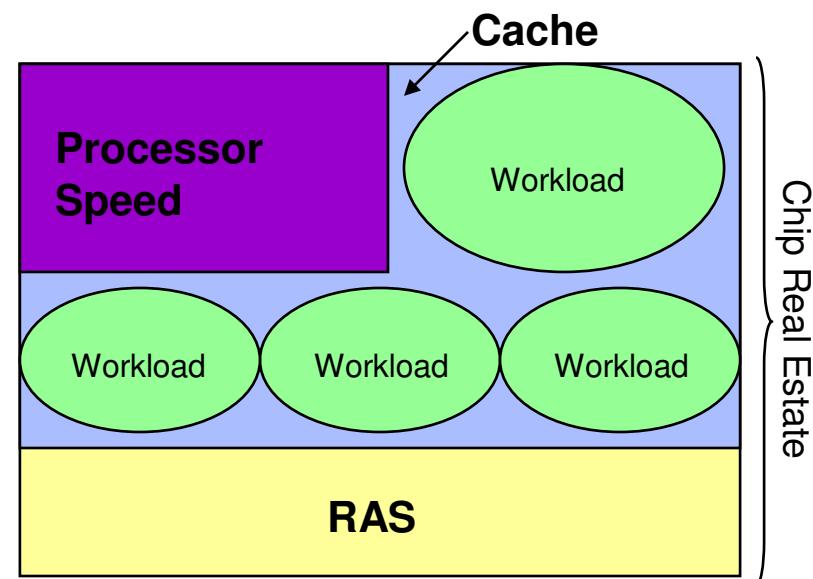
VMWare, Xen, Virtual Iron focus only on x86, not cross platform hardware management.

Chip Design Affects Virtualization Capabilities

Replicated Server Chip Design



Consolidated Server Chip Design



- Mixed workloads stress cache usage, requiring more context switches
- Working sets may be too large to fit in cache
- “Fast” processor speed is not fully realized due to cache misses

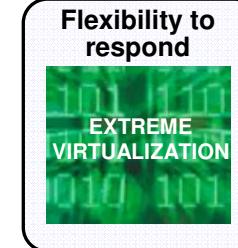
- System z cache is able to contain more working sets
- Processor speed is optimized by increased cache usage
- Additional RAS function is beneficial for mixed workloads

Note: System representations are not to scale, proportions may vary based on generation of chip and model

A Fully virtualized infrastructure enables optimization to maximize efficiency



Consolidate the workloads of thousands of distributed servers in a single system



Up to **80%** Reduction in energy consumption

Up to **90%** Reduction in Floor Space

Up to **90%** Reduction in SW License costs

Up to **70%** Reduction in total cost of ownership

Mainframe Security

Reducing risk – Protecting businesses

- Helping businesses:
- Protect from INTRUSION
 - z/OS and z/VM Integrity Statement
- Protect DATA
 - Built in encryption accelerators in every server
 - FIPS-140-20 Level 4 certified encryption co-processors for highly secure encryption
- Ensure PRIVACY
 - Access to all resources is controlled by an integrated central security manager
- Protect VIRTUAL SERVERS
 - The only servers with EAL5 Common Criteria Certification for partitioning
- Respond to COMPLIANCE REGULATIONS
 - Up to **70%** in security audit savings

*Up to **52%** lower security administrative costs.*



The Gold Standard for Security

Manage Risk with Mainframe Resiliency

Availability built in across the system



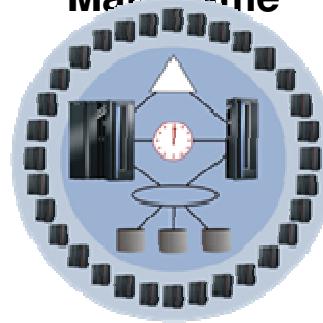
Designed to deliver continuous availability at the *application level*

Single Mainframe



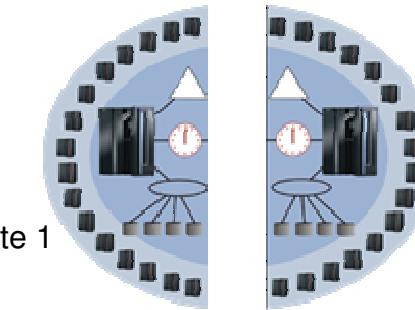
Where mean time
between failure is
measured in decades

Multiple Mainframe



Designed for
application availability
of 99.999%

Multiple Data Centers



Industry-leading
solution for
disaster recovery

- ✓ *Avoiding the cost of downtime*
- ✓ *Ensuring access to critical applications*
- ✓ *Maintaining productivity of users*
- ✓ *Open to clients 24/7*

Summary of the Benefits of Mainframe

Server Attributes	System z	Distributed System
Workload Management <ul style="list-style-type: none">Easily handles massive, risky, and undefined workload requirementsScales up and out to handle workloadReassigns resources to accommodate workload based on priority		
Server Reliability <ul style="list-style-type: none">Isolates failing components and seamlessly moves work to working componentsAutomatically activates extra components during busy timesContinues working when components are being repairedIncludes extremely reliable hardware combined with a bulletproof operating system, which enables simplified, reliable single-server deployment		
Server Security <ul style="list-style-type: none">Grows to handle workload within one secure boxAllows application of security policies and procedures in one place with no duplication requirementsProvides multi-level security, at both hardware and software levels, for true workload isolationThrough memory protection, ensures that control information is not corrupted by raw data from insecure sourcesRuns multiple environments in partitions on the hardwareDoes not dedicate applications to servers (applications run on one server)		
Server Performance <ul style="list-style-type: none">Achieves fast application performance by collocating business logic with information in one serverAvoids wasted processing time to package and encrypt data for network use		
Server Administration Costs <ul style="list-style-type: none">Does not require additional staff to apply patches and deploy upgrades and applications on numerous operating systemsDoes not require additional staff to monitor applications to determine where software failure or overload occursIncludes workload management capabilities and security features enable multiple workloads to be deployed in one fully utilized server, which reduces power consumption and cooling costs when compared to many under-utilized servers		

ARCHITECTURE & Hardware Platform



History

7th April 1964, Poughkeepsie NY: Announcement of the first general-purpose computers:

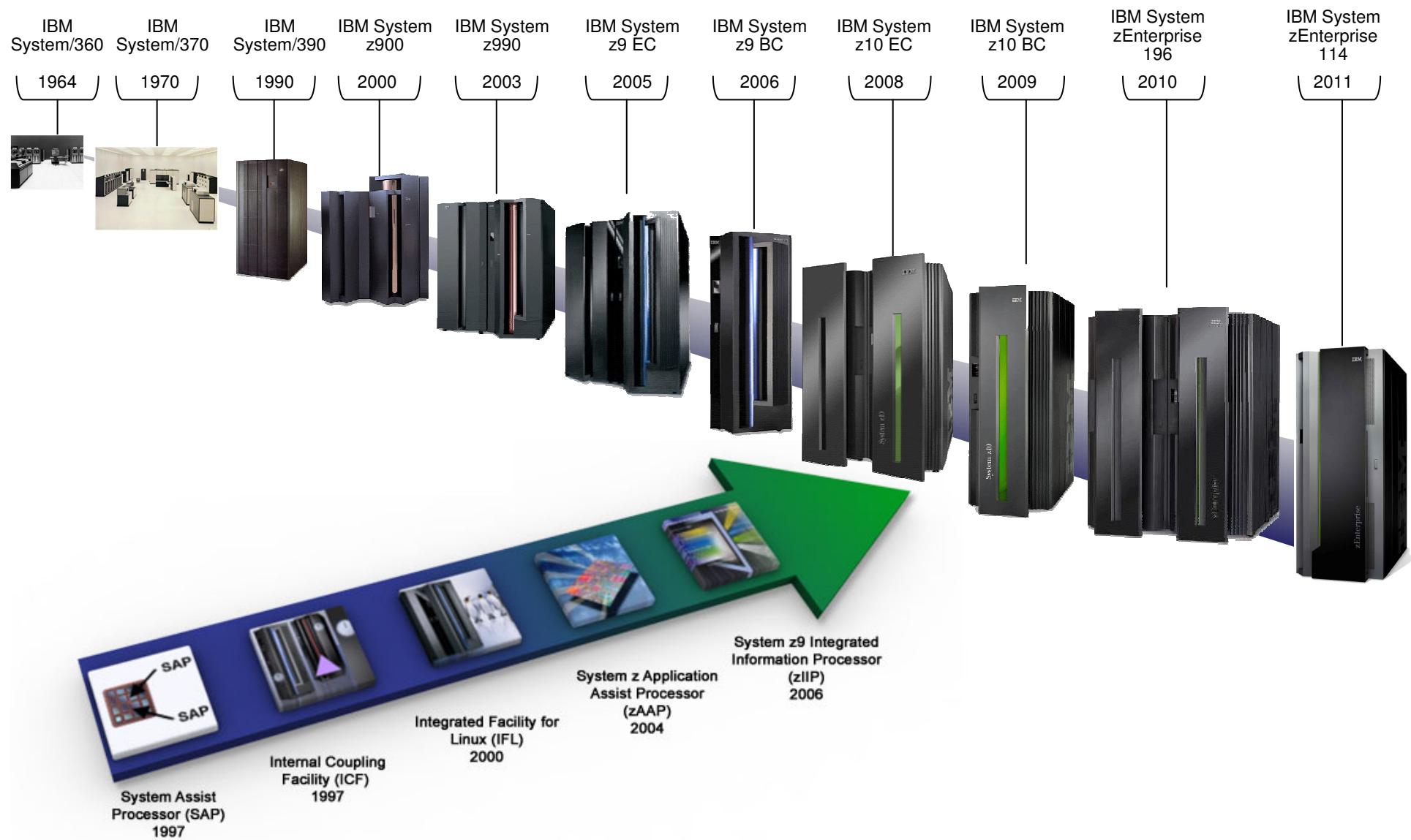
A new generation of electronic computing equipment was introduced today by International Business Machines Corporation. IBM Board Chairman Thomas J. Watson Jr. called the event the most important product announcement in the company's history.

The new equipment is known as the IBM System/360.

"System/360 represents a sharp departure from concepts of the past in designing and building computers. It is the product of an international effort in IBM's laboratories and plants and is the first time IBM has redesigned the basic internal architecture of its computers in a decade. The result will be more computer productivity at lower cost than ever before. This is the beginning of a new generation -- not only of computers -- but of their application in business, science and government." *

* from the April 1964 announcement press release

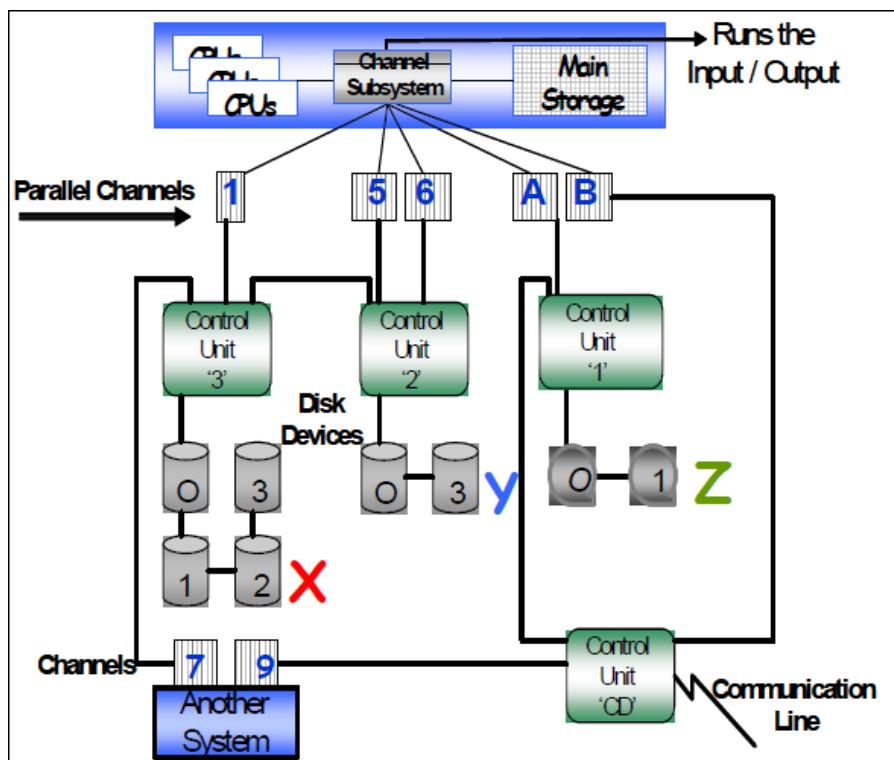
Evolution of the Mainframe



Conceptual diagram

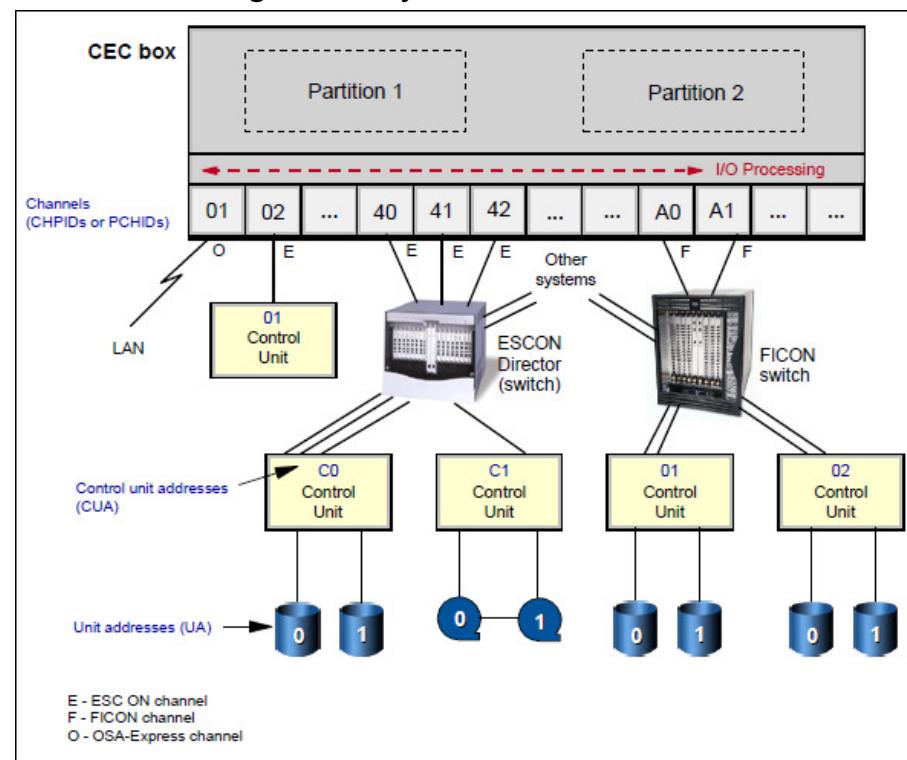
OLD S/360

The central processor box contains the processors, memory, 1 control circuits and interfaces for *channels*

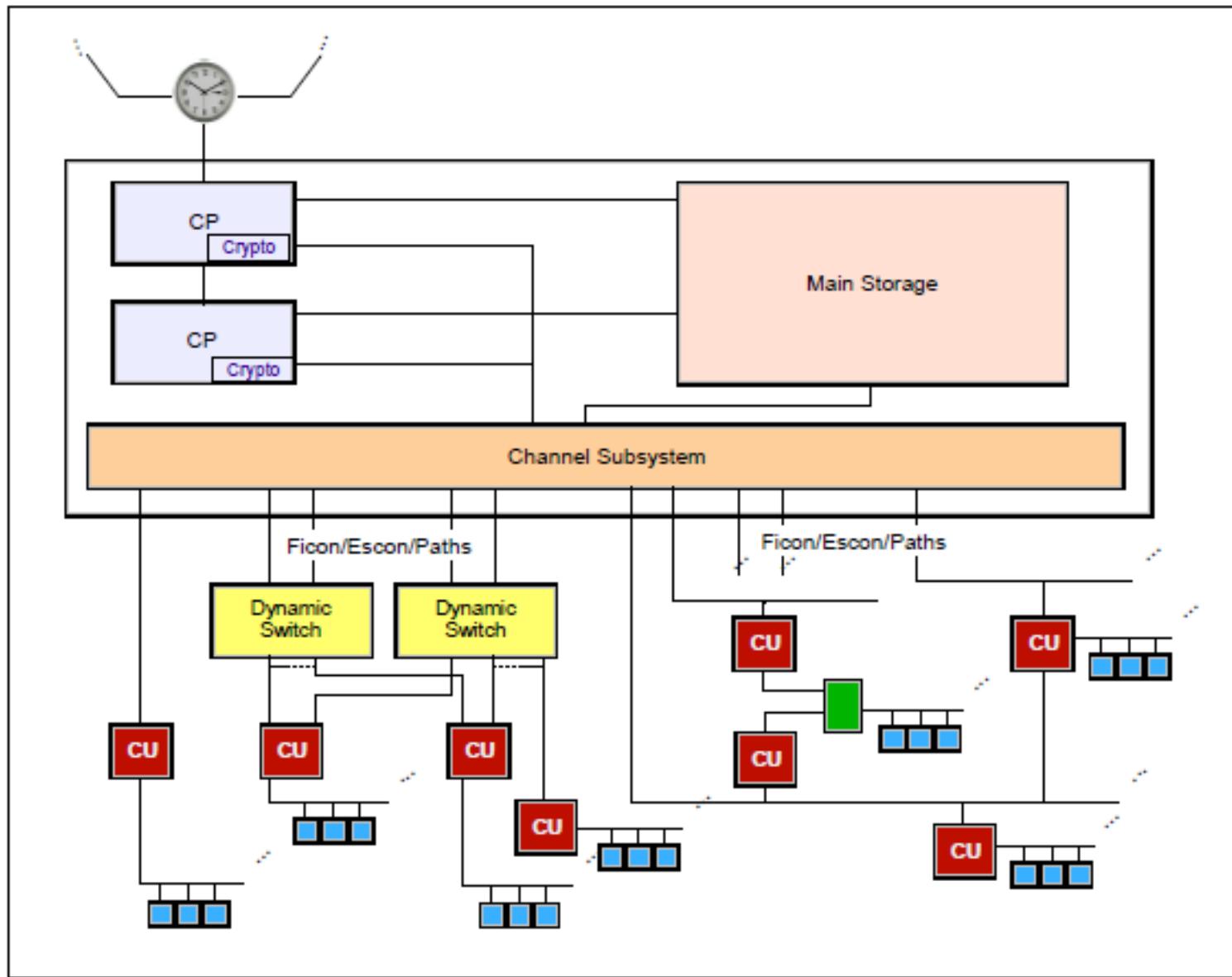


RECENT

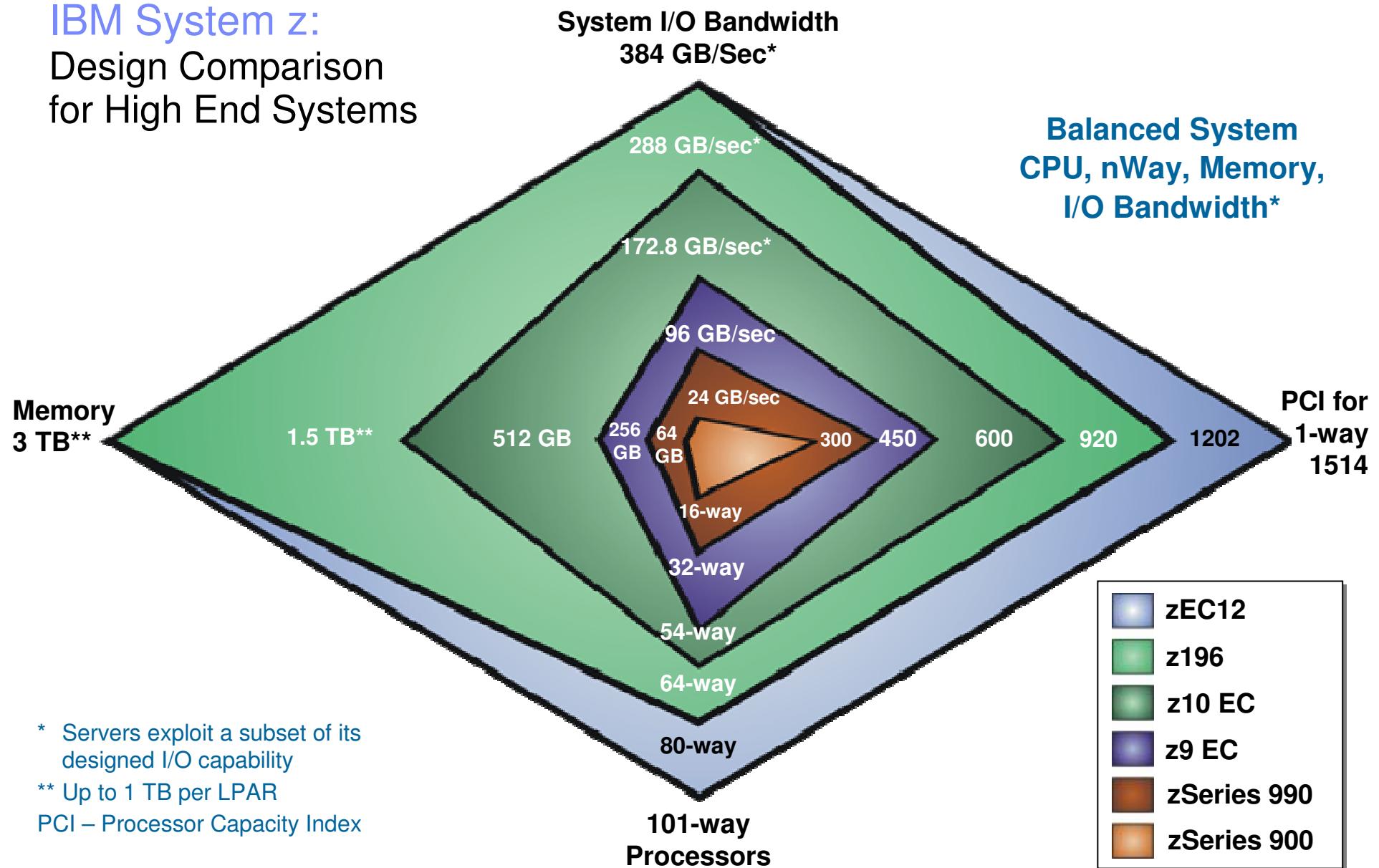
Current CPC designs are considerably more complex than the early S/360 design. This complexity includes many areas:
I/O connectivity and configuration
I/O operation
Partitioning of the system



Mainframe basic components



IBM System z: Design Comparison for High End Systems

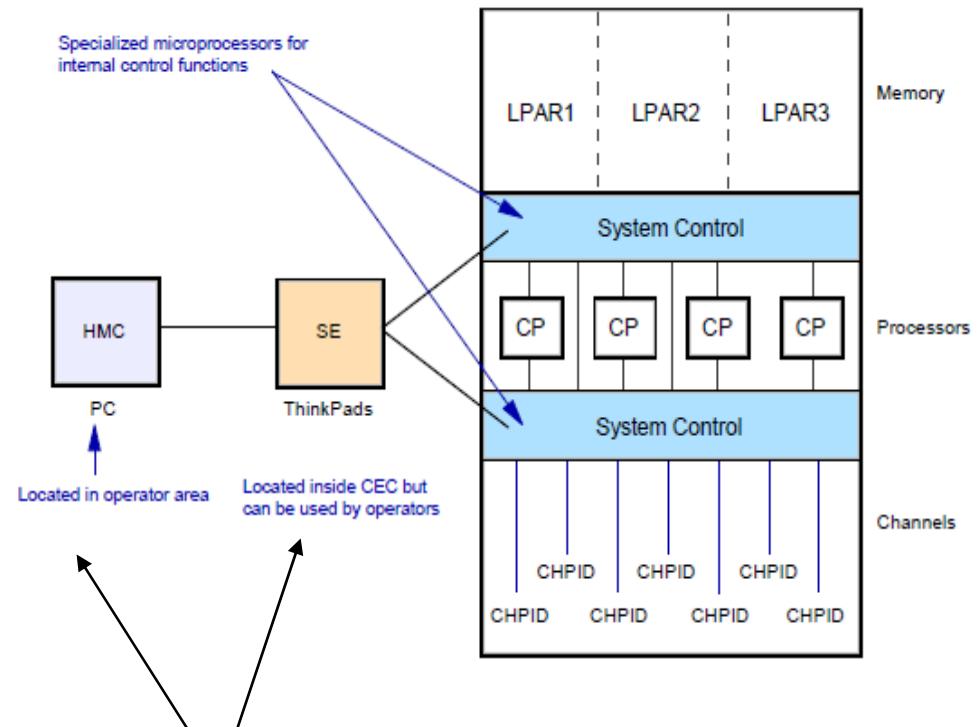


The virtualization concept

- The ability to **share everything** is based on one of the major concepts of the Mainframe. As it is commonly used in computing systems, virtualization refers to the **technique of hiding** the **physical characteristics** of the computing resources from users of those resources. For example, each operating system in a logical partition of the Mainframe platform thinks it has exclusive access to a real hardware image. The **actual resources are shared** with other logical partitions. The virtualization concept is **not an add-on** to the platform. z/Architecture contains many facilities in both the hardware and software that facilitate resource virtualization. All elements of Mainframe enable the virtualization concept.
- Virtualizing the Mainframe environment involves creating virtual systems (logical partitions and virtual machines), and assigning virtual resources, such as memory and I/O channels, to them. Resources can be **dynamically added or removed** from these logical partitions through operator commands.
- Dynamic logical partitioning and virtual machines increase **flexibility**, enabling selected system resources such as processors, memory, and I/O components to be added and deleted from partitions while they are actively in use. The ability to reconfigure logical partitions dynamically enables system administrators to dynamically move resources from one partition to another.
- Processor Resource/Systems Manager™ (**PR/SM™**) is a **hypervisor** integrated with all Mainframe elements that maps physical resources into virtual resources so that many logical partitions can **share the physical resources**.

PR/SM and logical partitions

- Processor Resource/Systems Manager is a feature that enables logical partitioning of the central processor complex (CEC). PR/SM provides **isolation** between partitions, which enables installations to separate users into distinct processing images, or to restrict access to certain workloads where different security clearances are required.
- Each logical partition operates as an independent server running its own operating environment. On the latest Mainframe models, you can define up to 60 logical partitions running z/VM®, z/OS, Linux on IBM Mainframe, z/TPF, and more operating systems. PR/SM enables each logical partition to have **dedicated or shared** processors and I/O channels, and dedicated memory (which you can dynamically reconfigure as needed).

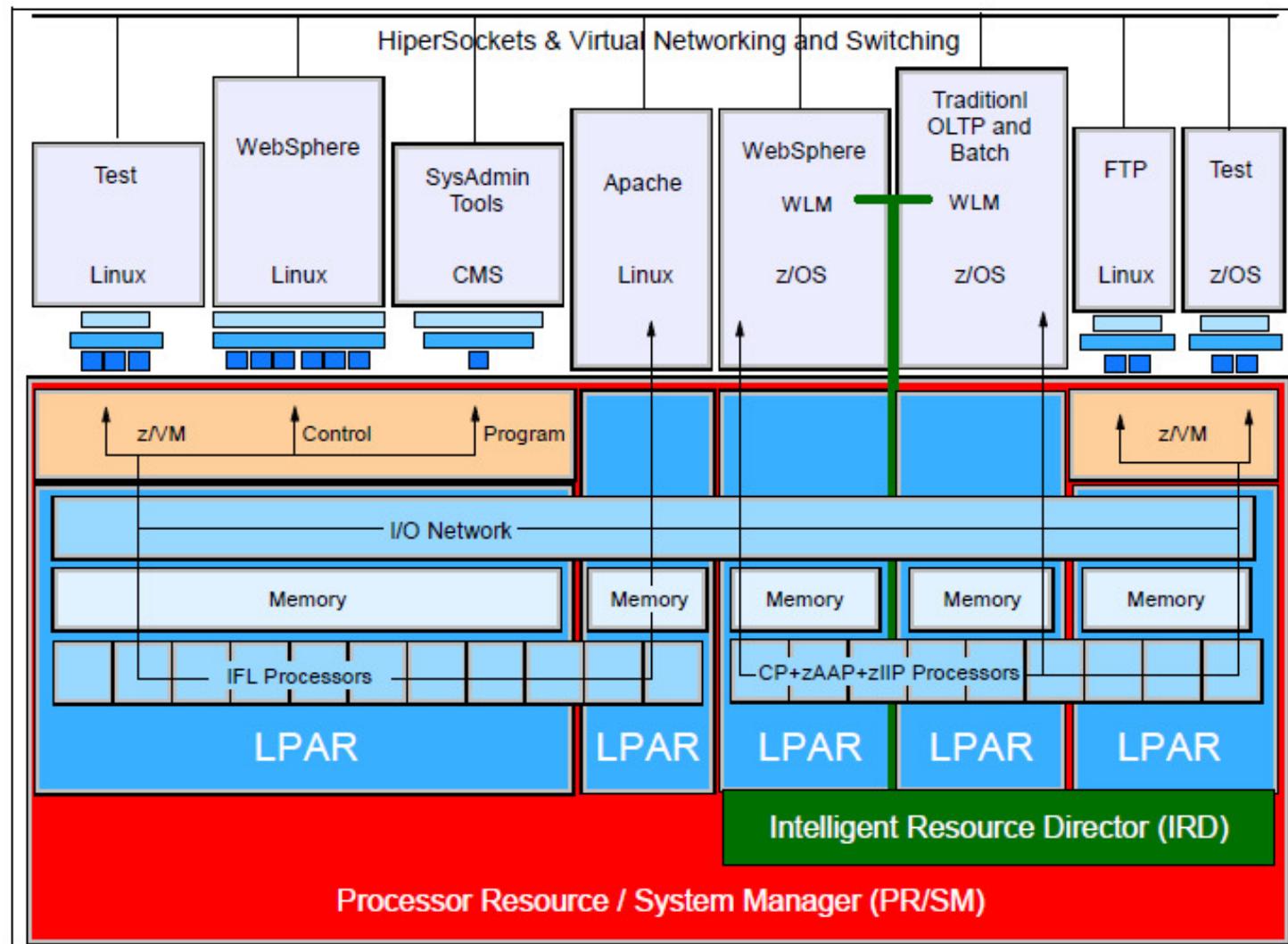


Either can be use to
configure the IOCDs

Support Elements (SEs)

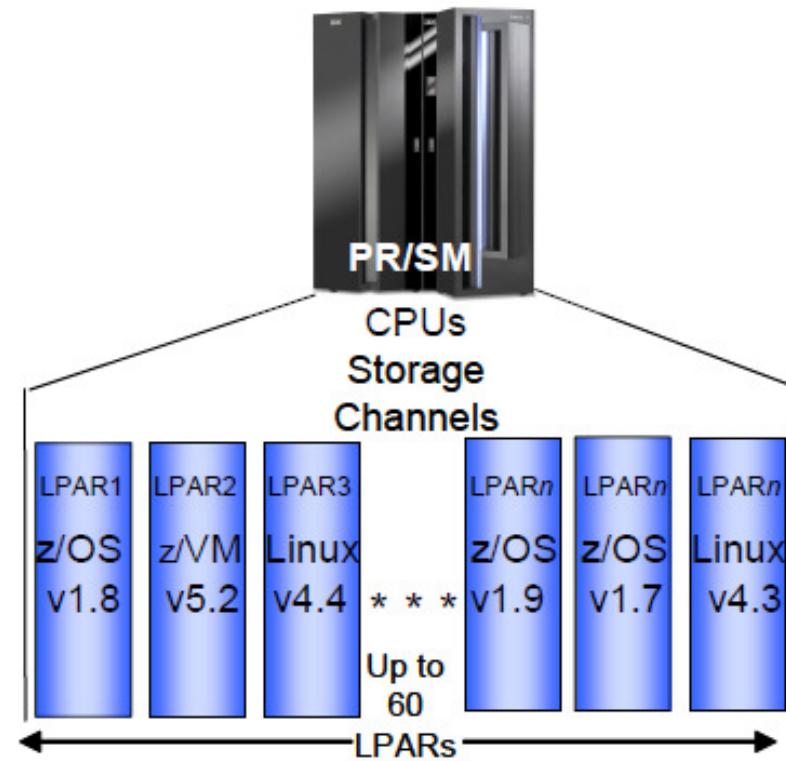


LPAR concept



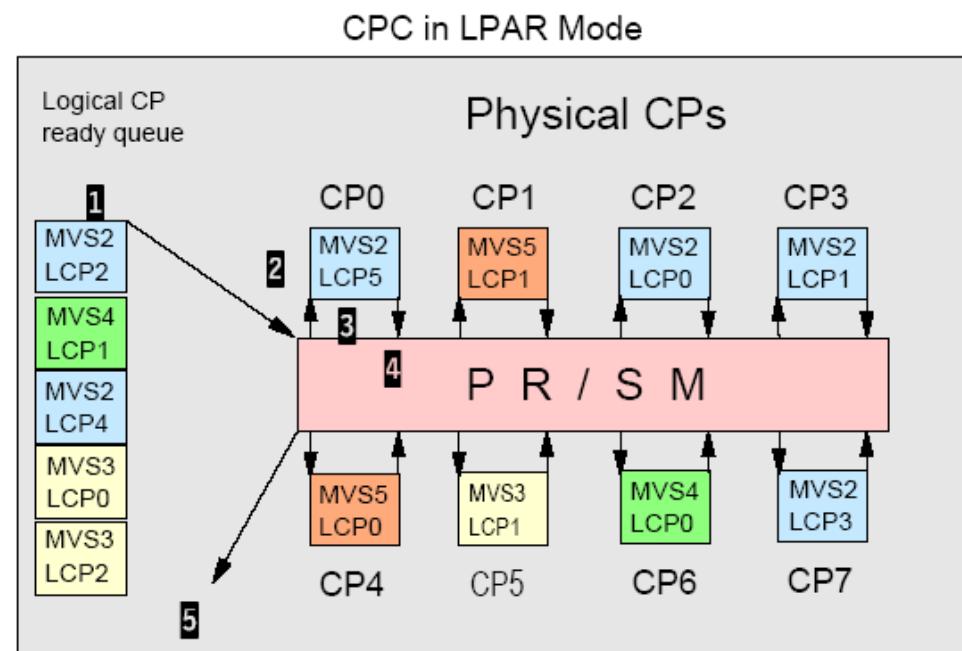
Logical Partitions (LPARs) or Servers

- A system programmer can assign different operating environments to each partition with isolation
- An LPAR can be assigned a number of dedicated or shared processors.
- Each LPAR can have different storage (CSTOR) assigned depending on workload requirements.
- The I/O channels (CHPIDs) are assigned either statically or dynamically as needed by server workload.
- Provides an opportunity to consolidate distributed environments to a centralized location



LPAR Logical Dispatching (Hypervisor)

- The next logical CP to be dispatched is chosen from the logical CP ready queue based on the **logical CP weight**.
- LPAR LIC **dispatches** the selected logical CP (LCP5 of MVS2 LP) on a physical CP in the CPC (CP0, in the visual).
- The z/OS dispatchable unit running on that logical processor (MVS2 logical CP5) begins to execute on physical CP0. It executes until its **time slice** (generally between 12.5 and 25 milliseconds) **expires**, or it enters a wait, or it is intercepted for some reason.
- In the visual, the logical CP keeps running until it uses all its time slice. At this point the logical CP5 **environment is saved** and control is passed back to LPAR LIC, which starts executing on physical CP0 again.
- LPAR LIC determines why the logical CP ended execution and **requeues** the logical CP accordingly. If it is ready with work, it is requeued on the logical CP ready queue and step 1 begins again.



HiperDispatch

- PR/SM and z/OS work in tandem to more efficiently use processor resources. HiperDispatch is a function that combines the dispatcher actions and the knowledge that PR/SM has about the topology of the server.
- Performance can be optimized by redispatching units of work to same processor group, keeping processes running near their cached instructions and data, and minimizing transfers of data ownership among processors/books.
- The nested topology is returned to z/OS by the Store System Information (STSI) 15.1.3 instruction, and HiperDispatch utilizes the information to concentrate logical processors around shared caches (L3 at PU chip level, and L4 at book level), and dynamically optimizes assignment of logical processors and units of work.
- z/OS dispatcher manages multiple queues, called affinity queues, with a target number of four processors per queue, which fits nicely into a single PU chip. These queues are used to assign work to as few logical processors as are needed for a given logical partition workload. So, even if the logical partition is defined with a large number of logical processors, HiperDispatch optimizes this number of processors nearest to the required capacity. The optimal number of processors to be used are kept within a book boundary where possible.

LPAR

Characteristics

- LPARs are the equivalent of a separate mainframe for most practical purposes
- Each LPAR runs its own operating system
- Devices can be shared across several LPARs
- Processors can be dedicated or shared
- When shared each LPAR is assigned a number of logical processors (up to the maximum number of physical processors)
- Each LPAR is independent

Summary

- System administrators assign:
 - Memory
 - Processors
 - CHPIDs either dedicated or shared
- This is done partly in the IOCDS and partly in a system profile on the Support Element (SE) in the CEC. This is normally updated through the HMC.
- Changing the system profile and IOCDS will usually require a power-on reset (POR) but some changes are dynamic
- A maximum of 60 LPARs can be defined in a z196 CPC

Terminology Overlap



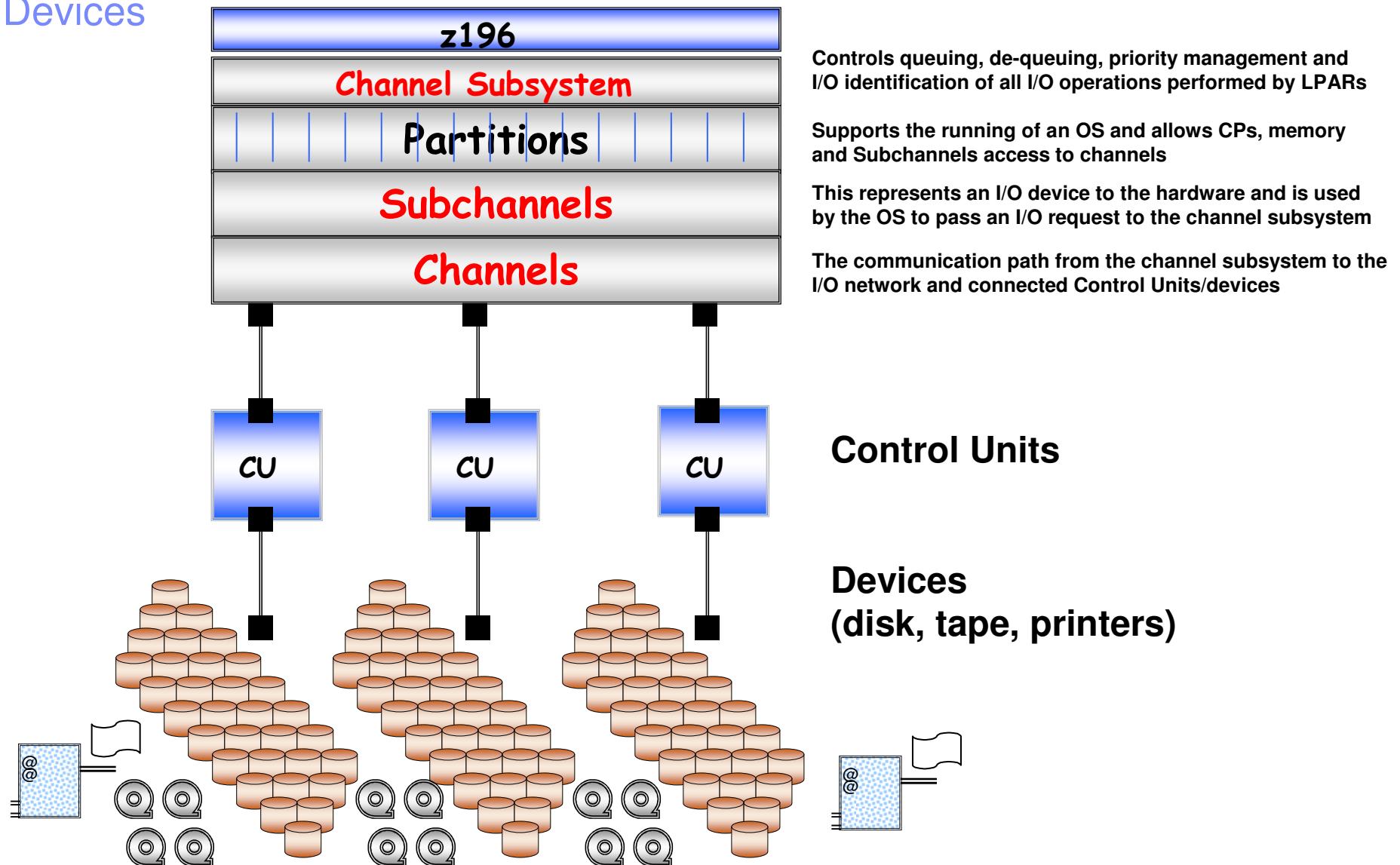
Note: LPAR may be referred to as an “image” or “server”

The channel subsystem

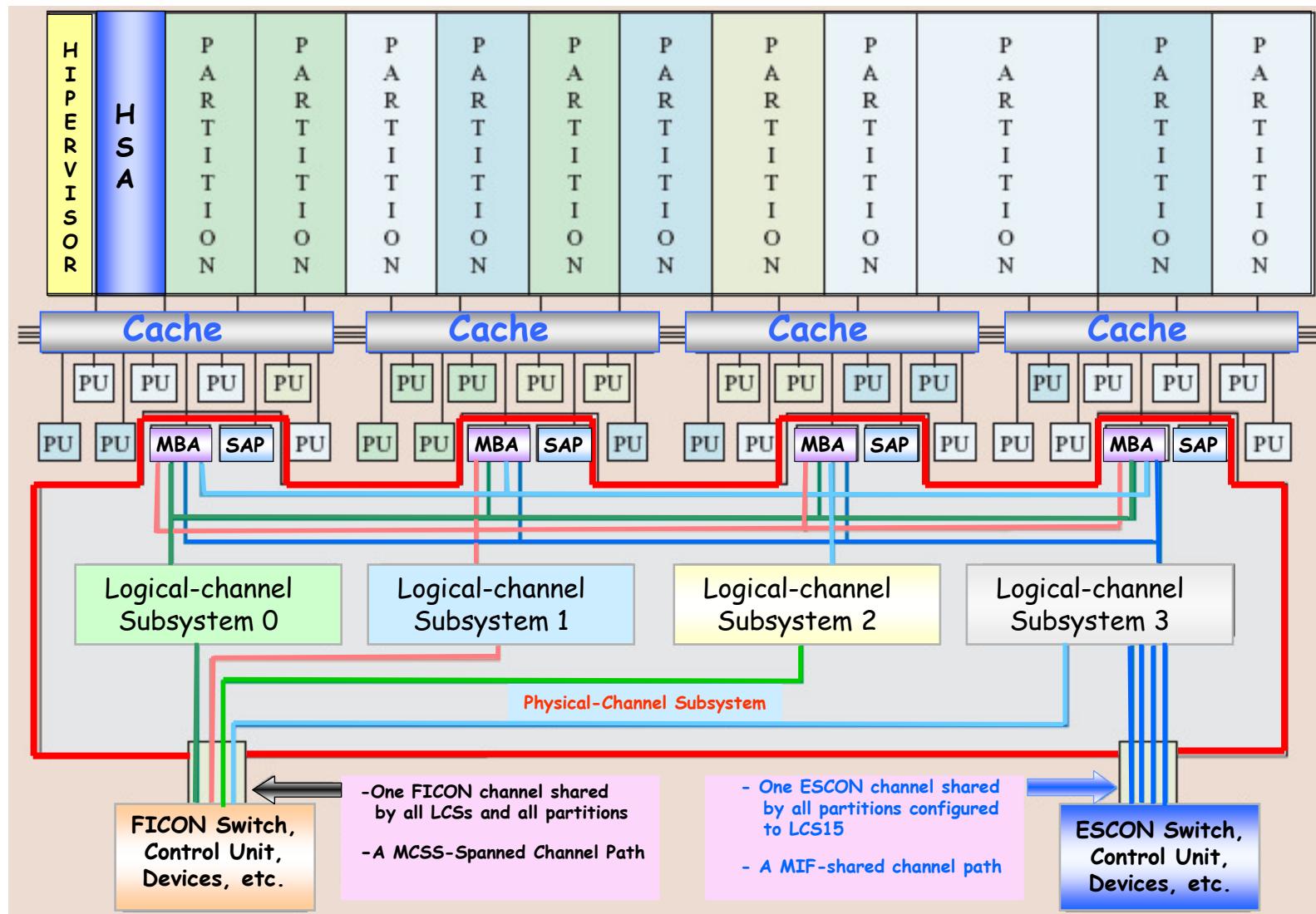
One of the main strengths of the Mainframe computers is the ability to deal with a large number of simultaneous I/O operations. The channel subsystem (CSS) has a major role in providing this strength. The CSS manages the flow of information between I/O devices and central memory. By doing so it relieves CPUs of the task of communicating directly with I/O devices and permits data processing to proceed concurrently with I/O processing. The channel subsystem is built on the following components:

- **SAP (system assist processor)** One of the Mainframe processor types, the SAP connects the channel subsystem to the I/O devices that are attached to the channels. The SAP uses the I/O configuration loaded in the Hardware System Area (HSA), and knows which device is connected to each channel, and what is its protocol. The SAP manages the queue of I/O operations passed to the channel subsystem by z/OS.
- **Channels** These are small processors that communicate with I/O control units (CU). They manage the transfer of data between central storage and the external device.
- **Channel path** The channel subsystem communicates with I/O devices through channel paths. If a channel is shared between multiple logical partitions, each logical partition establishes a unique channel path to the each device using this channel.
- **Subchannels** A subchannel provides the logical appearance of a device to the program and contains the information required for performing a single I/O operation. One subchannel is provided for each I/O device addressable by the channel subsystem.

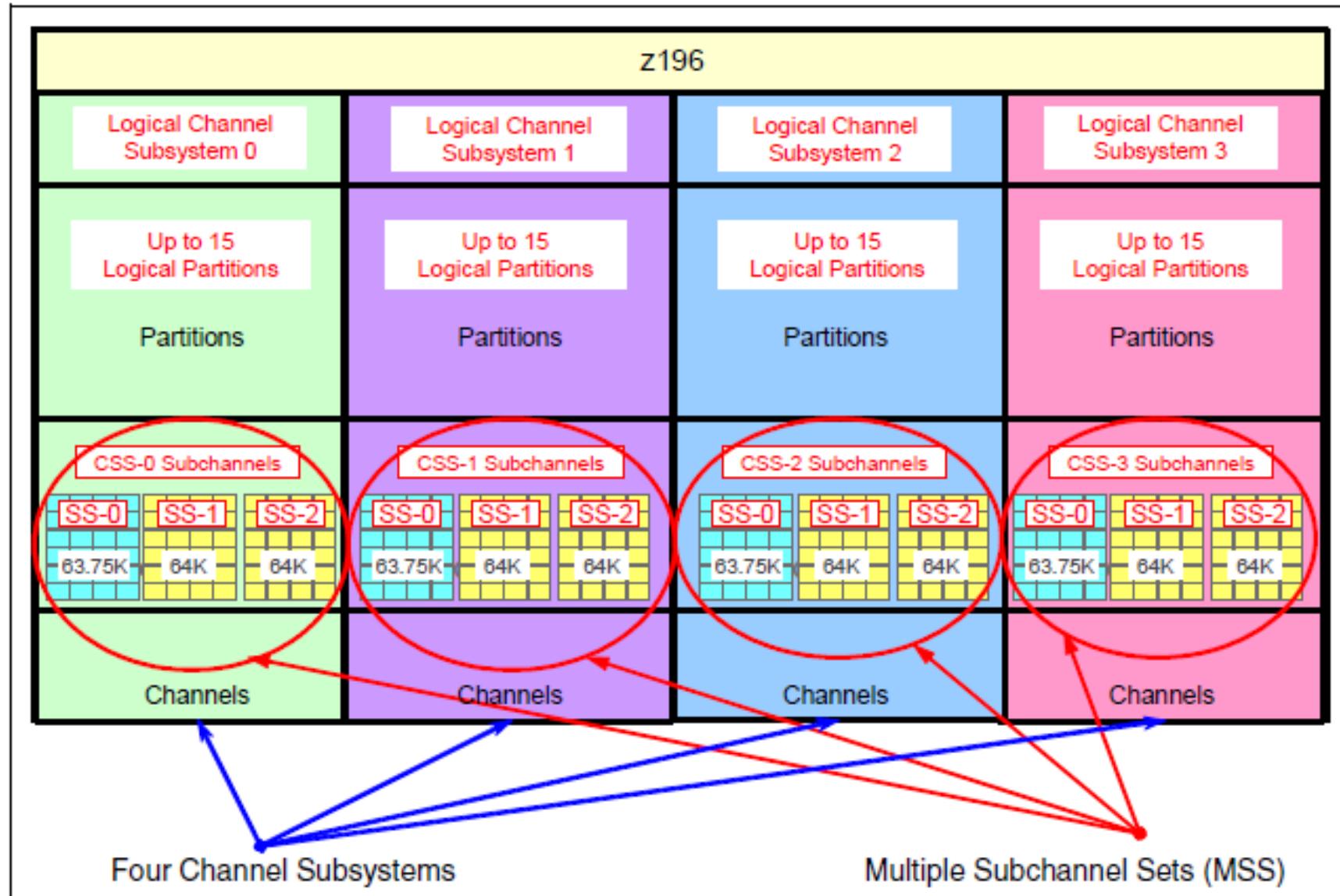
Channel Subsystem Relationship to Channels, Control Units and I/O Devices



The Mainframe I/O Logical Channel Subsystem Schematic

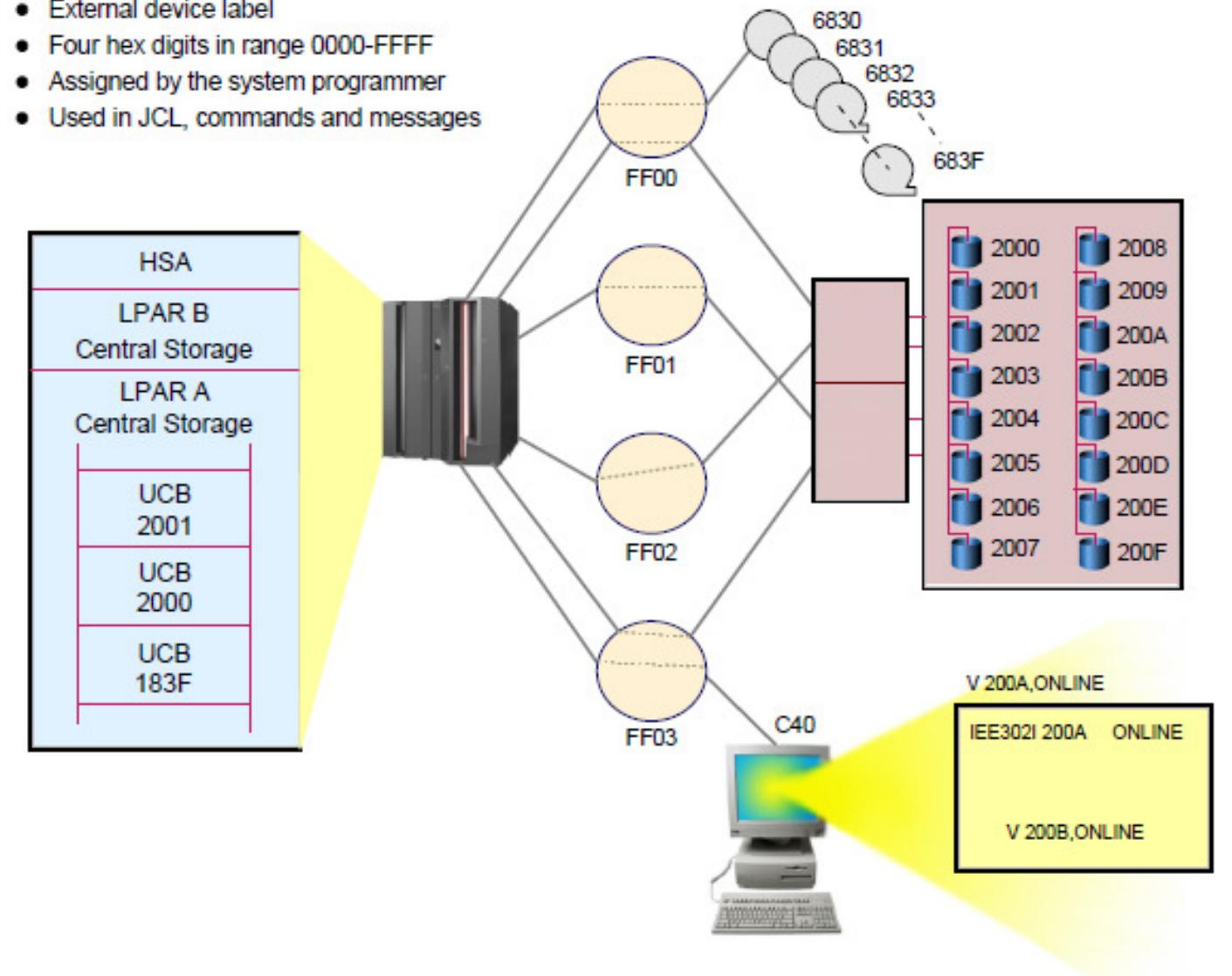


Multiple channel subsystems and multiple subchannel sets



I/O Device addressing

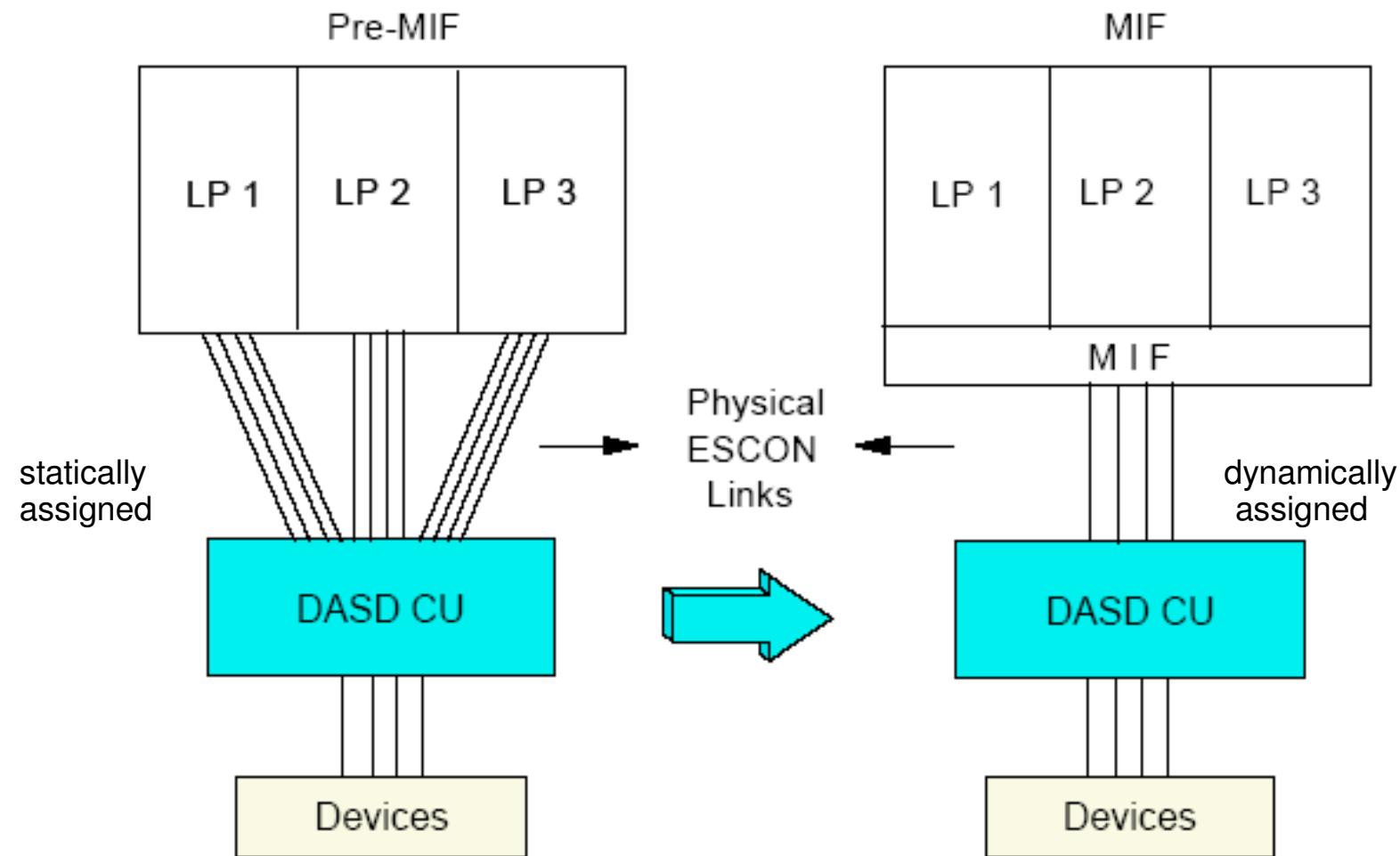
- External device label
- Four hex digits in range 0000-FFFF
- Assigned by the system programmer
- Used in JCL, commands and messages



System z I/O Connectivity

- ESCON and FICON channels
- Switches to connect peripheral devices to more than one CEC
- CHPID addresses are two hex digits (**FF / 256**)
- Multiple partitions can share CHPIIDs (**MIF**)
- I/O subsystem layer exists between the operating system and the CHPIIDs
- I/O control layer uses a control file IOCDS that translates physical I/O addresses into devices numbers that are used by z/OS
- Device numbers are assigned by the system programmer when creating the IODF and IOCDS and are arbitrary (but not random!)
- On modern machines they are three or four hex digits
 - example - FFFF = 64K devices can be defined**
- The ability to have dynamic addressing theoretically 7,848,900 maximum number of devices can be attached.

MIF Channel Consolidation - example

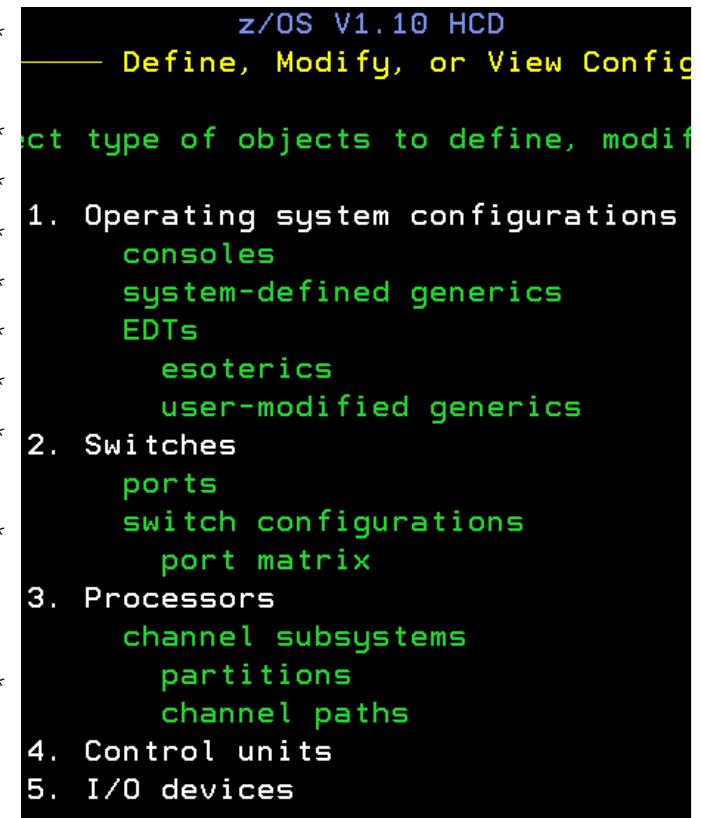


HCD & Sample IOCP

```
ID      MSG2='ESRAU.IODF99 - 2011-02-15 22:05',SYSTEM=(2097,1), *
LSYSTEM=CECDCEA,
*TOK= ('CECDCEA',00800007C74E2094220520410111046F00000000,*
00000000,'11-02-15','22:05:20','ESRAU','IODF99')

RESOURCE PARTITION=((CSS(0),(PCF2GAR2,5),(PRDA,1),(PRDC,2),(PR*
DE,3),(PRDF,4),(*,6),(*,7),(*,8),(*,9),(*,A),(*,B),(*,C)*
,(*,D),(*,E),(*,F)),(CSS(1),(*,1),(*,2),(*,3),(*,4),(*,5)*
),(*,6),(*,7),(*,8),(*,9),(*,A),(*,B),(*,C),(*,D),(*,E),*
(*,F)),(CSS(2),(*,1),(*,2),(*,3),(*,4),(*,5),(*,6),(*,7)*
,(*,8),(*,9),(*,A),(*,B),(*,C),(*,D),(*,E),(*,F)),(CSS(3)*
),(*,1),(*,2),(*,3),(*,4),(*,5),(*,6),(*,7),(*,8),(*,9),*
(*,A),(*,B),(*,C),(*,D),(*,E),(*,F)))

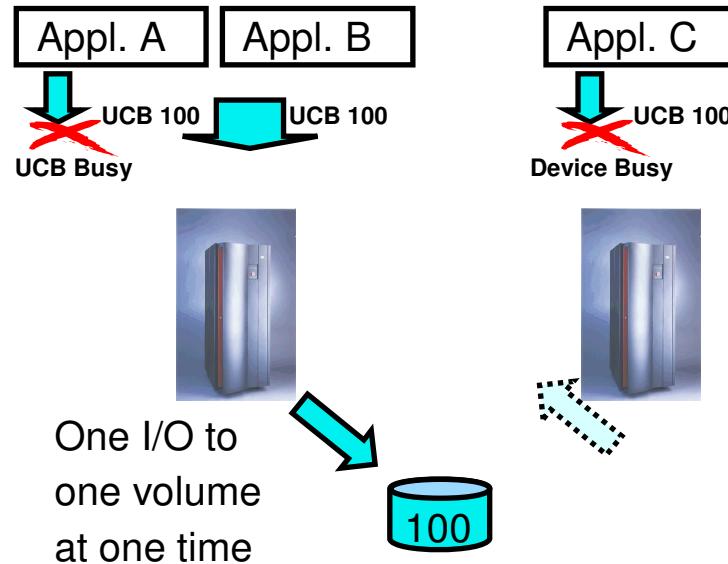
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...
CNTLUNIT CUNUMBR=FFFD,PATH=((CSS(0),08,09,0A,0B,0C,0D,0E,0F)),*
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IODEVICE ADDRESS=(FF90,007),CUNUMBR=(FFFD),UNIT=CFP
IODEVICE ADDRESS=(FF97,007),CUNUMBR=(FFFD),UNIT=CFP
```



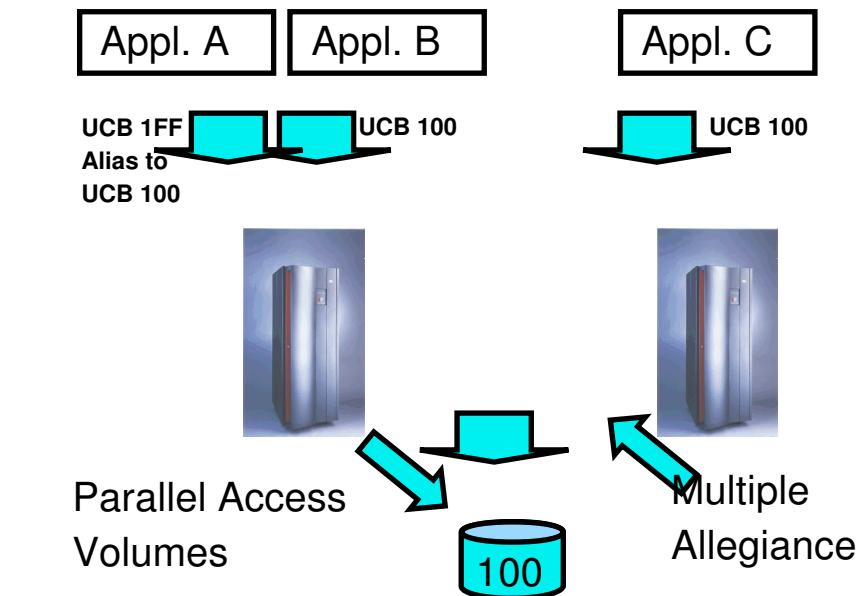
PAV (Parallel Access Volume) & MA (Multiple Allegiance)

- IBM PAV enables System z to process multiple I/Os to same logical volume at once
- IBM Multiple Allegiance (concurrent execution of multiple requests from multiple hosts) expands capability across multiple System z servers
- I/O Priority enables use of info from z/OS Workload Manager to manage I/O processing order

I/O without PAV/MA

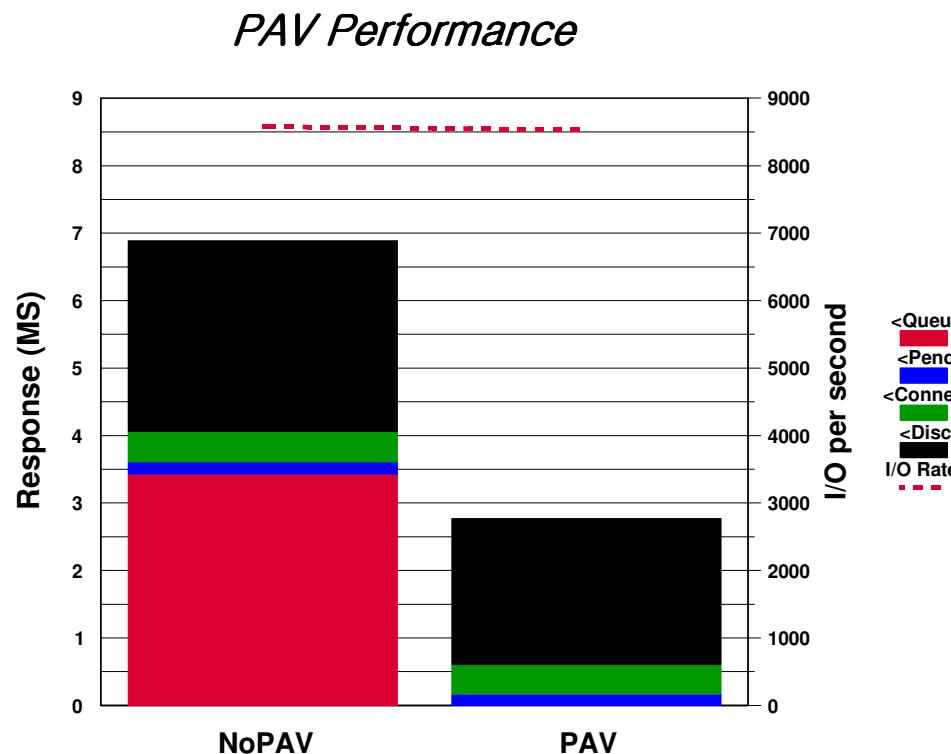


I/O with PAV/MA

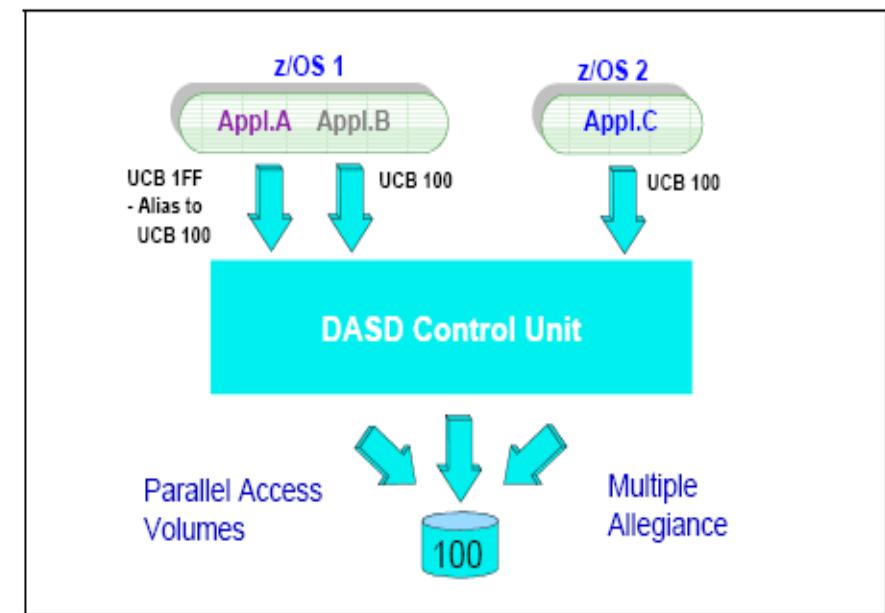


IBM PAV – Static, Dynamic & Hyper

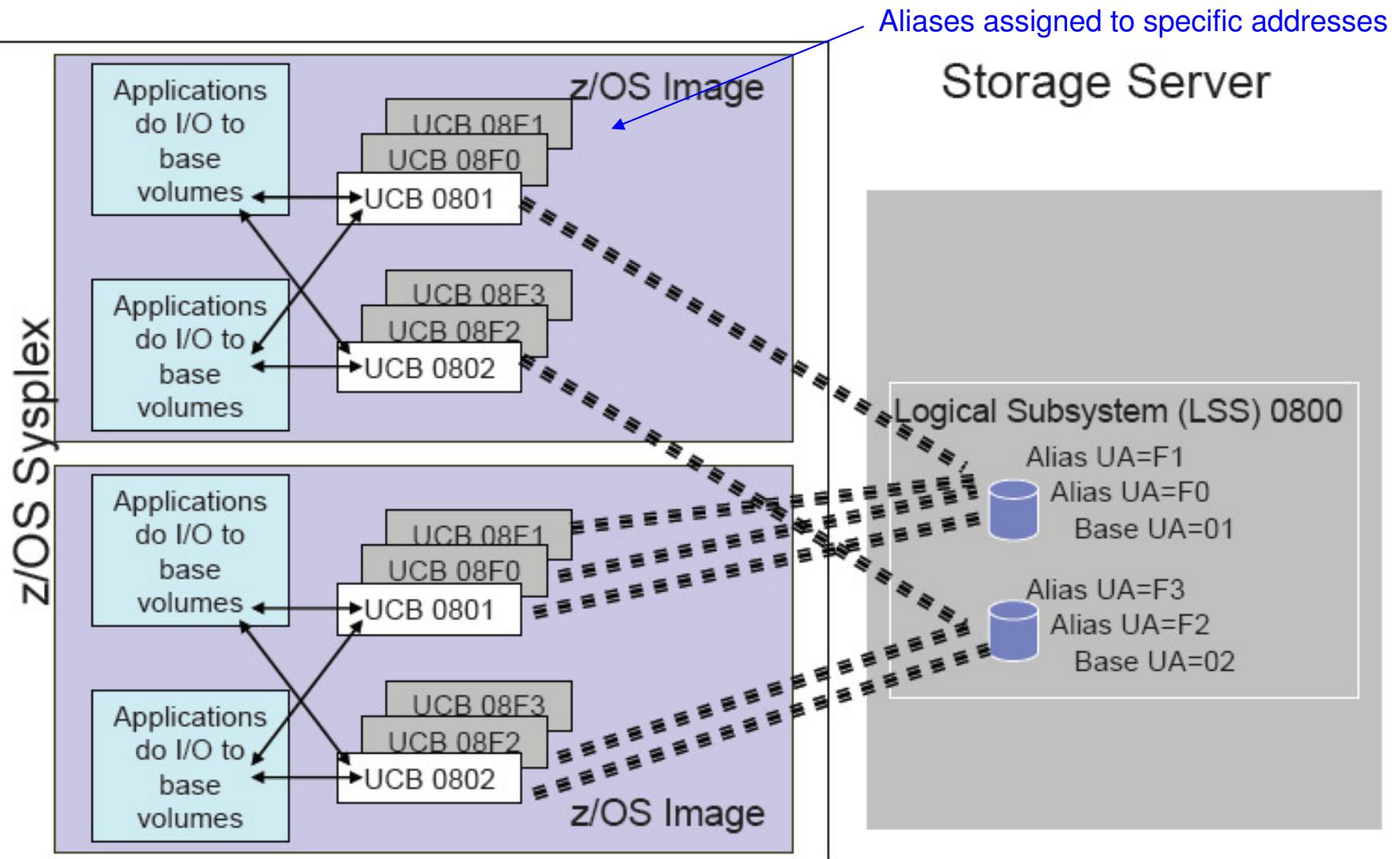
- **Static PAV:** Aliases are always associated with the same Base Address.
- **Dynamic PAV:** Aliases are assigned up front but can be reassigned to any base address as need dictates: WLM function call Dynamic Alias Management - reactive alias assignment
- **HyperPAV:** On demand/ Proactive alias assignment



I/O flow of PAV & MA

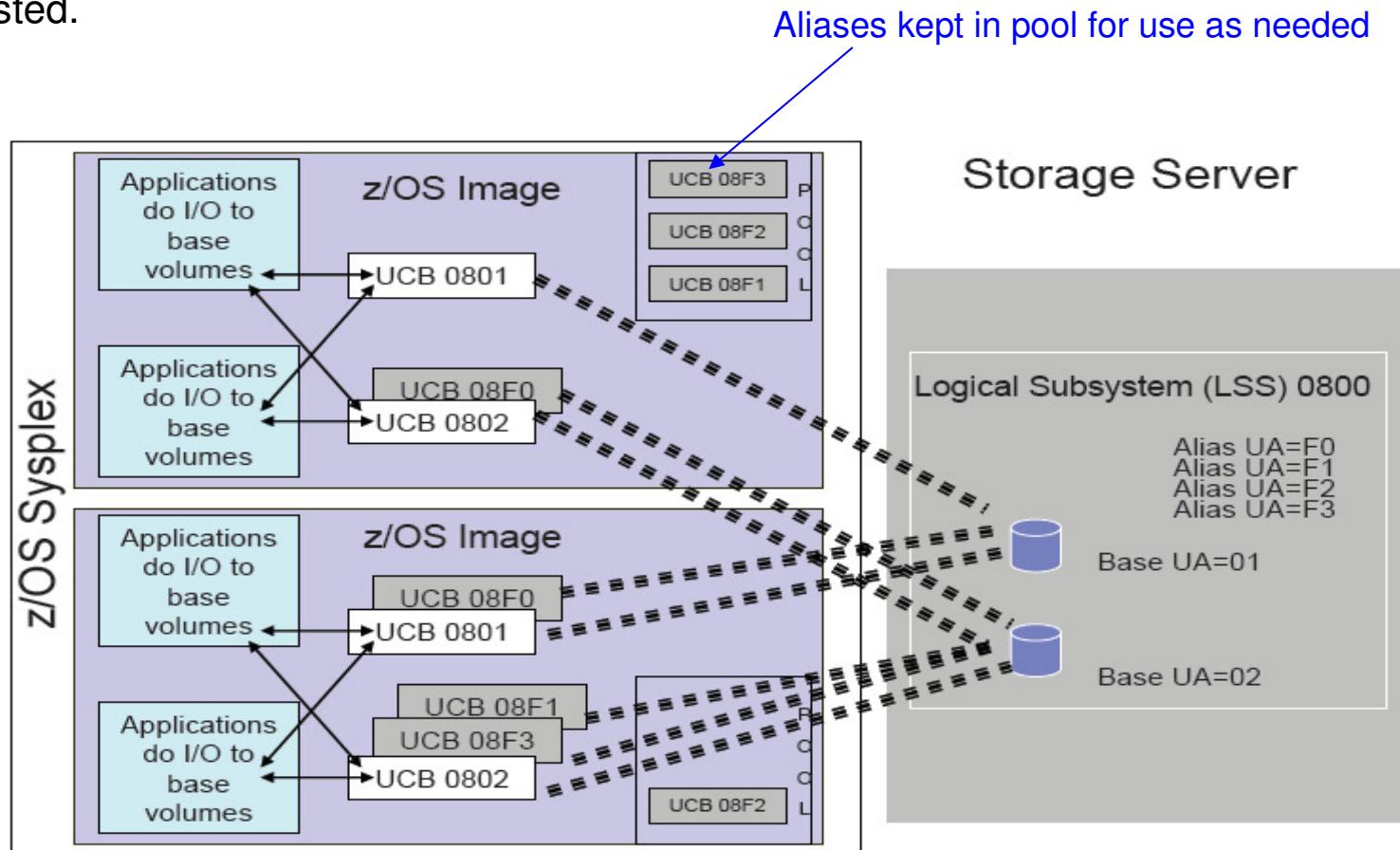


Static PAV & Dynamic PAV



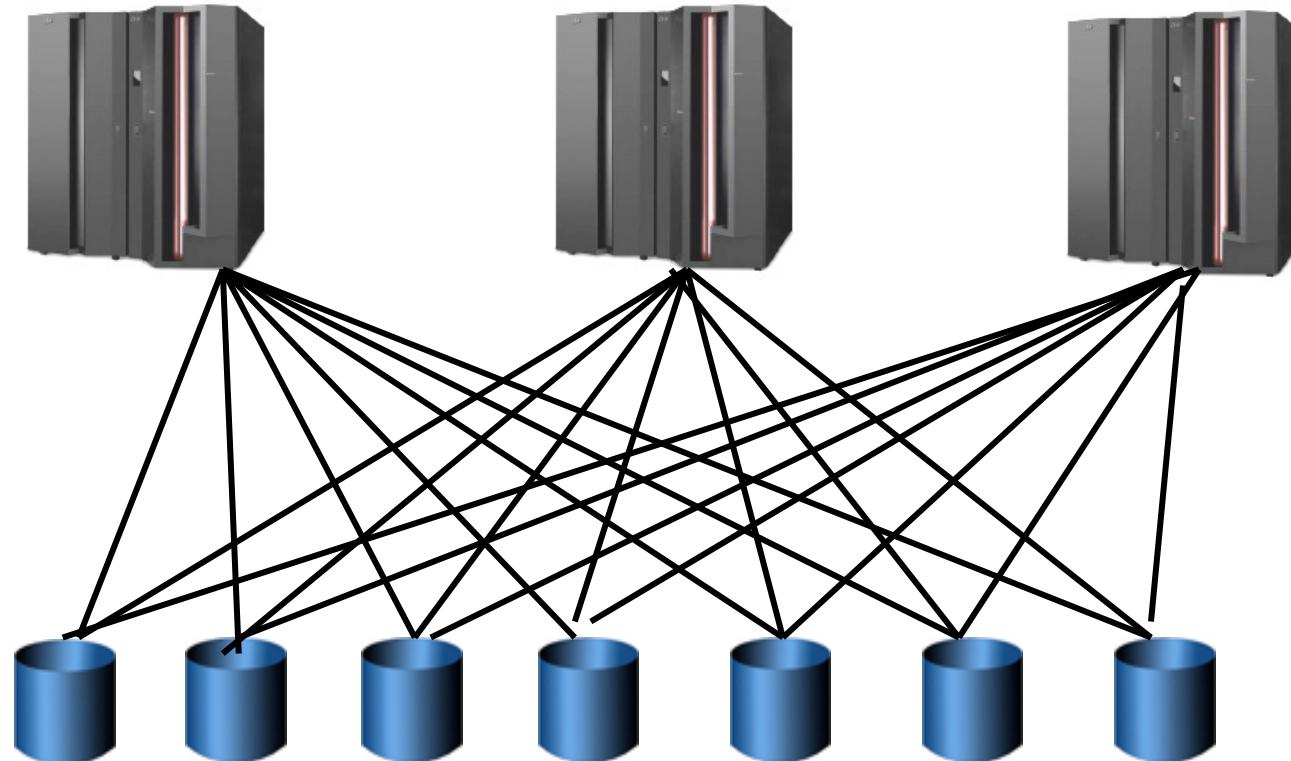
Hyper PAV

- Alias is taken from and returned to a pool instead of LCU.
- Define max. number of aliases per LCU in HCD.
- Every I/O Request is queued when all aliases allocated in the pool in the same LCU are exhausted.

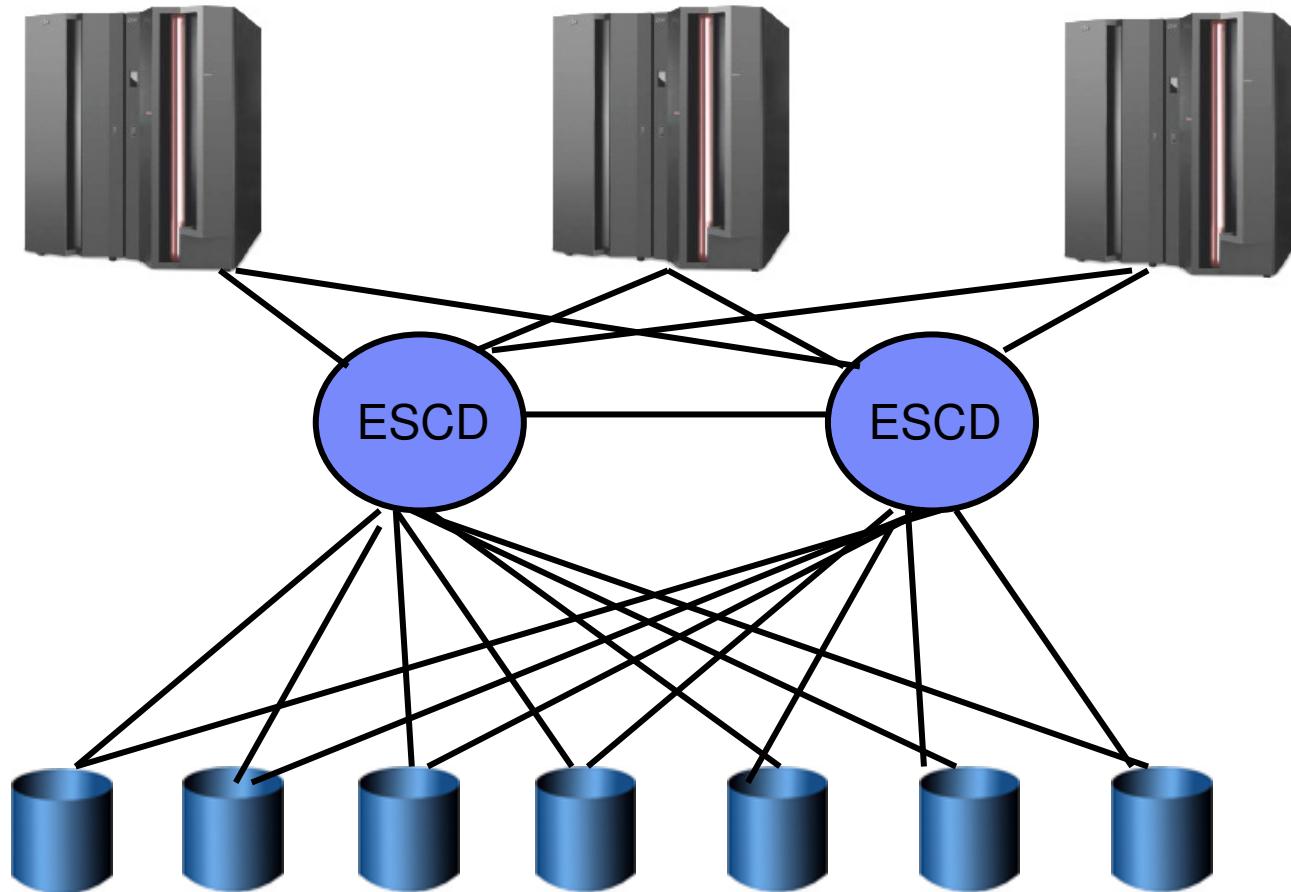


ESCON Connectivity

- ESCON (Enterprise Systems Connection) is a data connection created by IBM commonly used to connect their mainframe computers to peripheral devices.
- ESCON replaced the older, slower parallel Bus&Tag channel technology
- The ESCON channels use a director to support dynamic switching.

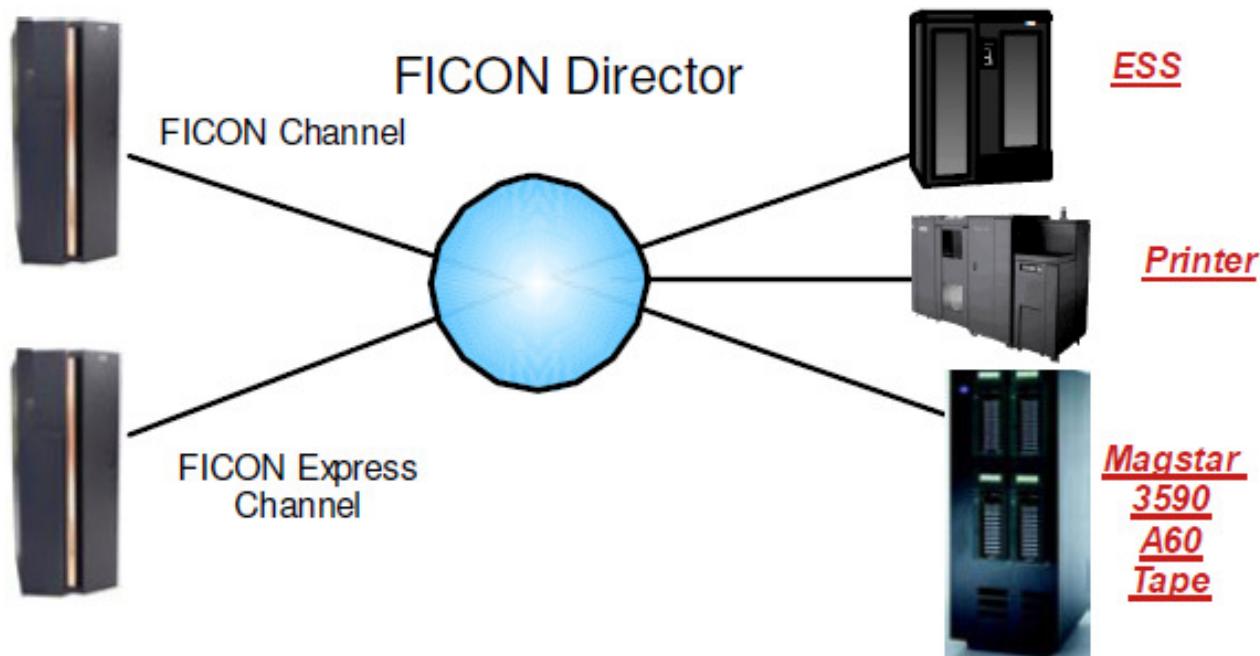


ESCON Director

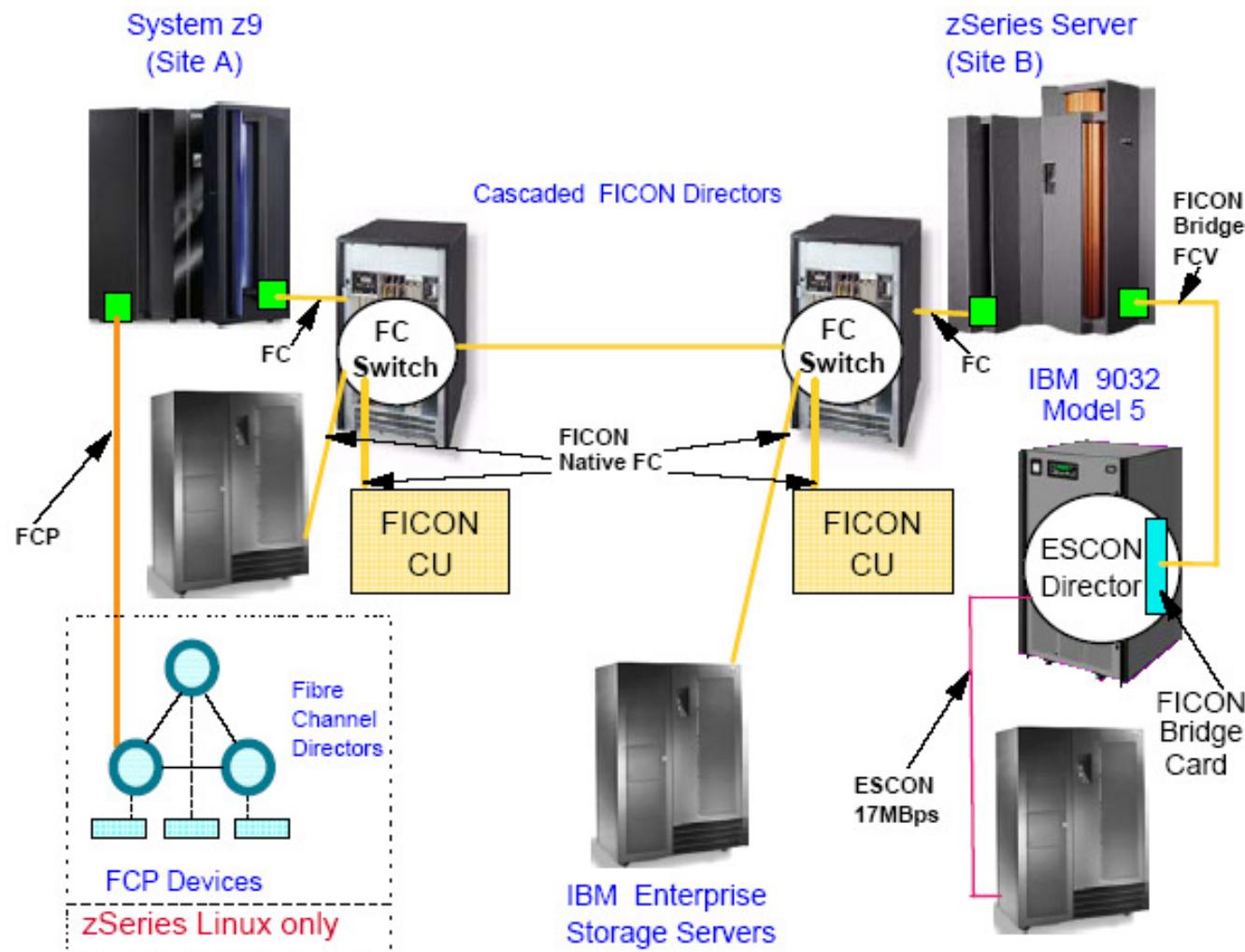


Fiber Connectivity (FICON)

- FICON (for Fiber Connectivity) was the next generation high-speed input/output (I/O) interface used by mainframe computer connections to storage devices.
- FICON channels increase I/O capacity through the combination of a new architecture and faster physical link rates to make them up to eight times as efficient as ESCON.



FICON Connectivity

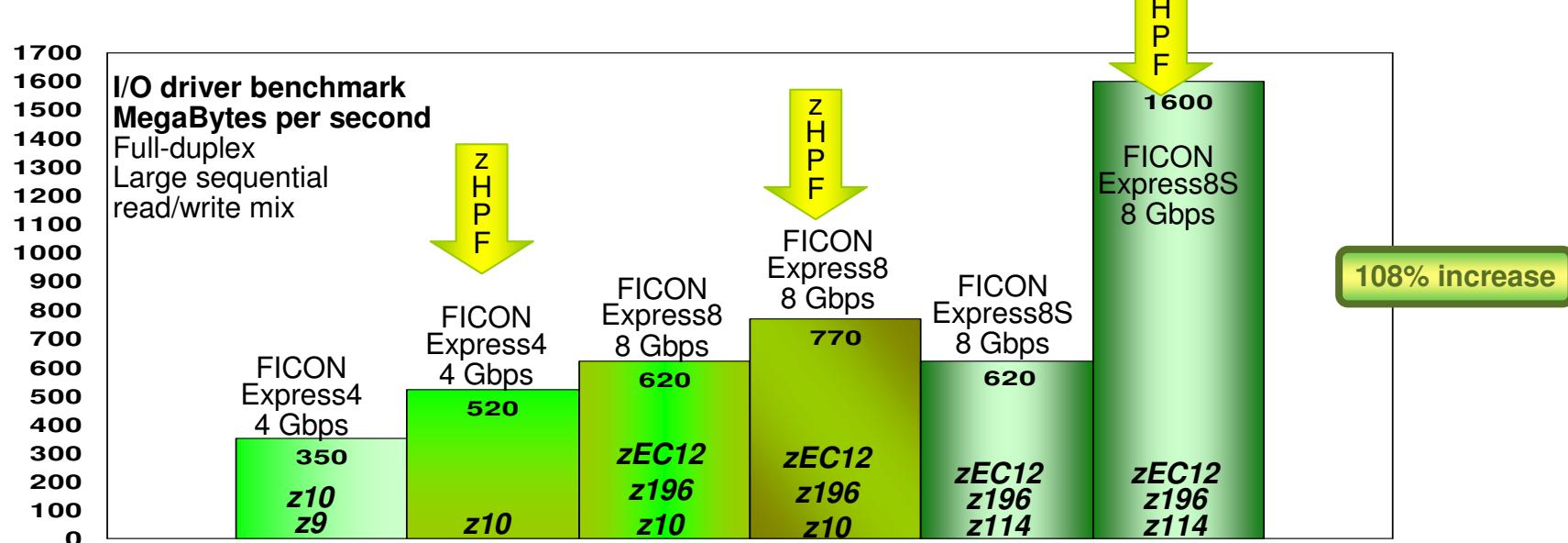
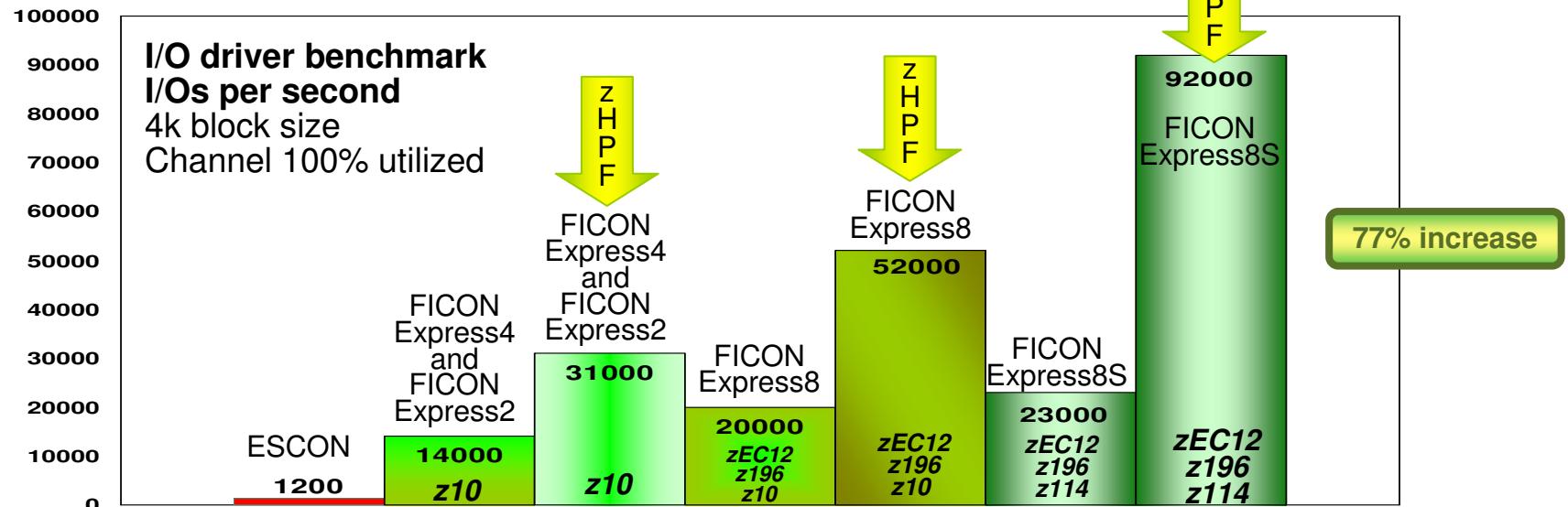


ESCON vs FICON

- ESCON
 - 20 Mbytes / Second
 - Lots of “dead time”. One active request at a time.
 - One target control unit

- FICON
 - 800 Mbytes / Second
 - Uses FCP standard
 - Fiber Optic cable (less space under floor)
 - Currently, up to 64 simultaneous “I/O packets” at a time with up to 64 different control units
 - Supports Cascading switches

FICON performance on System z



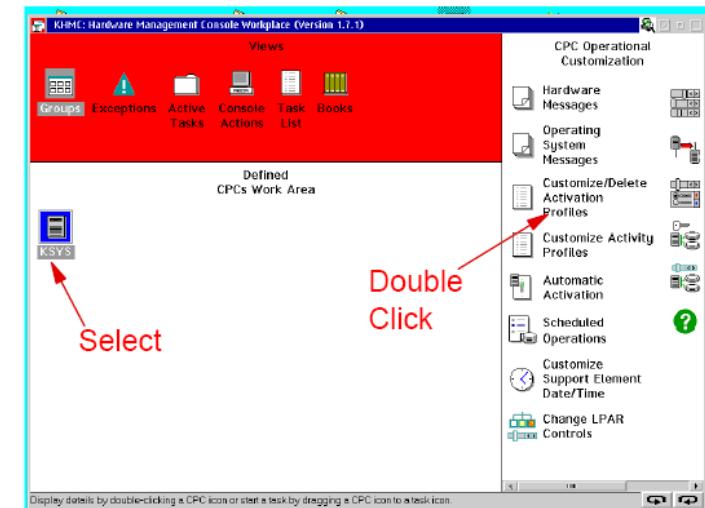
Hardware Management Console

Mainframe hardware can be managed by using either the Support Elements directly attached to the server or using the Hardware Management Console (HMC), which is a desktop application providing the end user interface to control and monitor the status of the system.

Working from an HMC, an operator, a system programmer, or IBM technical personnel can perform basic operations on the Mainframe servers. The HMC is a powerful console that can load and shut down system images as well as the entire machine. Some of the common capabilities of the HMC are:

- Load the Mainframe hardware configuration.
- Load or reset a system image.
- Add and change the hardware configuration (most of them dynamically).
- Access the hardware logs.

All these functions can be executed using a browser interface in a totally secure environment.



Reserved processors & storage

Reserved processors are defined by the Processor Resource/Systems Manager (PR/SM) to allow for a nondisruptive capacity upgrade. Reserved processors are like spare logical processors, and can be shared or dedicated. Reserved CPs should be defined to a logical partition to allow for nondisruptive image upgrades.

Reserved storage can optionally be defined to a logical partition, allowing a nondisruptive image memory upgrade for this partition. Reserved storage can be defined to both central and expanded storage, and to any image mode, except the coupling facility mode.

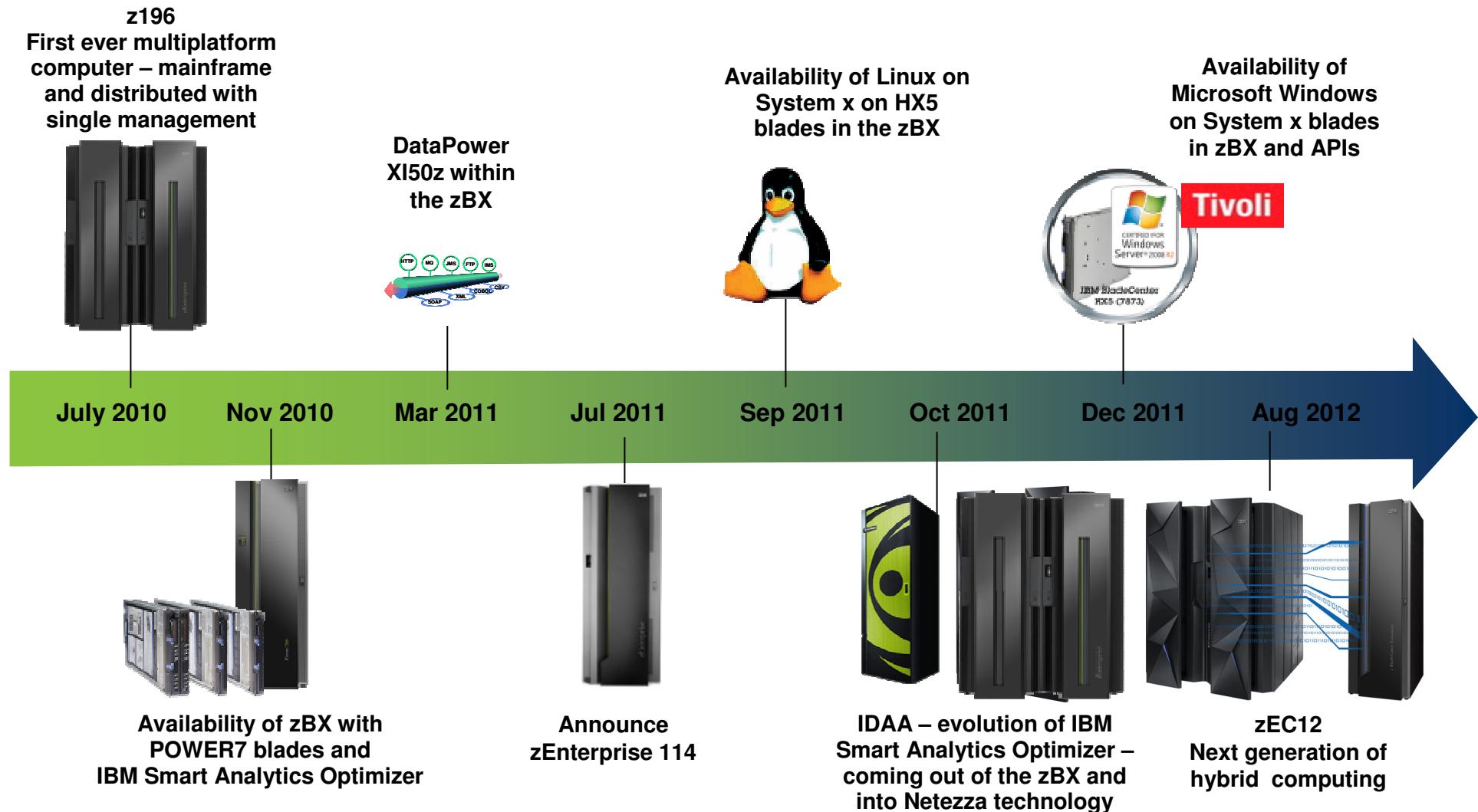
LPAR dynamic storage reconfiguration

Dynamic storage reconfiguration on z196 servers allows an operating system running in a logical partition to add (nondisruptively) its reserved storage amount to its configuration, if any unused storage exists. This unused storage can be obtained when another logical partition releases some storage or when a concurrent memory upgrade takes place. With dynamic storage reconfiguration, the unused storage does not have to be continuous.

HIGHLIGHTS of zEC12



Evolution of hybrid computing with IBM System z



Introducing the newest members of the zEnterprise System family

The zEnterprise EC12 and zEnterprise BladeCenter Extension Model 003

IBM zEnterprise EC12 (zEC12)

- zEC12 has the industry's fastest superscalar chip with each core at 5.5 GHz
- New innovation to drive availability with IBM zAware and Flash Express
- Optimized for the corporate data serving environment
- Hardware functions boost software performance for Java™, PL/I, DB2®



IBM zEnterprise Unified Resource Manager and zEnterprise BladeCenter® Extension (zBX) Mod 003

- Supports the new zEC12 platform
- Hosts PS701 and HX5 blades
- Provides workload-awareness resource optimization
- Enhancements to System Director support zBX
- System z will continue to expand hybrid computing

Plus more flexibility and function by connecting to IDAA

- IBM DB2 Analytics Accelerator (IDAA) allows deployment of business analytics on the same platform as operational applications
- Analytics and OLTP can be run as the same workload

zEC12 Overview



- Machine Type
 - 2827
- 5 Models
 - H20, H43, H66, H89 and HA1
- Processor Units (PUs)
 - 27 (30 for HA1) PU cores per book
 - Up to 16 SAPs per system, standard
 - 2 spares designated per system
 - Dependant on the H/W model - up to 20, 43, 66, 89, 101 PU cores available for characterization
 - Central Processors (CPs), Internal Coupling Facility (ICFs), Integrated Facility for Linux (IFLs), System z Application Assist Processors (zAAPs), System z Integrated Information Processor (zIIP), optional - additional System Assist Processors (SAPs)
 - Sub-capacity available for up to 20 CPs
 - 3 sub-capacity points
- Memory
 - RAIM Memory design
 - System Minimum of 32 GB
 - Up to 768 GB per book
 - Up to 3 TB for System and up to 1 TB per LPAR
 - 32 GB Fixed HSA, standard
 - 32/64/96/112/128/240/256 GB increments
 - Flash Express
- I/O
 - 6 GBps I/O Interconnects – carry forward only
 - Up to 48 PCIe interconnects per System @ 8 GBps each
 - Up to 4 Logical Channel Subsystems (LCSSs)
 - Up to 3 Sub-channel sets per LCSS
- STP - optional (No ETR)

zEnterprise EC12 Functions and Features (GA Driver Level 12K – September, 2012)

Five hardware models
Six core 32nm PU chip
Up to 101 processors configurable as CPs, zAAPs, zIIPs, IFLs, ICFs, or optional SAPs
Increased capacity processor (1.25 x z196)
Up to 20 sub capacity CPs at capacity settings 4, 5, or 6
z/Architecture Enhancements including 2 GB Pages, Transactional Execution and Runtime Instrumentation
2nd Generation out-of order design
Enhanced processor cache design
Dedicated data compression and crypto coprocessor on each PU
Up to 3 TB of Redundant Array of Independent Memory (RAIM)
Flask Express and pageable large page support
Crypto Express4S and Cryptographic enhancements
New Channel path selection algorithms

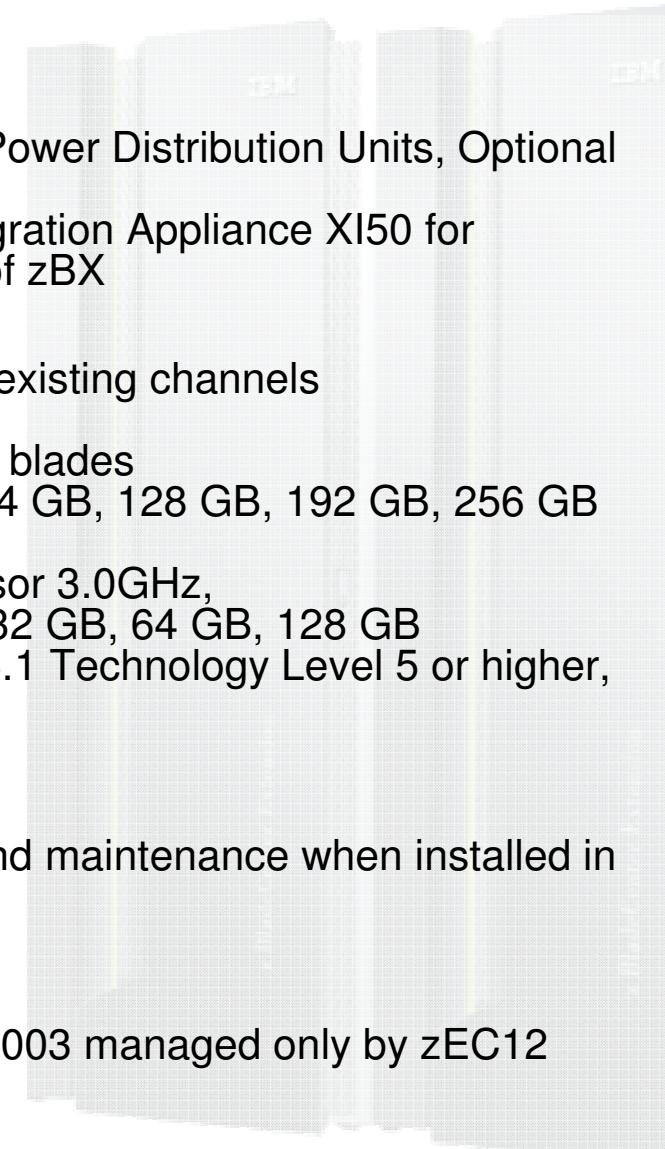


OSA-Express 4S 1000BASE-T
CFCC Level 18
IBM zAware
On Demand enhancements
Non-Raised floor option for Air Cooled System only with overhead I/O and power cabling options
Raised floor option for Air and Water Cooled System with overhead I/O and power cabling options
New 'radiator' design for Air Cooled System
Optional water cooling with Exhaust Air Heat Exchanger & air backup
Cycle Steering for Power Save and back-up for radiator and water cooled systems
Optional High Voltage DC power
Static Power Save Mode
Optional overhead Power and I/O cabling
NTP Broadband Authentication
zBX Model 003 and Unified Resource Manager

IBM zEnterprise BladeCenter Extension (zBX)

Machine Type: 2458 Model 003

- zBX is built with integrated IBM certified components
 - Standard parts – TOR switch, BladeCenter Chassis, Power Distribution Units, Optional Acoustic Panels
 - Optional optimizer - IBM WebSphere DataPower Integration Appliance XI50 for zEnterprise (DataPower XI50z) ordered as a feature of zBX
- Up to 112 blades are supported on zBX
 - System x and POWER7 blades are acquired through existing channels
 - IBM System x Blades – up to 56 entitlements
 - IBM BladeCenter HX5 (7873) dual-socket 16-core blades
Four supported memory configurations in zBX – 64 GB, 128 GB, 192 GB, 256 GB
 - IBM POWER7 Blades – up to 112 entitlements
 - IBM BladeCenter PS701 Express - 8-core processor 3.0GHz,
Three supported memory configurations in zBX - 32 GB, 64 GB, 128 GB
 - AIX: AIX 5.3 Technology Level 12 or higher, AIX 6.1 Technology Level 5 or higher, AIX 7.1
 - Up to 28 DataPower XI50z blades (double wide)
 - Mix and match blades in the same chassis
- System z support -- Blades assume System z warranty and maintenance when installed in the zBX
- Investment protection
 - Upgrade Model 002 to Model 003
 - Model 002 managed only by z196 or z114 and Model 003 managed only by zEC12



zEnterprise zBX Functions and Features

One hardware model
zBX is controlled by one specific zEC12
Up to 4 Racks (B, C, D and E)
2 BladeCenters Chassis per rack
Non-acoustics doors standard
Optional Rear Door Heat Exchanger
Optional Rear acoustic door
Redundant Power, Cooling and Management Modules
10 GbE and 1 GbE Network Modules
8 Gb FC modules
IEDN 10 GbE link aggregation between the BladeCenter and TORs



Advance Management Module
1000BASE-T and 10 GbE TORs
Up to 112 Blades
POWER7 Blades
IBM System x Blades
IBM WebSphere DataPower Integration Appliance XI50 for zEnterprise
Additional connectivity for SANs
HMCs for Unified Resource Manager
Upgraded Hypervisor levels
Unified Resource Manager support for zEC12 and zBX Model 003
Unified Resource Manager support for ensembles with zEC12, z196, z114, and zBX Models 002 and 003

Design highlights

- Offer a *flexible infrastructure*
- Offer state-of-the-art *integration* capability
- Offer *high performance*
- Offer the *high capacity and scalability*
- Offer the capability of *concurrent upgrades* for processors, memory, and I/O connectivity
- Implement a system with *high availability* and *reliability*
- Have broad internal and external *connectivity* offerings
- Provide the highest level of *security* in which every two PUs share a CP Assist for Cryptographic Function (CPACF).
- Be *self-managing* and *self-optimizing* – *IRD, Hiperdispatch*
- Have a *balanced system design*

zEC12 PU core design

- Derived from z196 core
 - Enhancing z196 Out of Order (OoO) execution design
 - Improved pipeline balance / reduced bottlenecks
 - Enhanced branch prediction latency and I-fetch throughput
 - Numerous small / local improvements to improve execution bandwidth and throughput
 - Can decode up to 3 instructions per cycle and initiate the execution of up to 7 instructions per cycle
- Main Highlights
 - New 2nd-level cache design
 - Distinct cache structures for instructions and operand L2
 - 33% larger (1MB each) and with improved latency on L1 misses
 - New 2nd-level branch prediction array
 - Improve capacity (24K branches) for large footprint enterprise workloads
 - Crypto / compression Co-processor per core
 - Faster improved startup latency
 - Improved CoP cache handling with effective miss latency reduction
 - Support for Unicode UTF8<>UTF16 conversions (CU12/CU21 bulk improvements)
 - Low-level power optimization at various design levels
 - Enable higher frequency within similar physical power constraints
 - Power capping features for DCA N-mode
 - Support new architectural features, such as
 - Transactional execution (TX)
 - Run-time instrumentation (RI)
 - EDAT-2

Core Design changes compared to z196

- Reduce Finite Cache Penalty
 - New L1/L2 cache structure for L2 latency reduction for both instruction and data misses
 - Bigger L2 (1M-Byte per instruction and Data L2 cache each) with shorter latency
 - D-TLB install buffer to improve d-TLB hit rates, improved hit under miss processing in TLB2
 - Various HW prefetcher and SW prefetch (PFD) handling improvements
- Improve OSC (fetch / store conflict) scheme
 - Additional culprit/victim tracking based on instruction TEXT (not just history based)
- Enhance branch prediction structure and sequential instruction fetching
 - secondary BTB (BTB2) effectively providing 33% more branches
 - Faster prediction throughput in BTB1 by usage of a Fast re-Indexing Table (FIT)
 - Improve sequential instruction stream delivery
- Millicode Handling
 - Selective HW execution of prior millicoded instructions (TR/TRT; STCK*)
 - Streamlined millicode entry to reduce hardware interlocks for commonly used instructions
 - e.g. MVCP
 - MVCL improvements
 - New millicode assist to prefetch data into L4 (in addition to architected addition to prefetch into L3)
 - Overlapping miss handling between
 - Speed up both aligned and unaligned data-moves through caches and through memory

z196 Architecture

- Continues line of upward-compatible Mainframe processors
- Rich CISC (Complex Instruction Set Computer) Instruction Set Architecture (ISA)
 - 984 instructions (762 implemented entirely in hardware)
 - 24, 31, and 64-bit addressing modes
 - Multiple address spaces robust inter-process security
 - Multiple arithmetic formats
 - Industry-leading virtualization support
 - High-performance logical partitioning via PR/SM
 - Fine-grained virtualization via z/VM scales to 1000's of images
 - Precise, model-independent definition of hardware/software interface
- Architectural extensions for IBM z196
 - 110+ new instructions added to improve compiled code efficiency
 - Decimal floating point quantum exceptions
 - New crypto functions and modes
 - Virtual architectural level

*RISC = Reduced Instruction Set Computer

zEC12 Architecture Extensions

- Transactional Execution (a/k/a Transactional Memory)
 - Software-defined sequence treated by hardware as atomic “transaction”
 - Enables significantly more efficient software
 - Highly-parallelized applications
 - Speculative code generation
 - Lock elision
 - Designed for exploitation by Java; longer-term opportunity for DB2, z/OS, others
- Runtime instrumentation
 - Real-time information to software on dynamic program characteristics
 - Enables increased optimization in JVM/JIT recompilations
 - Additional exploitation opportunities in the works
- 2 GB page frames
 - Increased efficiency for DB2 buffer pools, Java heap, other large structures
- Software directives to improve hardware performance
 - Data usage intent improves cache management
 - Branch pre-load improves branch prediction effectiveness
 - Block prefetch moves data closer to processor earlier, reducing access latency
- Decimal format conversions
 - Enable broader exploitation of Decimal Floating Point facility by COBOL programs

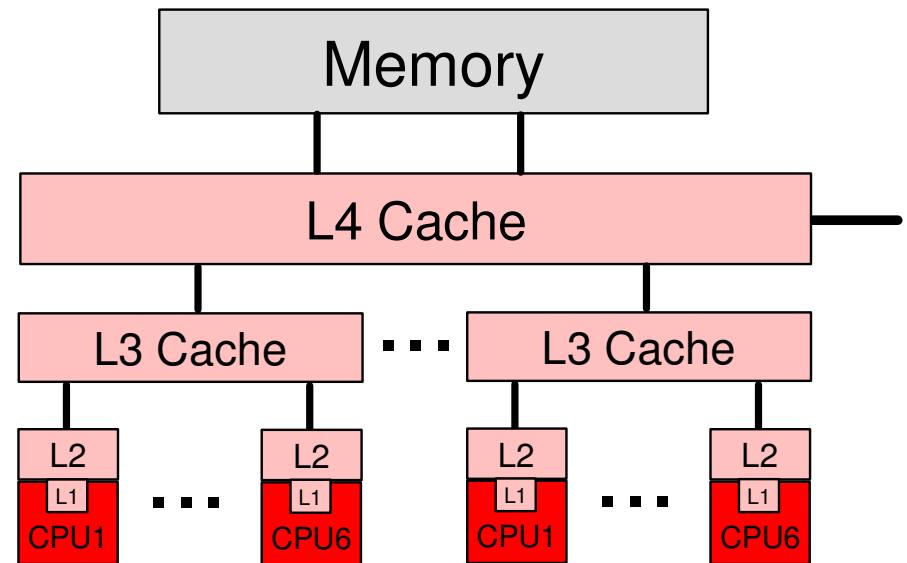
zEC12 Architecture Extensions - continued

- Run-time Instrumentation
 - A new hardware facility for managed runtimes
 - Tailored towards Java Runtime Environment (JRE)
 - Dynamic and self-tuning online recompilation
 - Not the same as current CPU Measurement Facility (CPUMF)
 - Both can be run concurrently
 - Allow dynamic optimization on code generation as it is being executed
 - Requires a much lower overhead environment (than current software-only profiling)
 - Provides information on hardware as well as program characteristics
 - enhances JRE decision-making by providing real-time feedback
- Key features
 - A collection buffer capturing a run-time trace till a instruction sample point, providing
 - “how we get here information”, e.g. branch history
 - Value profiling (of GPR) in the context of path traced
 - Meta-data collected for “what happened” information with the sample instruction
 - Cache miss
 - Branch prediction/resolution
 - 3 modes of sampling; by
 - cycle count, instruction count, or explicit indication

zEC12 Processor Design Basics

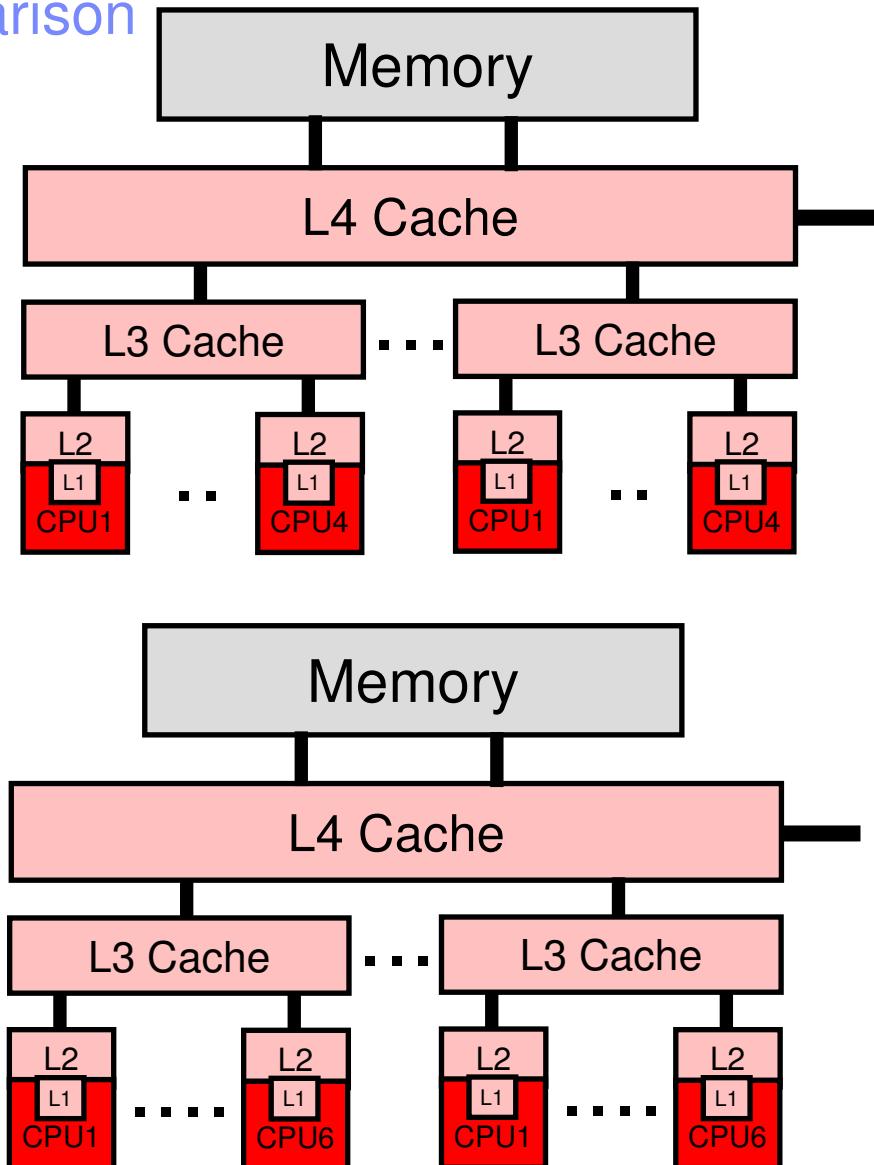
- Processor Design
 - PU core
 - Cycle time
 - Pipeline, execution order
 - Improved pipeline balance/reduced bottlenecks
 - Enhanced branch prediction and I-fetch
 - Streamlined store operations
 - Numerous small/local improvements
 - Hardware vs. millicode
 - Memory subsystem (nest)
 - High speed buffers (caches)
 - Improved latency on L1 misses
 - New 2nd-level cache design
 - Distinct structures for instructions and data
 - 1MB L1+ & 1MB 2nd-level cache per core
(z196 has 1.5 MB unified)

Logical View of Single Book



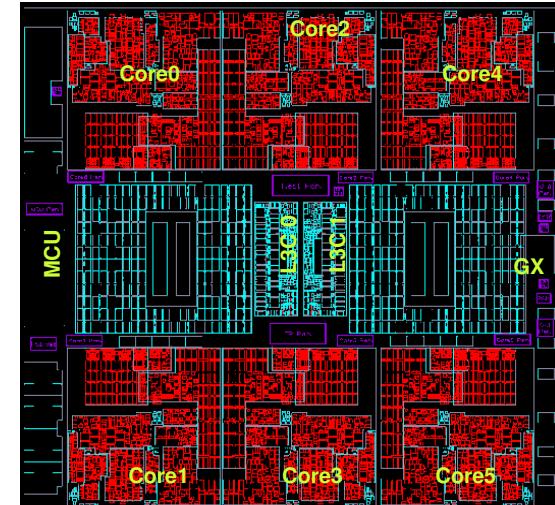
zEC12 versus z196 hardware comparison

- z196
 - CPU
 - 5.2 GHz
 - Out-Of-Order execution
 - Caches
 - L1 private 64k I, 128k D
 - L2 private 1.5 MB
 - L3 shared 24 MB / chip
 - L4 shared 192 MB / book
- zEC12
 - CPU
 - 5.5 GHz
 - Enhanced Out-Of-Order
 - Caches
 - L1 private 64k I, 96k D
 - L2 private 1 MB I + 1 MB D
 - L3 shared 48 MB / chip
 - L4 shared 384 MB / book

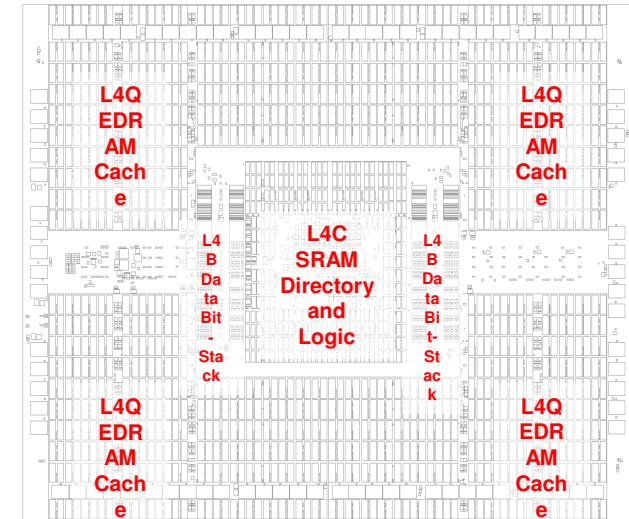


zEC12 Processor Design

- Built on solid foundation of z196
 - Leverage IBM 32nm SOI technology with eDRAM
- Enhanced high-frequency out-of-order core
 - Instruction pipeline streamlined for smoother flow
 - 2nd-level BTB expands branch prediction coverage
 - Faster engine for fixed-point division
 - Millicode performance improvements
- Cache hierarchy leadership extended
 - New structure for 2nd-level private cache
 - Separate optimizations for instructions and data
 - Reduced access latency for most L1 misses
 - 3rd-level on-chip shared cache doubled to 48MB
 - 4th-level book-shared cache doubled to 384MB
- More processors in the same package as z196
 - 6 processor cores per CP chip
 - Crypto/compression co-processor per core
 - Same power consumption as z196

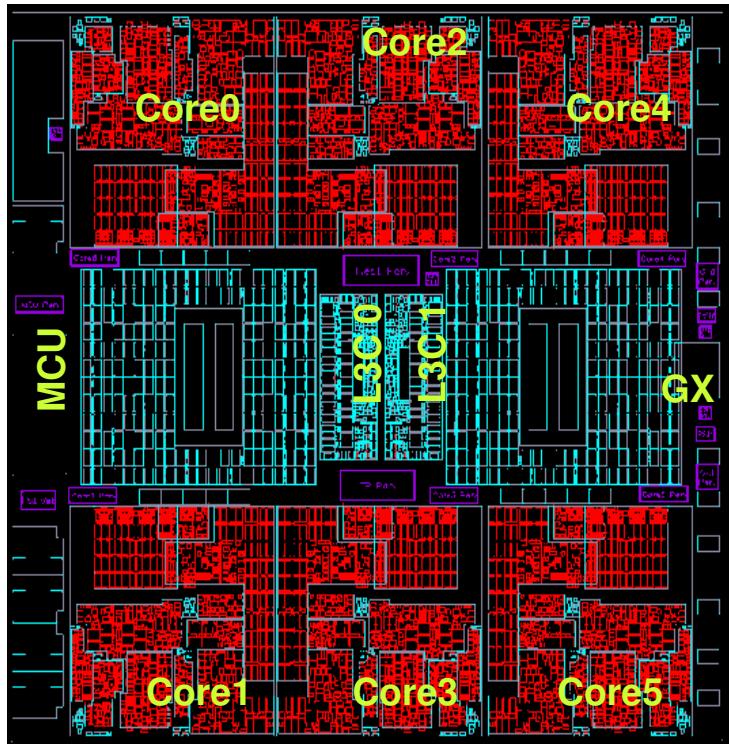


zEC12 PU Chip: 6 cores, 598 mm² chip



zEC12 SC Chip: 192MB cache, 526 mm² chip

zEC12 Hexa Core PU Chip Details

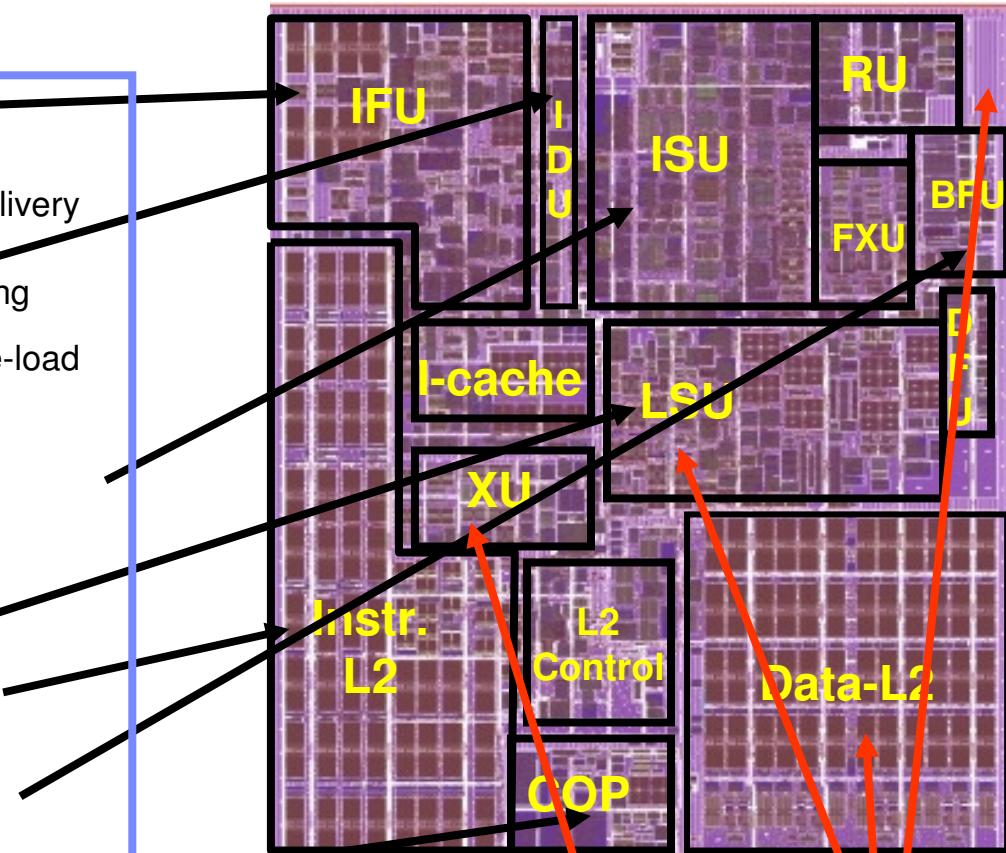


- 13S 32nm SOI Technology
 - 15 layers of metal
 - 7.68 km wire
- 2.75 Billion Transistors
- Chip Area
 - 597 mm²
 - 23.7mm x 25.2mm
 - 10000+ Power pins
 - 1071 signal I/Os

- Up to Six active cores per chip
 - 5.5 GHz
 - L1 cache/ core
 - 64 KB I-cache
 - 96 KB D-cache
 - L2 cache/ core
 - 1M+1M Byte hybrid split private L2 cache
- Dedicated Co-processors (COP) per core
 - Crypto & compression accelerators
 - Includes 16KB cache
- On chip 48 MB eDRAM L3 Cache
 - Shared by all six cores
- Interface to SC chip / L4 cache
 - 44 GB/sec to each of 2 SCs (5.5 GHz)
- I/O Bus Controller (GX)
 - Interface to Host Channel Adapter (HCA)
- Memory Controller (MC)
 - Interface to controller on memory DIMMs
 - Supports RAIM design

zEC12 PU Details

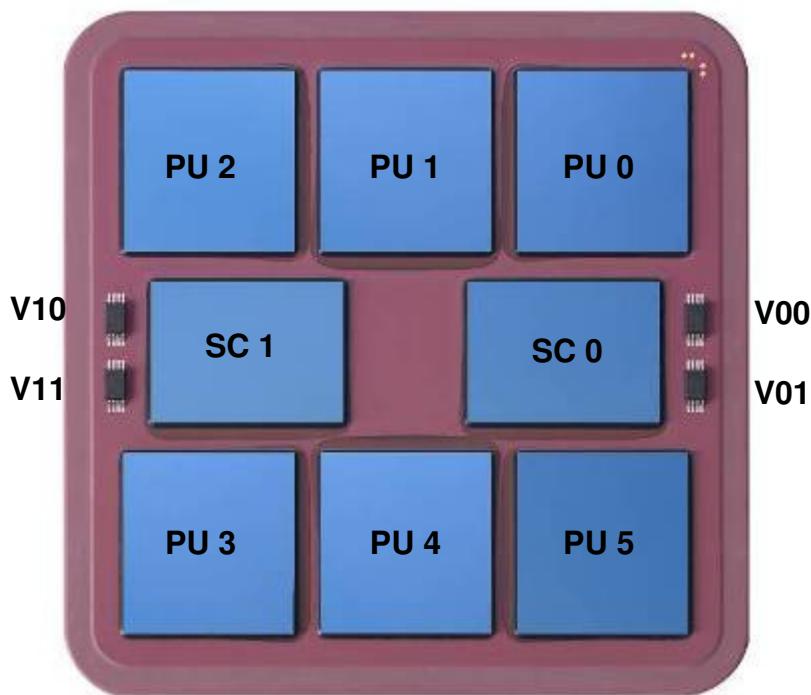
- Improved Instruction Fetching Unit
 - faster branch prediction
 - 2nd-level branch prediction
 - improved sequential instruction stream delivery
- Improved Out-of-order efficiency
 - better group formation, including regrouping
 - “uncracked” common instructions
 - on-the-fly Culprit/Victim detection for store-load hazards
- Increased Execution/Completion Throughput
 - bigger GCT, speculative completion
 - virtual branch unit
- Innovative Local Data-Cache design
 - store banking in Data-L1
 - unique Data-L2 cache (1M-byte) design
- Dedicated Instruction-L2 cache (1M-byte)
- Optimized Floating-Point Performance
 - Increased physical pool for FPRs
 - fixed-point divide in DFU
- Dedicated Co-Processor
 - Designed for improved start-up latency
 - UTF8<->UTF16 conversion support



- Main Architectural Extension Support
 - Transactional Memory support
 - Run-time instrumentation support
 - EDAT-2 support

zEC12 Multi-Chip Module (MCM) Packaging

- 96mm x 96mm MCM
 - 102 Glass Ceramic layers
 - 8 chip sites
- 7356 LGA connections
 - 27 and 30 way MCMs
 - Maximum power used by MCM is 1800W
- CMOS 13s chip Technology
 - PU, SC, S chips, 32nm
 - 6 PU chips/MCM – Each up to 6 active cores
 - 23.7 mm x 25.2 mm
 - 2.75 billion transistors/PU chip
 - L1 cache/PU core
 - L2 cache/PU core
 - L3 cache shared by 6 PUs per chip
 - 5.5 GHz
 - 2 Storage Control (SC) chip
 - 26.72 mm x 19.67 mm
 - 3.3 billion transistors/SC chip
 - L4 Cache 192 MB per SC chip (384 MB/Book)
 - L4 access to/from other MCMs
 - 4 EEPROM (S) chips – 1024k each
 - 2 x active and 2 x redundant
 - Product data for MCM, chips and other engineering information
 - Clock Functions – distributed across PU and SC chips
 - Master Time-of-Day (TOD) function is on the SC



z196 MCM vs zEC12 MCM Comparison

z196 MCM

- MCM
 - 96mm x 96mm in size
 - 6 PU chips per MCM
 - Quad core chips with 3 or 4 active cores
 - PU Chip size 23.7 mm x 21.5 mm
 - 5.2 GHz
 - Superscalar, OoO execution
 - L1: 64 KB I / 128 KB D private/core
 - L2: 1.5 MB I+D private/core
 - L3: 24 MB/chip – shared
 - 2 SC chips per MCM
 - L4: 2 x 96 MB = 192 MB L4 per book
 - SC Chip size 24.5 mm x 20.5 mm

–1800 Watts

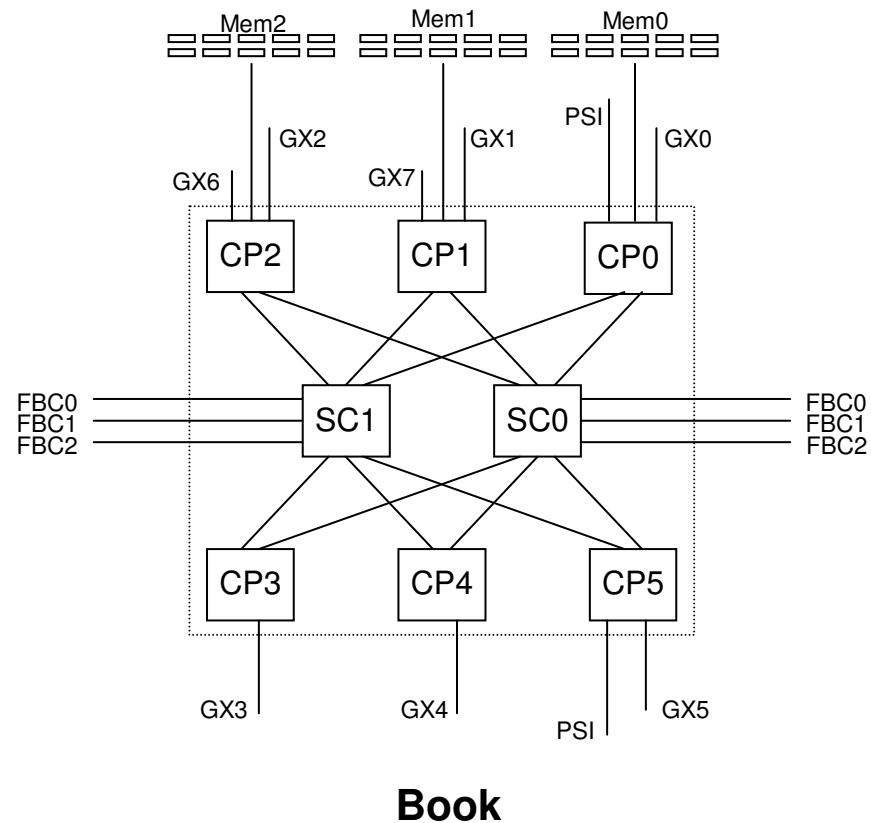
zEC12 MCM

- MCM
 - 96mm x 96mm in size
 - 6 PU chips per MCM
 - Hex-core chips with 4 to 6 active cores
 - PU Chip size 23.7mm x 25.2mm
 - 5.5 GHz
 - Superscalar, OoO enhanced
 - L1: 64 KB I / 96 KB D private/core
 - L2: 1 MB I / 1 MB D private/core
 - L3: 48 MB/chip - shared
 - 2 SC chips per MCM
 - L4: 2 x 192 MB = 384 MB L4 per book
 - SC Chip size 28.4mm x 23.9mm

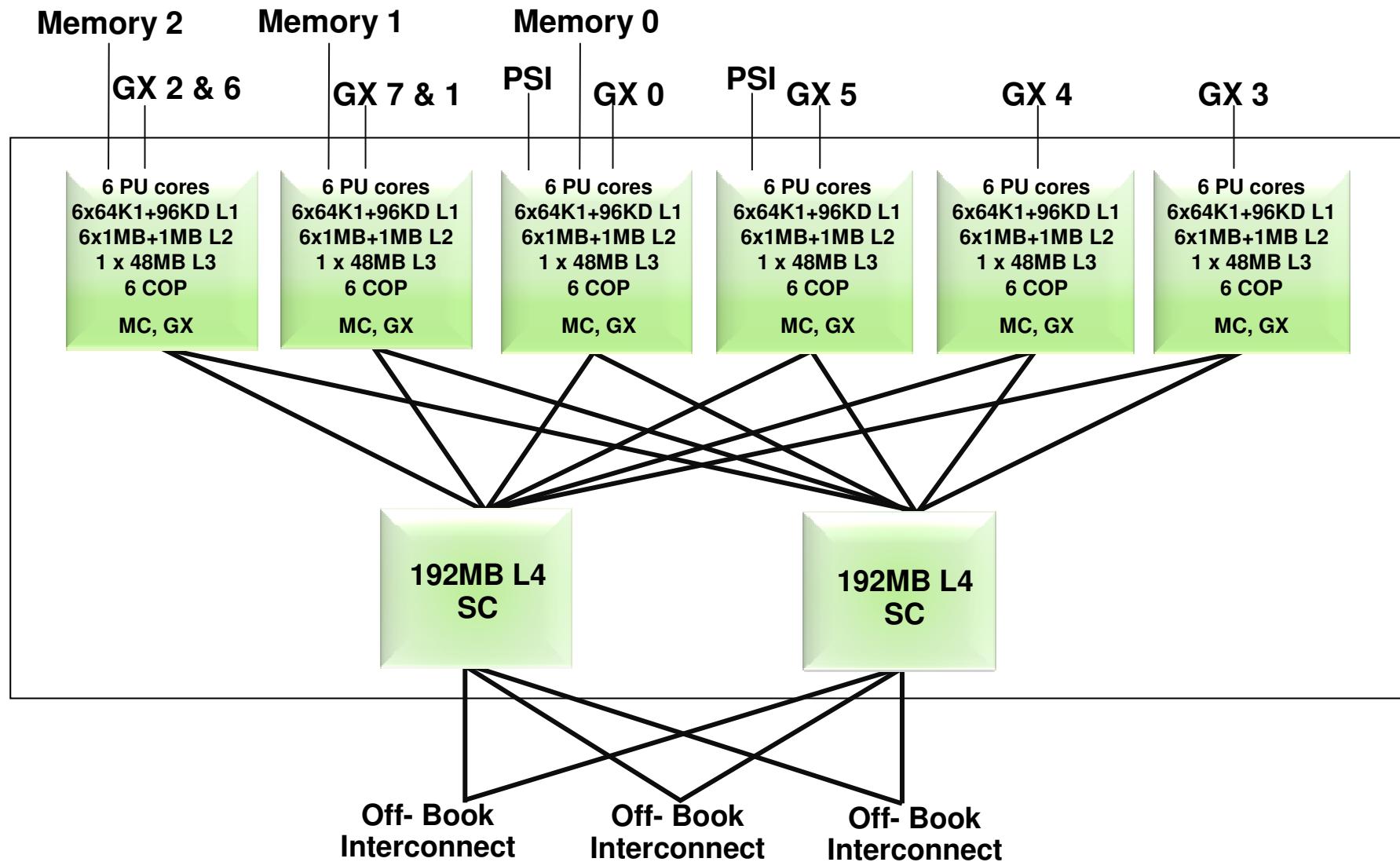
–1800 Watts

zEC12 Processor Sub-system Attributes

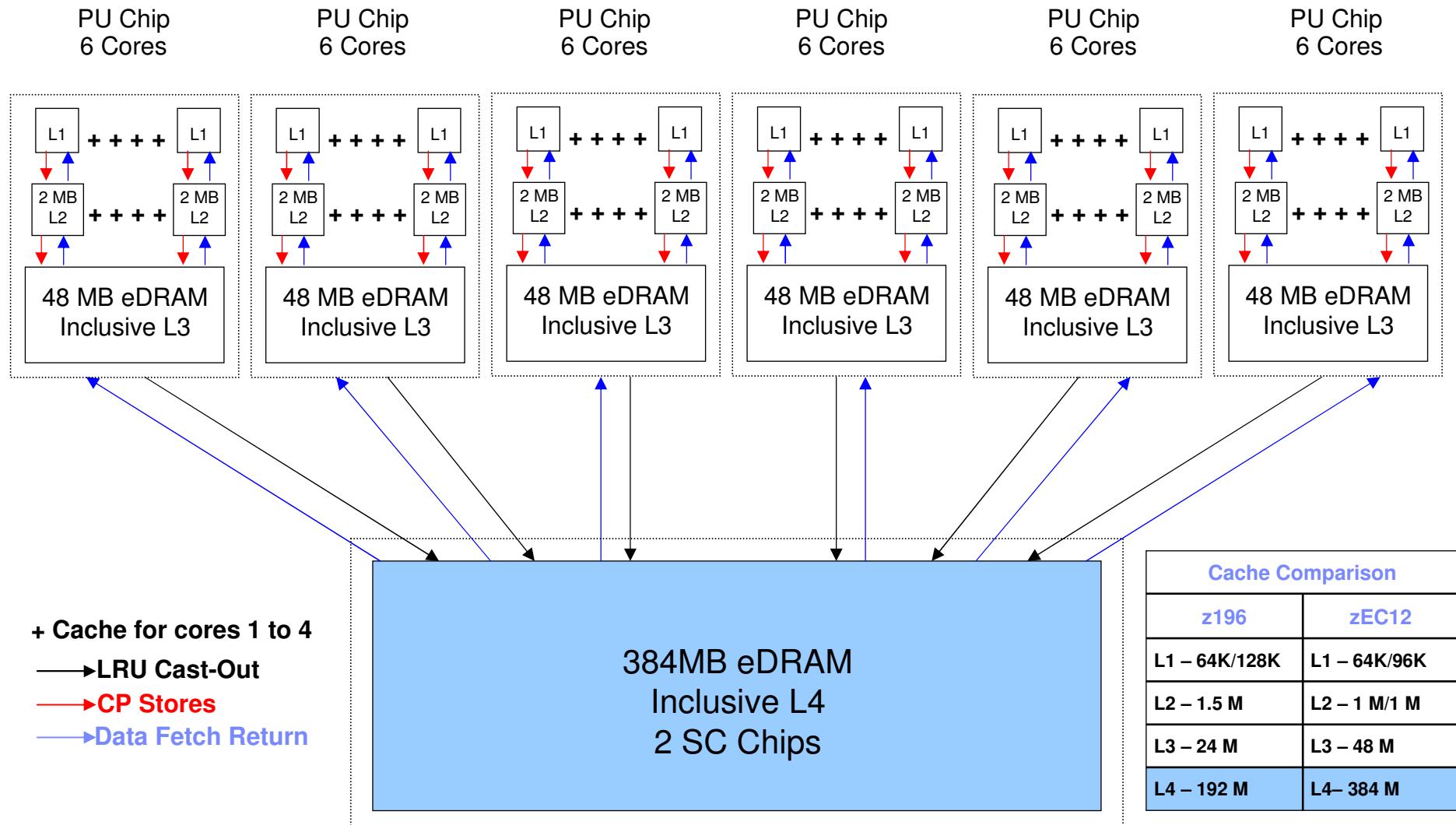
- 4 book System
 - Fully connected topology
 - 120 Processing Units
 - 12 Memory Controllers
 - Up to 24 I/O Hub and 48 ports
- Up to 3TB Memory capacity
 - 5-channel Memory RAIM protection
 - DIMM bus CRC error retry
 - 4-level cache hierarchy
 - eDRAM (embedded) caches
 - L3, L4 and SP Key Cache
- Concurrent Maintenance
 - Dynamic Book add/repair
- Support for I/O Hubs



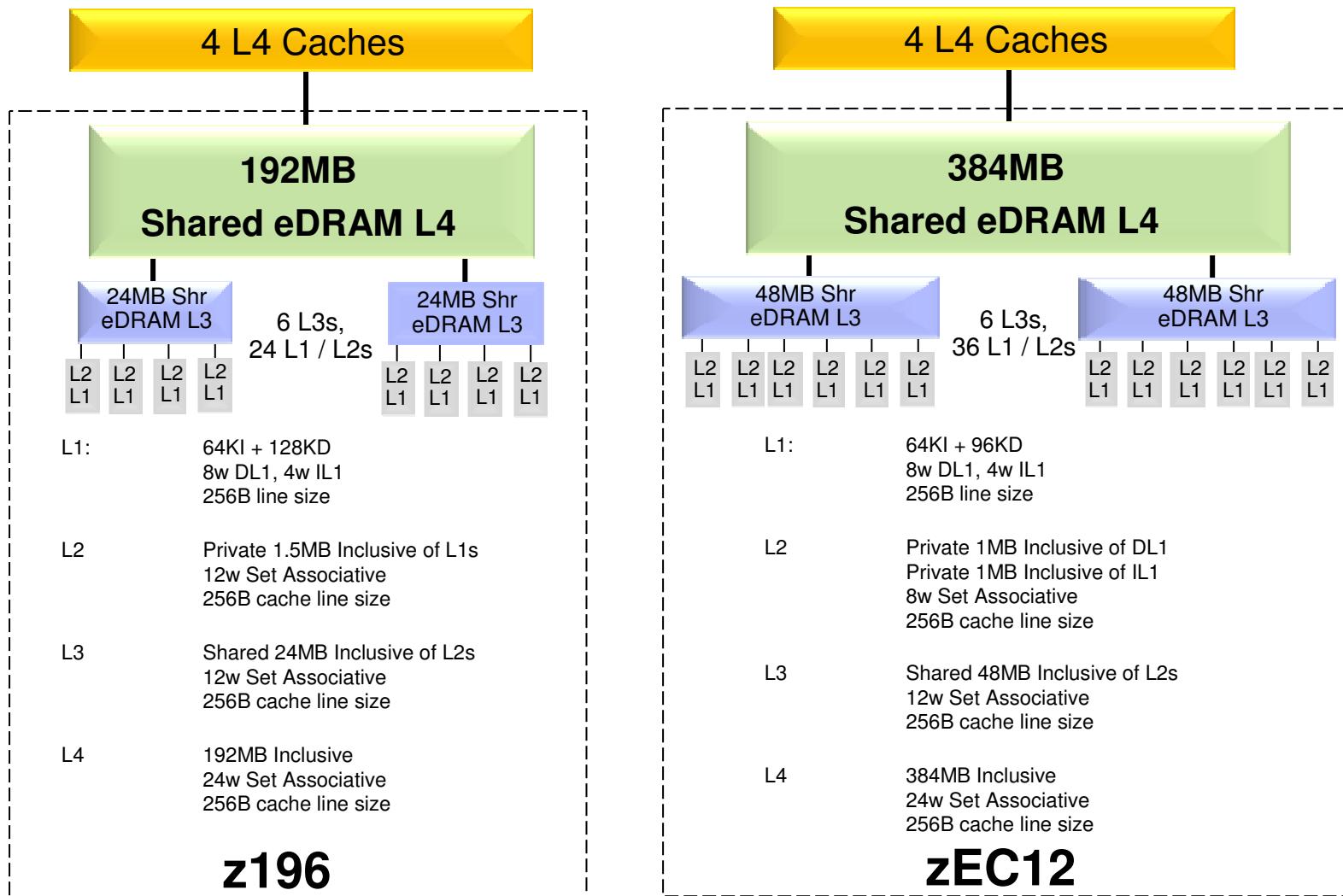
zEC12 36 PU MCM Structure



zEC12 Book Level Cache Hierarchy



System z Cache Topology – z196 vs. zEC12 Comparison



Hypervisor and OS Basics

▪ Hypervisor (PR/SM)

- Virtualization layer at OS level
- Distributes physical resources
 - Memory
 - Processors
 - Logicals dispatched on physicals
 - Dedicated
 - Shared
 - Affinities

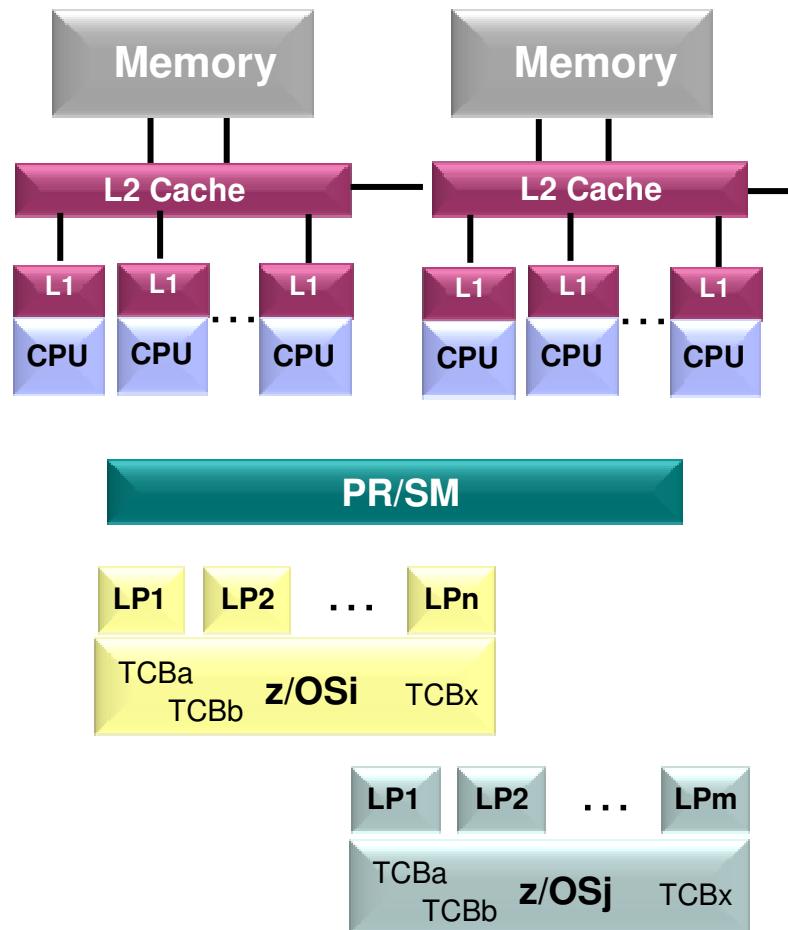
▪ OS

- Virtualization layer at address space level
- Distributes logical resources
 - Memory
 - Processors
 - Tasks dispatched on logicals

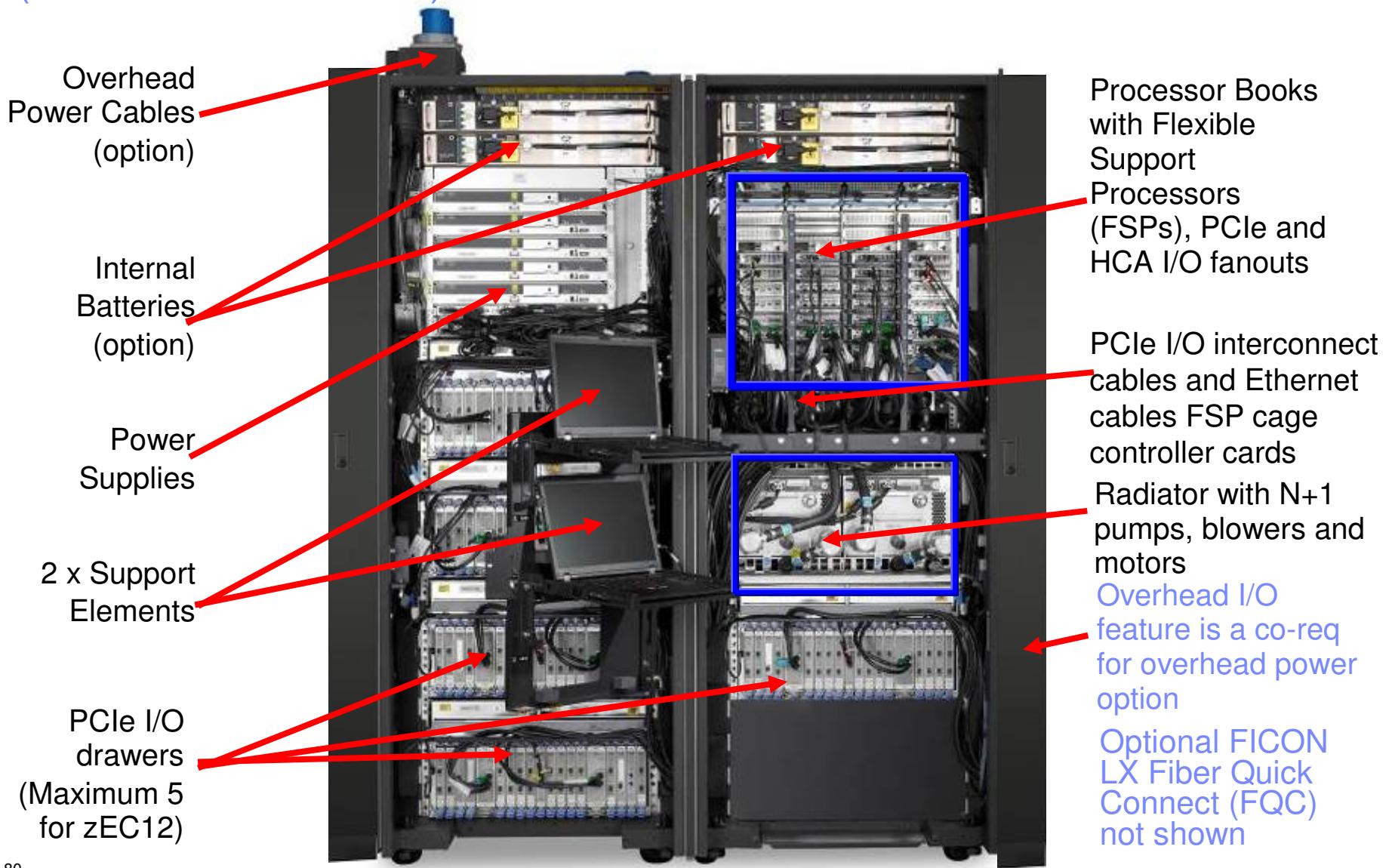
▪ Enhanced cooperation

- HiperDispatch with z10 EC
 - z/OS + PR/SM

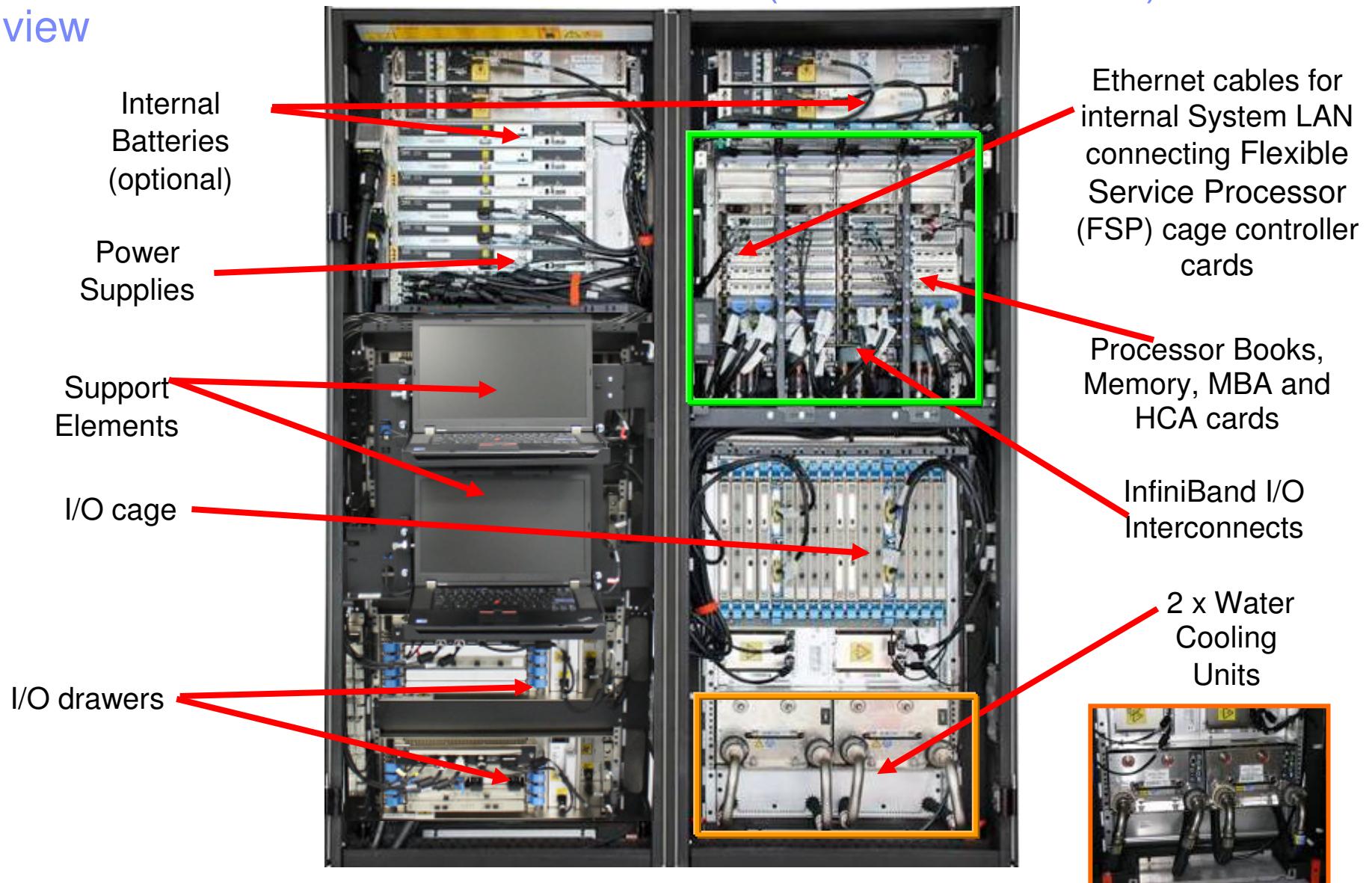
Logical View of 2 books



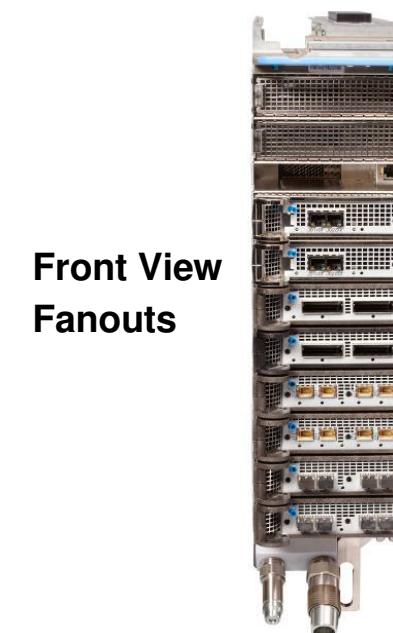
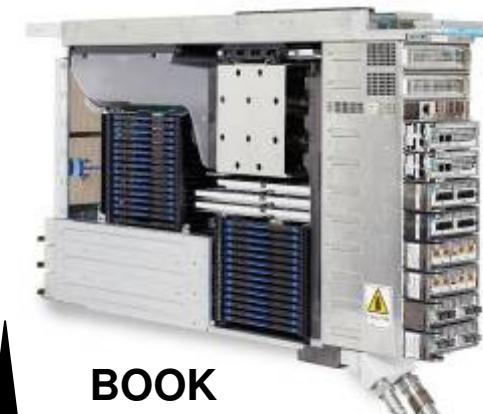
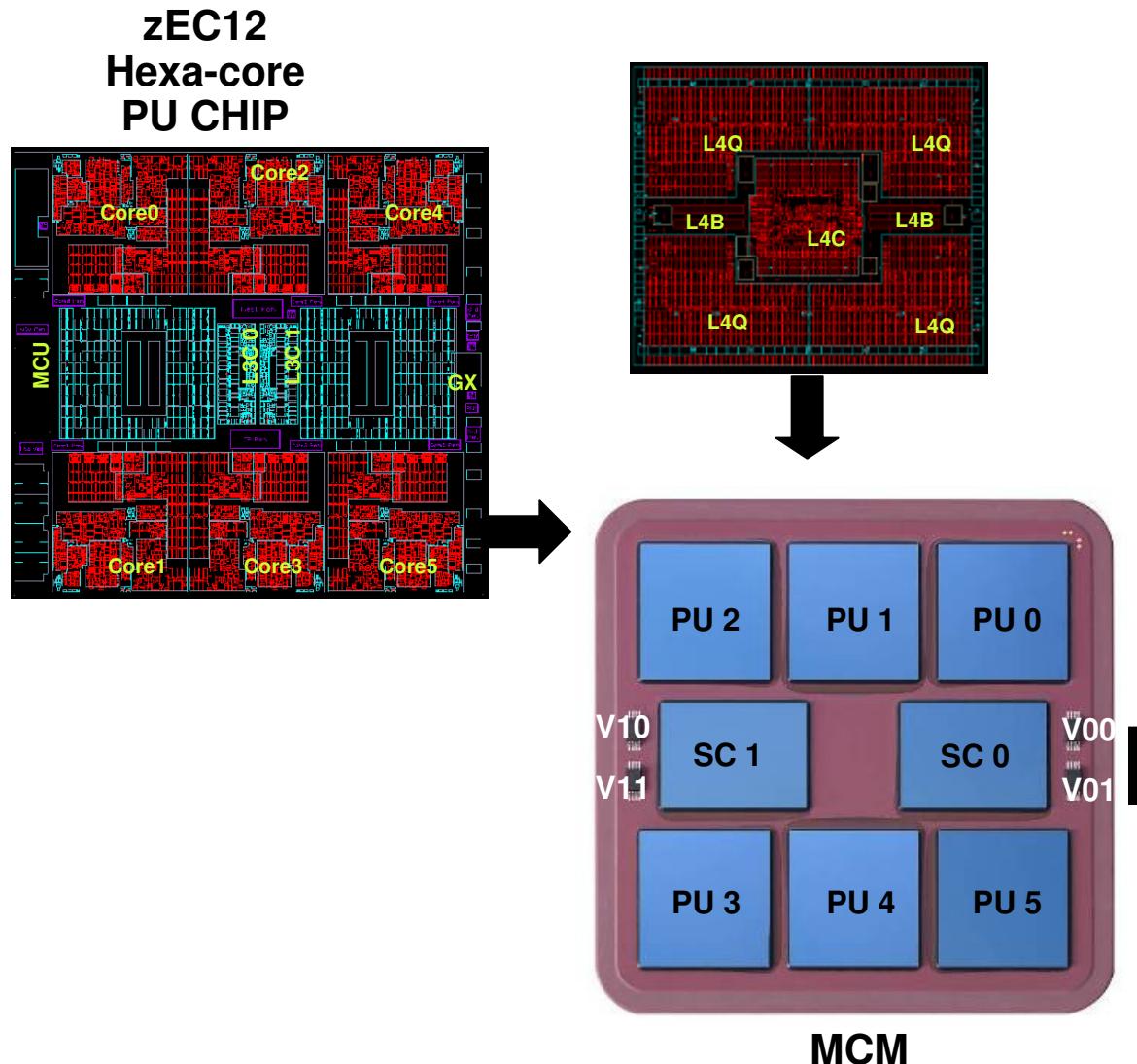
zEC12 New Build Radiator-based Air cooled – Under the covers (Model H89 and HA1) Front view



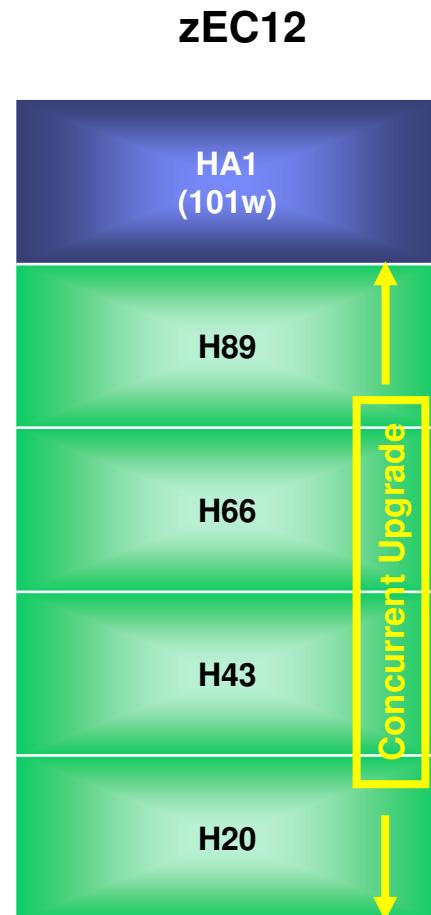
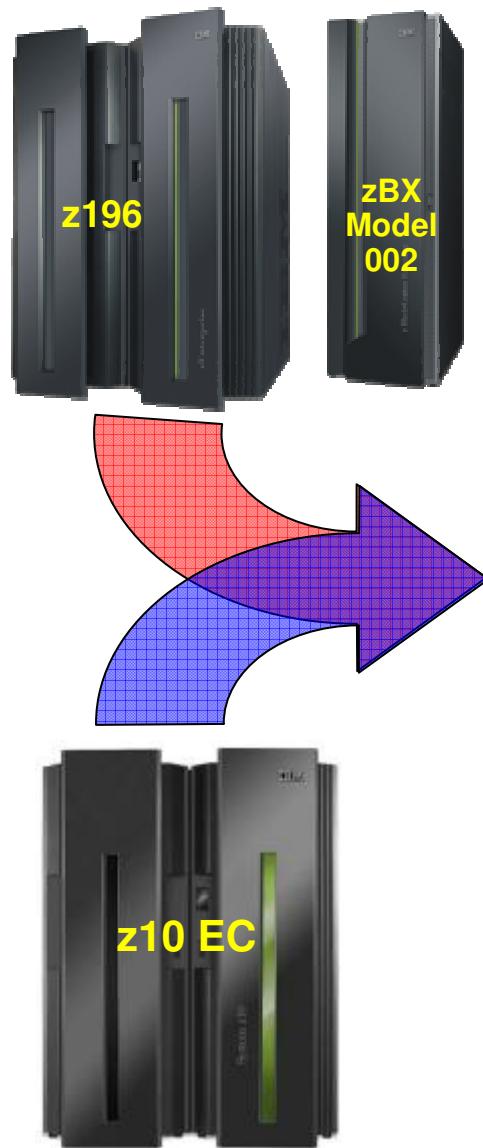
z196 Water cooled – Under the covers (Model M66 or M80) front view



zEC12 PU chip, SC chip and MCM

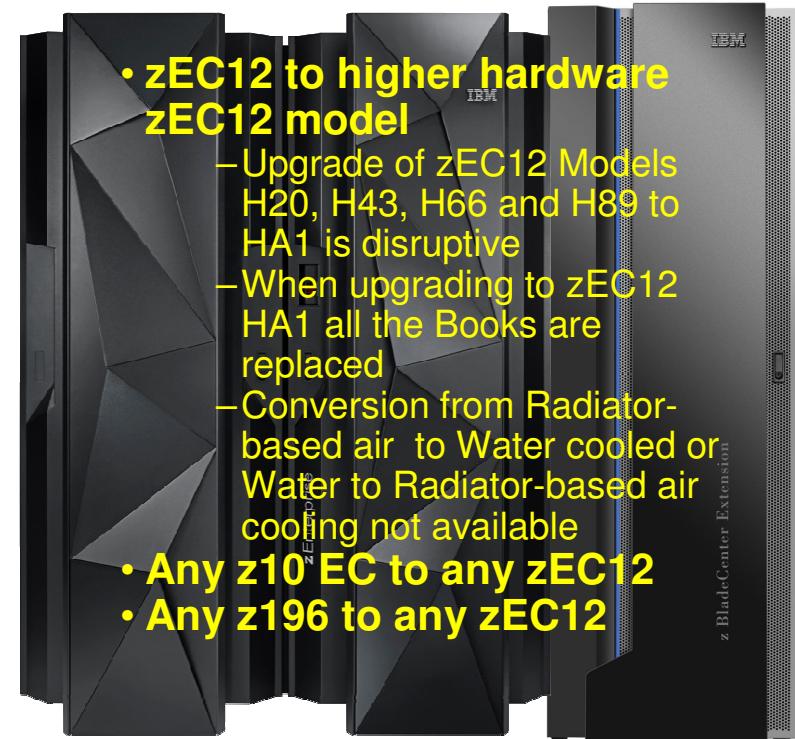


zEC12 Upgrades



zEC12

zBX Model 003



- **When a z196 with a zBX Model 002 is upgraded to zEC12, the zBX is converted to a Model 003. Additional planning required and conditions apply**

zEC12

Book Concept



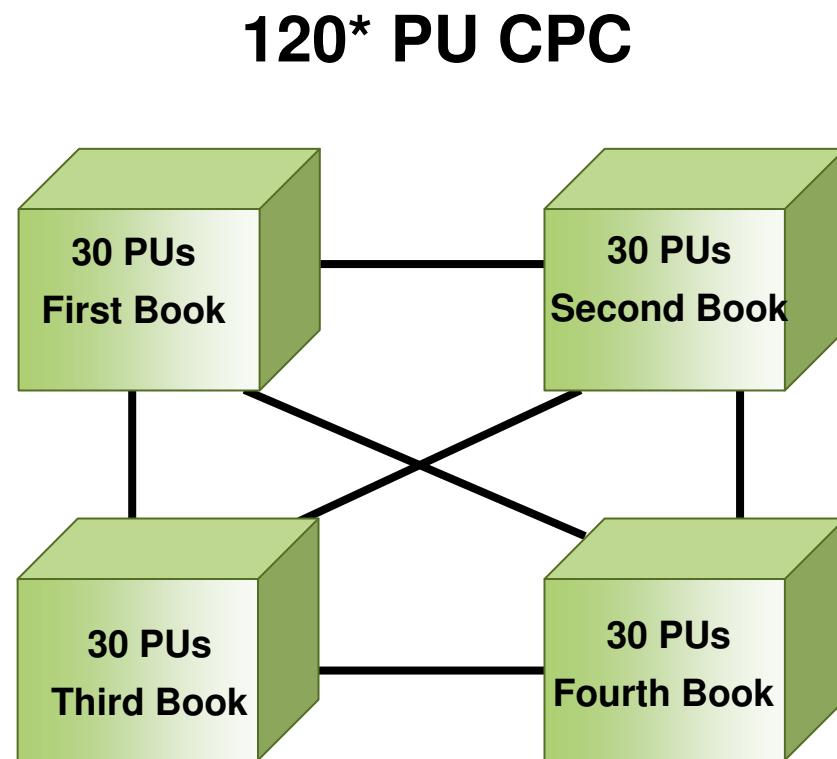
Book design

- A z196 system has up to four books on a fully connected topology, up to 80 processor units can be characterized, and up to 3 TB of memory capacity. Memory has up to 12 memory controllers, using 5-channel redundant array of independent memory (RAIM) protection, with DIMM bus cyclic redundancy check (CRC) error retry. The 4-level cache hierarchy is implemented with eDRAM (embedded) caches. Up until recently eDRAM was considered to be too slow for this kind of use, however, a break-through in IBM technology has negated that. In addition eDRAM offers higher density, less power utilization, fewer soft-errors, and better performance. Concurrent maintenance allows dynamic book add and repair.
- The z196 server uses 45nm chip technology, with advancing low latency pipeline design, leveraging high speed yet power efficient circuit designs. The multichip module (MCM) has a dense packaging, allowing modular refrigeration units (MRUs) cooling, or as an option, water cooling. The water cooling option is recommended as it can lower the total power consumption of the server.



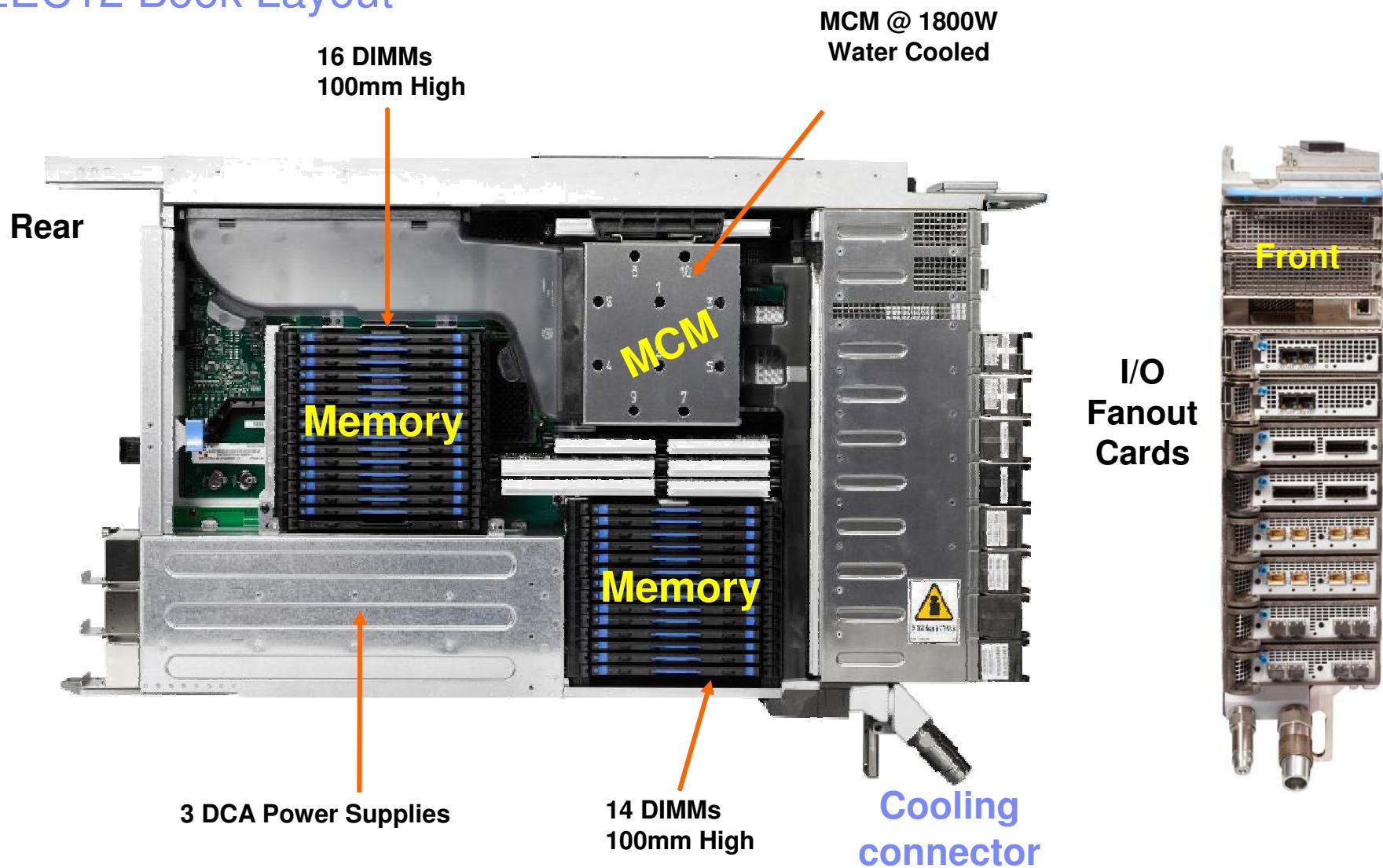
zEC12 – Inter Book Communications – Model HA1

- The zEC12 Books are fully interconnected in a point-to-point topology as shown in the diagram
- Data transfers are direct between Books via the Level 4 Cache chip in each MCM.
- Level 4 Cache is shared by all PU chips on the MCM



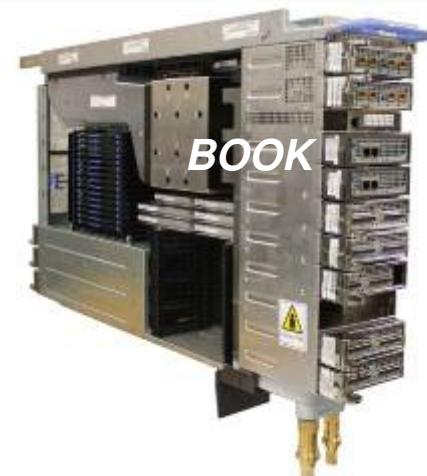
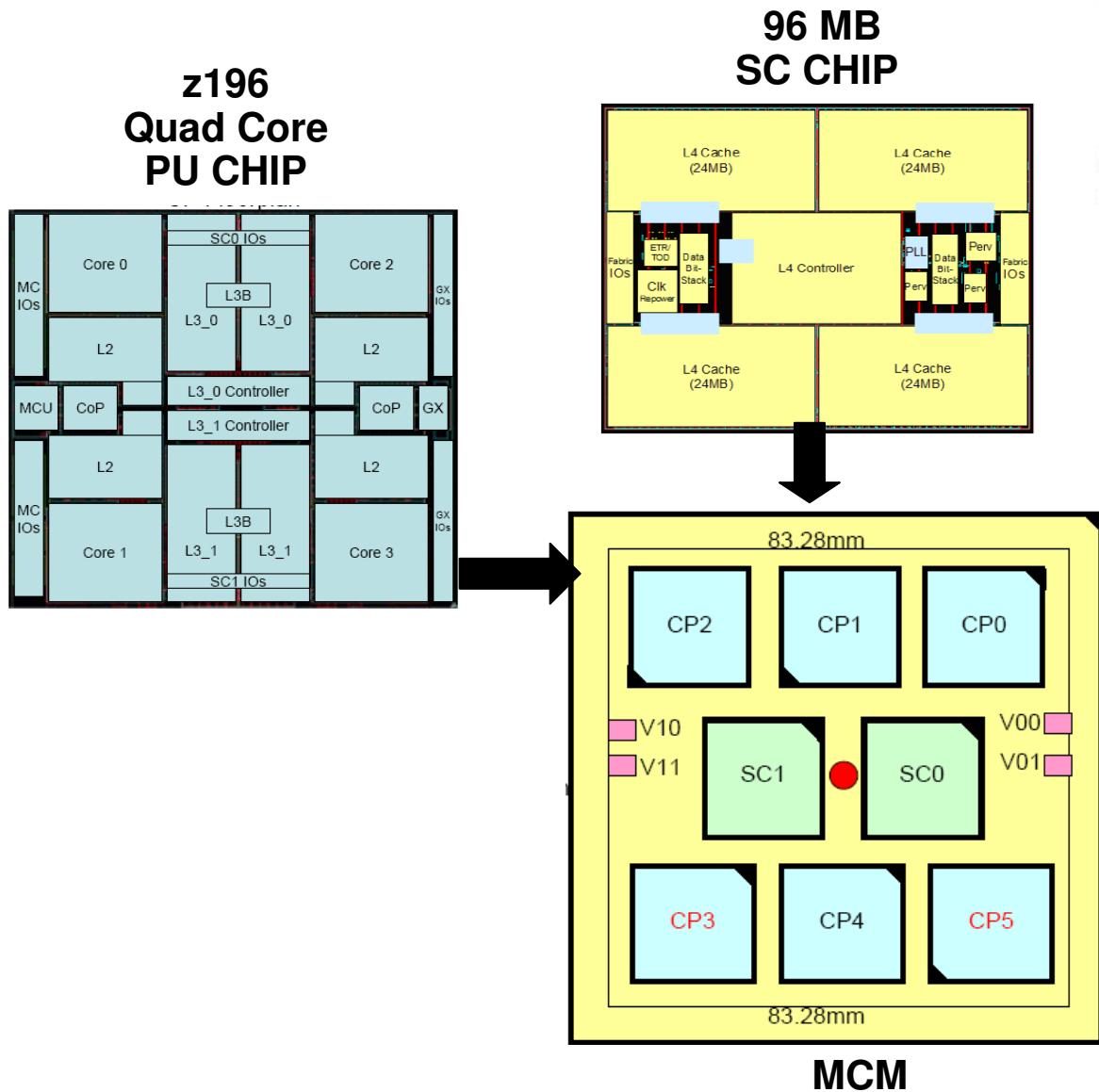
* Of the maximum 144 PUs only 120 are used

zEC12 Book Layout



Note: Unlike the z196, zEC12 Books are the same for the Radiator based Air and Water cooled Systems

z196 PU chip, SC chip and MCM

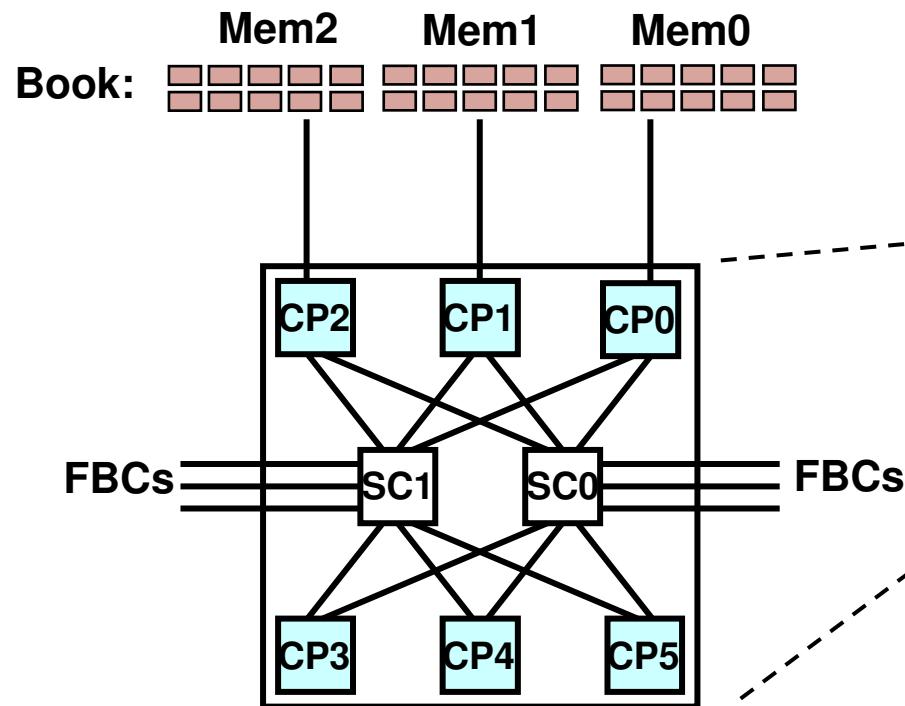


Front View



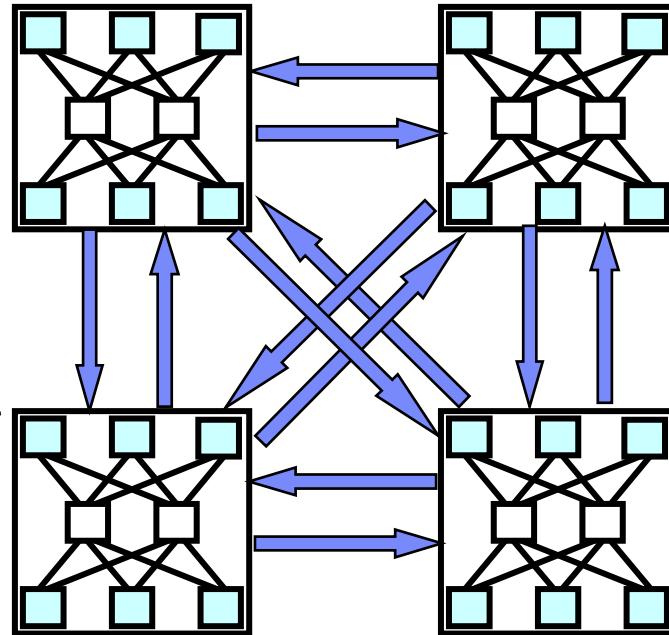
Front View
Fanouts

zEC12 Cache / Book Topology



* Of the maximum 144 PUs only 120 are used

Fully connected 4 Book system:



- **120* total cores**
- **Total system cache**
 - 1536 MB shared L4 (eDRAM)
 - 576 MB L3 (eDRAM)
 - 144 MB L2 private (SRAM)
 - 19.5 MB L1 private (SRAM)

Enhanced book availability

Book Add

- Model Upgrade by the addition of a single new book adding physical processors, memory, and I/O Connections.

Continued Capacity with Fenced Book

- Make use of the LICCC defined resources of the fenced book to allocate physical resources on the operational books as possible.

Book Repair

- Replacement of a defective book when that book had been previously fenced from the system during the last IML.

Book Replacement

- Removal and replacement of a book for either repair or upgrade

zEC12

Processor Unit Design



System z Servers Continue to Scale with zEC12

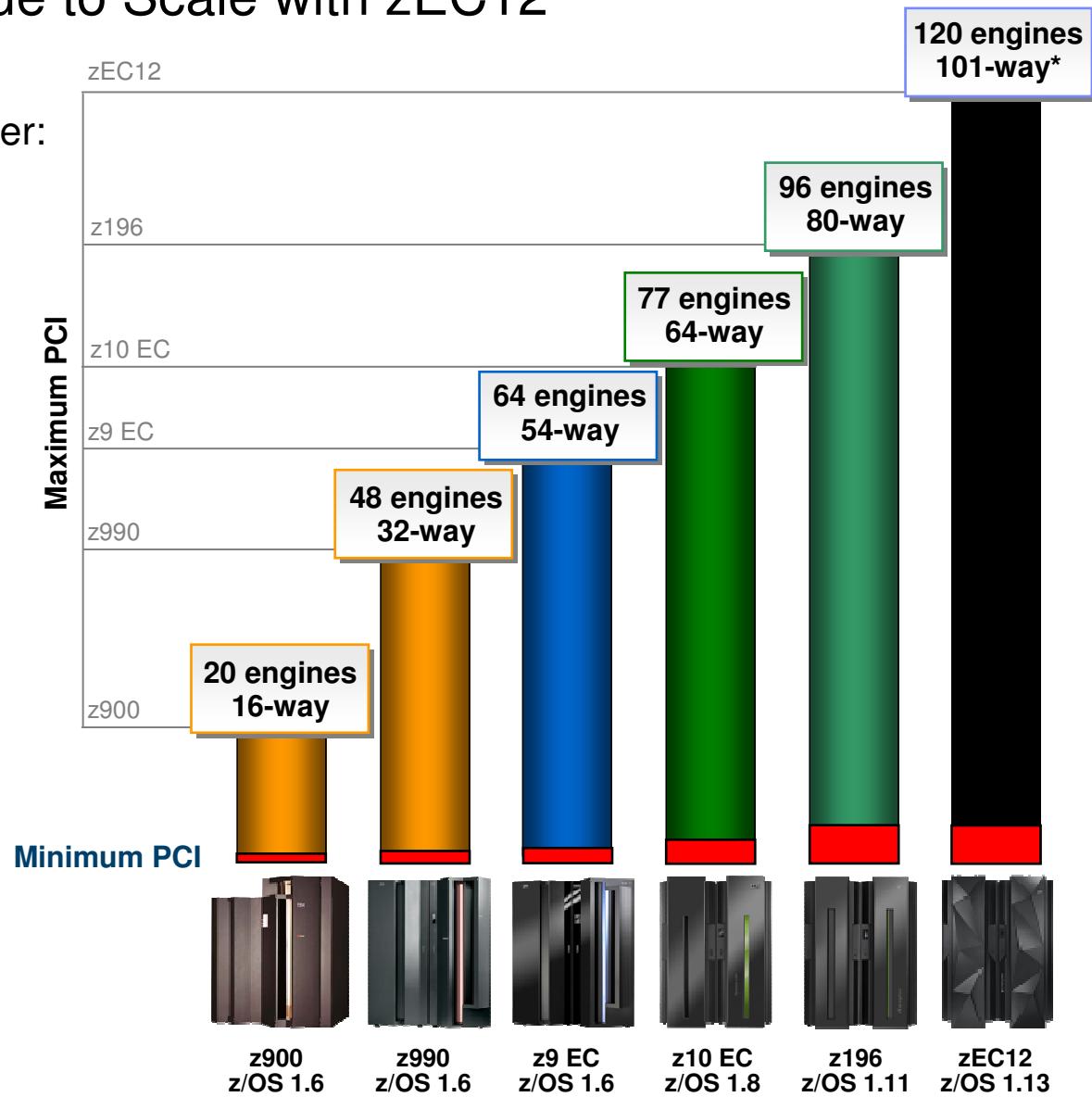
Each new range continues to deliver:

- New function
- Unprecedented capacity to meet consolidation needs
- Improved efficiency to further reduce energy consumption
- Continues to delivering flexible and simplified on demand capacity
- A mainframe that goes beyond the traditional paradigm

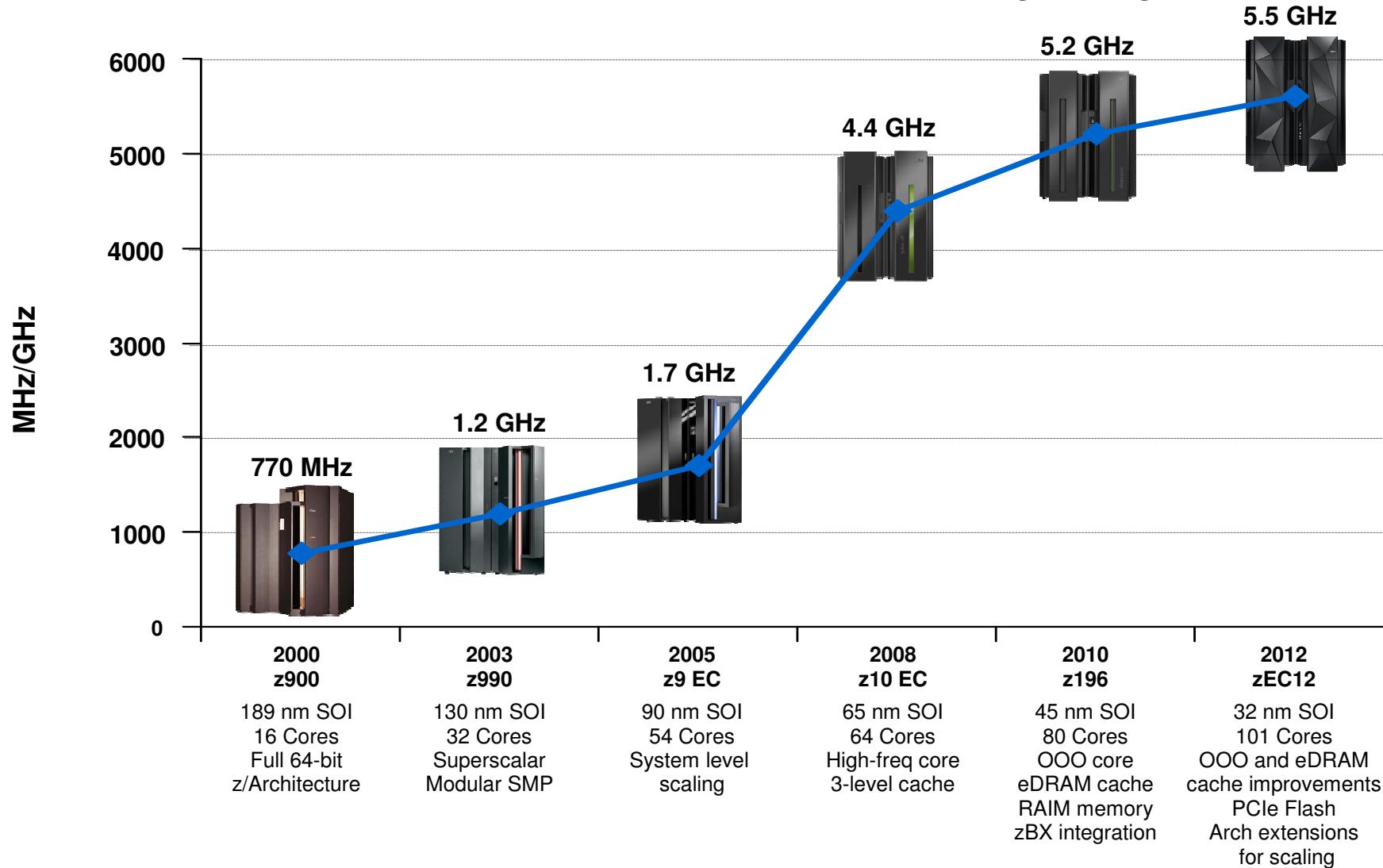


PCI - Processor Capacity Index

*z/OS supports up to a 100-way only



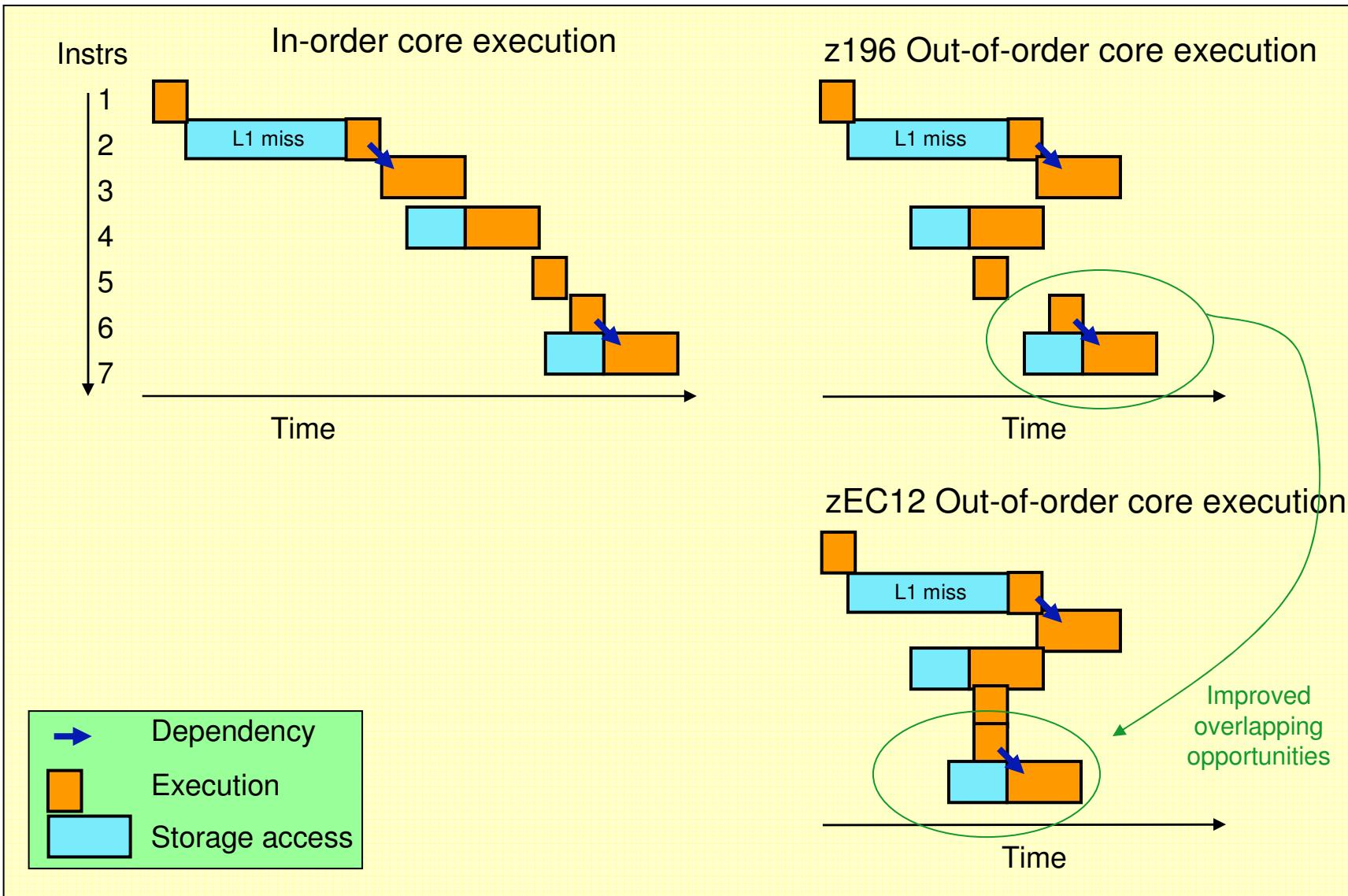
zEC12 Continues the CMOS Mainframe Heritage Begun in 1994



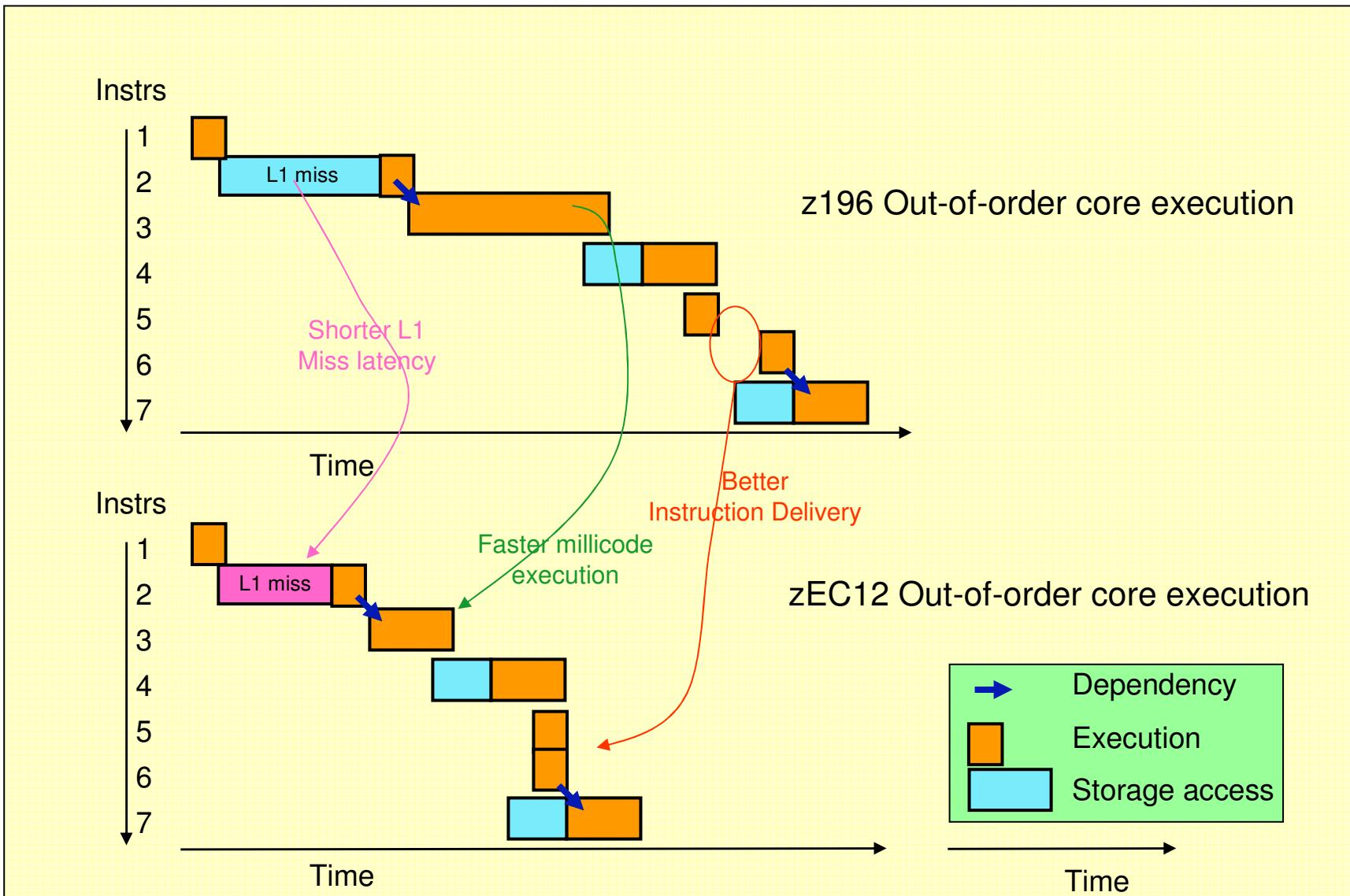
z196 GHz Leadership

- **Mainframe continues to grow frequency by**
 - Leveraging 45nm technology
 - Advancing low latency pipeline design
 - Leveraging high speed yet power-efficient circuit designs
- **z196 achieves industry leadership 5.2 GHz operation**
- **High-frequency processor design is enabled by**
 - Innovative power-efficient circuit designs
 - IBM's SOI silicon technology
 - Leadership packaging technology including glass-ceramic MCMs
 - Leadership cooling technology, with choice of MRU or chilled-water cooling
- **GHz is especially important for CPU-intensive applications**
- **System performance is not linear with frequency**
 - Need to use LSPR + Mainframe capacity planning tools for real client / workload sizing
- **GHz is not the only dimension that matters**
 - Must balance frequency, pipeline efficiency, energy efficiency, cache/memory design, I/O design

Out of Order Execution – z196 Vs zEC12



zEC12 OoO - Improved instruction delivery and execution



Superscalar processor

A scalar processor is a processor that is based on a single-issue architecture, which means that only a single instruction is executed at a time. A superscalar processor allows **concurrent execution of instructions** by adding additional resources onto the microprocessor to achieve more parallelism by creating multiple pipelines, each working on its own set of instructions.

A superscalar processor is based on a **multi-issue architecture**. In such a processor, where **multiple instructions can be executed at each cycle**, a higher level of **complexity** is reached, because an operation in one pipeline stage might depend on data in another pipeline stage. Therefore, a superscalar design demands careful consideration of which instruction sequences can successfully operate in a long pipeline environment.

On the z196, **up to three instructions can be decoded per cycle** and **up to five instructions/operations can be executed per cycle**. Execution can occur out of (program) order.

If the **branch prediction logic** of the microprocessor makes the wrong prediction, removing all instructions in the parallel pipelines also might be necessary. Obviously, the cost of the wrong branch prediction is more costly in a high-frequency processor design. For this reason, a variety of history-based branch prediction mechanisms are used.

The branch target buffer (**BTB**) runs ahead of instruction cache pre-fetches to prevent branch misses in an early stage. Furthermore, a branch history table (**BHT**) in combination with a pattern history table (**PHT**) and the use of tagged multi-target prediction technology branch prediction offer an extremely high branch prediction success rate.

Branch prediction

Because of the ultra high frequency of the PUs, the penalty for a wrongly predicted branch is high. For that reason a multi-pronged strategy for branch prediction, based on gathered branch history combined with several other prediction mechanisms, is implemented on each microprocessor. The branch history table (BHT) implementation on processors has a large performance improvement effect. Originally introduced on the IBM ES/9000 9021 in 1990, the BHT has been continuously improved.

The BHT offers significant branch performance benefits. The BHT allows each PU to take instruction branches based on a stored BHT, which improves processing times for calculation routines. Besides the BHT, the z196 uses a variety of techniques to improve the prediction of the correct branch to be executed. The techniques include:

- Branch history table (BHT)
- Branch target buffer (BTB)
- Pattern history table (PHT)
- BTB data compression

The success rate of branch prediction contributes significantly to the superscalar aspects of the z196. This is because the architecture rules prescribe that, for successful parallel execution of an instruction stream, the correctly predicted result of the branch is essential.

Wild branch

When a bad pointer is used or when code overlays a data area containing a pointer to code, a random branch is the result, causing a 0C1 or 0C4 abend. Random branches are very hard to diagnose because clues about how the system got there are not evident. With the **wild branch hardware facility, the last address from which a successful branch instruction was executed is kept**. z/OS uses this information in conjunction with **debugging aids**, such as the **SLIP command**, to determine where a wild branch came from and might collect data from that storage location. This approach decreases the many debugging steps necessary when looking for where the branch came from.

IEEE floating point

Over 130 binary and hexadecimal floating-point instructions are present in z196. They incorporate **IEEE Standards** into the platform.

Translation look-aside buffer

The translation look-aside buffer (TLB) in the instruction and data L1 caches use a secondary TLB to **enhance performance**. In addition, a translator unit is added to translate misses in the secondary TLB.

Instruction fetching, decode, and grouping

The superscalar design of the microprocessor allows for the decoding of up to three instructions per cycle and the execution of up to five instructions per cycle. Both **execution** and **storage accesses** for instruction and **operand fetching** can occur out of sequence.

Extended translation facility

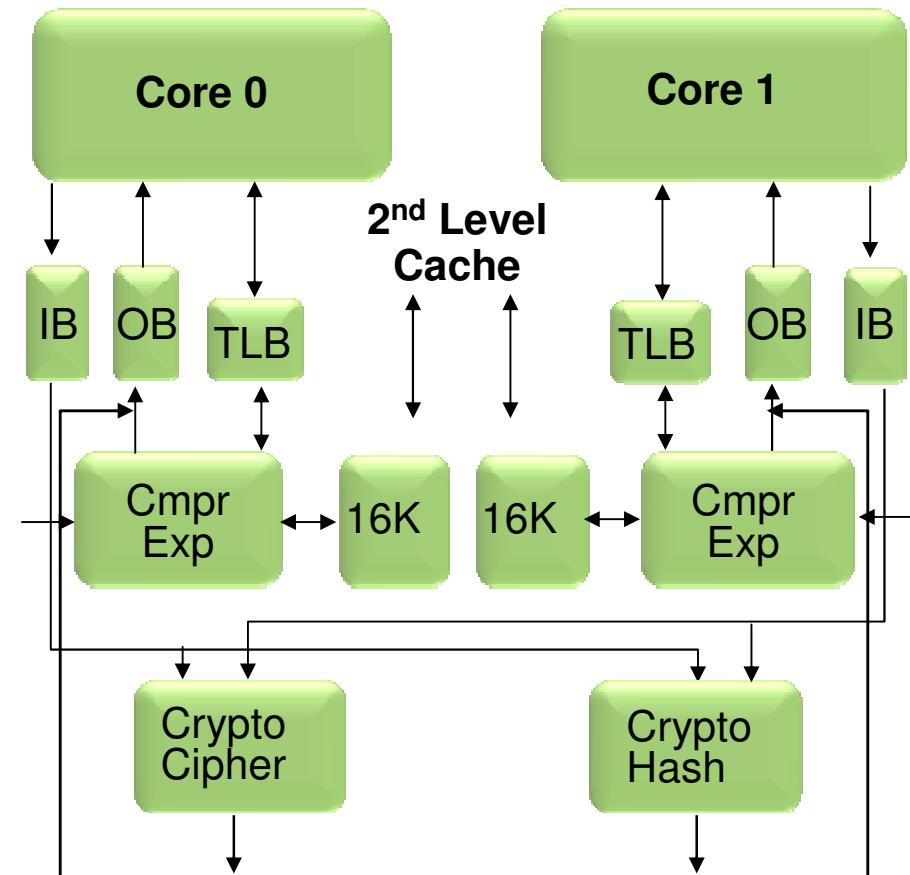
Used in data conversion operations for data encoded in **Unicode**, causing applications that are enabled for Unicode or globalization to be more efficient. These data-encoding formats are used in **Web services**, **grid**, and on-demand environments where **XML** and **SOAP** technologies are used.

Instruction set extensions

Hexadecimal floating point, Immediate, Load, Cryptographic, Extended Translate Facility-3 and Assist instructions,

z196 Compression and Cryptography Accelerator

- **Data compression engine**
 - Static dictionary compression and expansion
 - Dictionary size up to 64KB (8K entries)
 - Local 16KB cache per core for dictionary data
- **CP Assist for Cryptographic Function (CPACF)**
 - Enhancements for new NIST standard
 - Complemented prior ECB and CBC **symmetric** cipher modes with XTS, OFB, CTR, CFB, CMAC and CCM
 - New primitives (128b Galois Field multiply) for GCM
- **Accelerator unit shared by 2 cores**
 - Independent compression engines
 - Shared cryptography engines



Decimal floating point accelerator

The decimal floating point (DFP) accelerator function is present on each of the microprocessors (cores) on the quad-core chip. Its implementation meets business **application** requirements for **better performance, precision, and function**.

Base 10 arithmetic is used for most business and financial computation. Floating point computation that is used for work typically done in decimal arithmetic has involved frequent necessary data conversions and approximation to represent decimal numbers. This has made floating point arithmetic complex and error-prone for programmers using it for applications in which the data is typically decimal data.

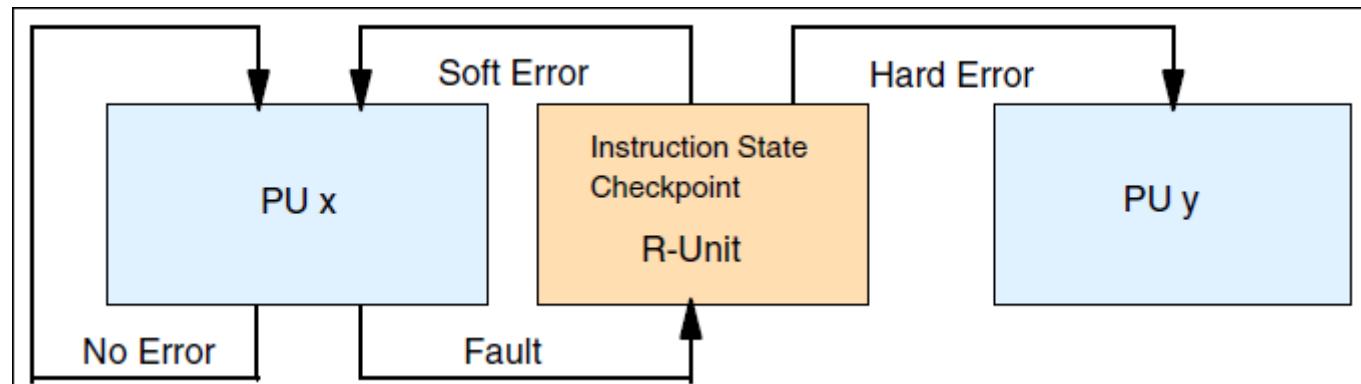
Benefits

- **Avoids** rounding issues such as those happening with **binary-to-decimal conversions**.
- Has better functionality over existing binary coded decimal (BCD) operations.
- Follows the standardization of the dominant decimal data and decimal operations in commercial computing supporting **industry standardization** (IEEE 745R) of decimal floating point operations. Instructions are added in support of the Draft Standard for Floating-Point Arithmetic, which is intended to supersede the ANSI/IEEE Std 754-1985.

Processor error detection and recovery

The PU uses something called transient recovery as an error recovery mechanism.

When an error is detected, the instruction unit retries the instruction and attempts to recover the error. If the retry is not successful (that is, a **permanent fault exists**), a **relocation process** is started that restores the full capacity by moving work to another PU. Relocation under hardware control is possible because the R-unit has the full architected state in its buffer



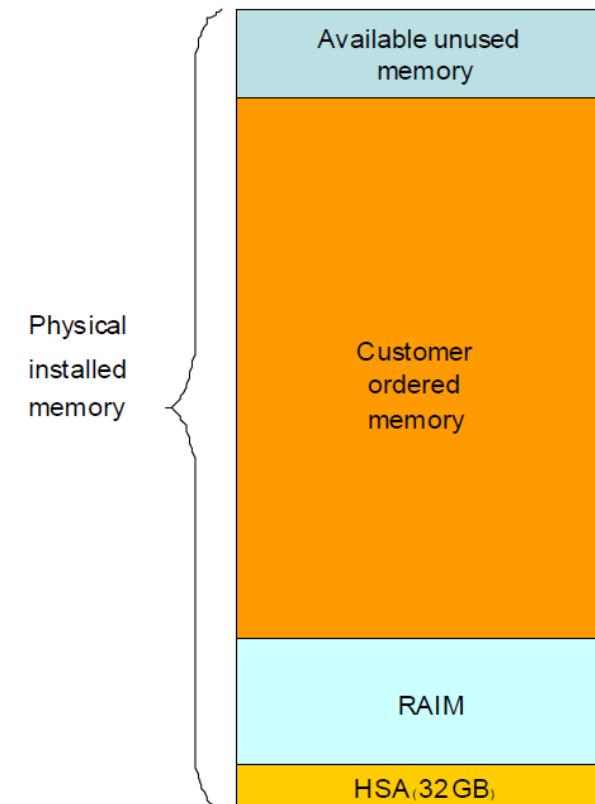
zEC12

Memory



Memory Usage and Allocation

- Customer memory allocation under the zEC12 eConfig panel will configure the most efficient configuration of memory DIMMs. Most configurations will not leave enough spare physical memory for future LICC upgrades.
- Physical memory DIMM counts in the eConfig output does not mean that additional spare physical memory is available.
 - Memory usage on zEC12 is similar to z196 in that RAIM memory accounts for 20 percent of the physical memory that is installed on the server. In addition to RAIM, zEC12 reserves 32GB for HSA usage.
- Always use eConfig to determine the amount of available physical memory. This can be done by examining the Memory Preplanned Capacity field. Customers that require future LICC memory upgrade should be configuring additional preplanned memory.



Large page support

- By default, page frames are allocated with a 4 KB size. The z196 supports a large page size of 1 MB. The first z/OS release that supports large pages is z/OS V1R9.
- The translation look-aside buffer (TLB) exists to reduce the amount of time required to translate a virtual address to a real address by dynamic address translation (DAT) when it needs to find the correct page for the correct address space.
- It is very desirable to have one's addresses in the TLB. With 4 K pages, holding all the addresses for 1 MB of storage takes **256 TLB lines**. When using 1 MB pages, it takes only **1 TLB line**. This means that large page size exploiters have a much smaller TLB footprint.

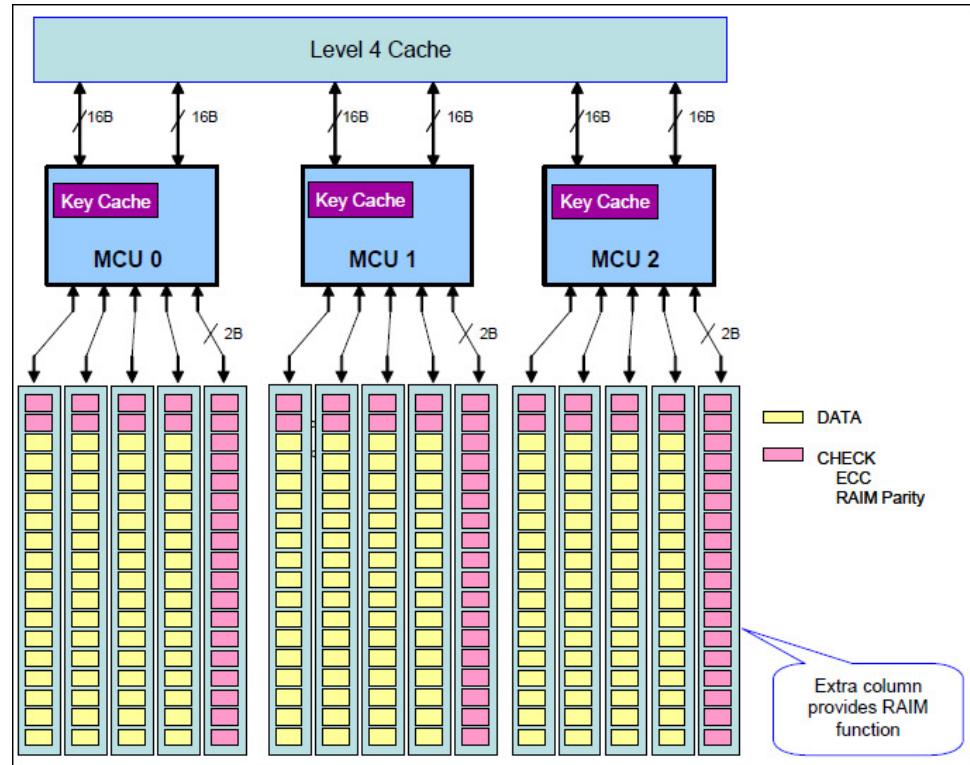
Hardware system area

- The hardware system area (HSA) is a **non-addressable** storage area that contains server Licensed Internal Code and configuration-dependent control blocks. The HSA has a fixed size of **32 GB** and is not part of the purchased memory that is ordered and installed.

z196 Redundant Array of Independent Memory (RAIM)

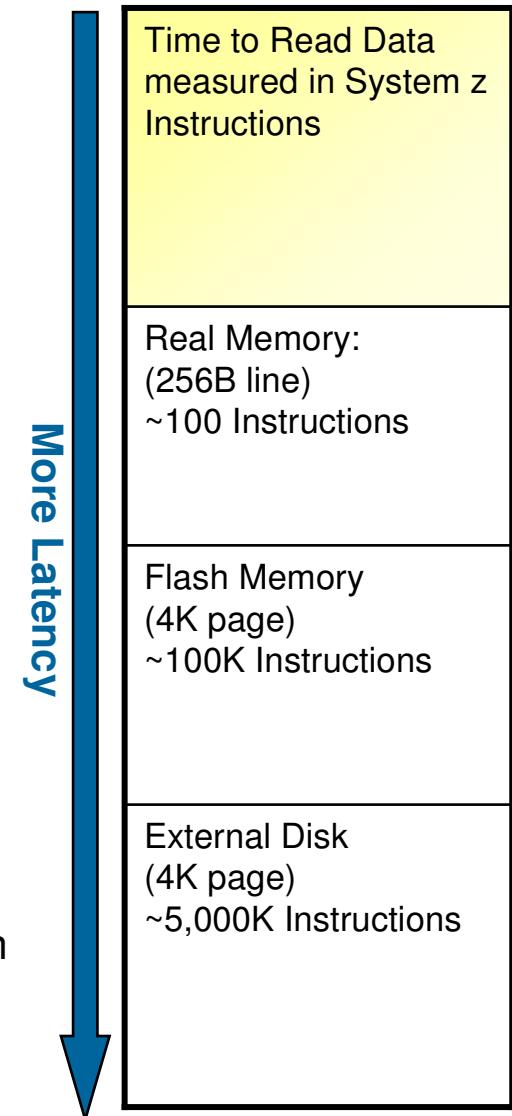
z196 introduces the redundant array of independent memory (RAIM). The RAIM design detects and recovers from DRAM, socket, memory channel or DIMM failures. The RAIM design requires the addition of one memory channel that is dedicated for RAS

- The parity of the four “data” DIMMs are stored in the DIMMs attached to the fifth memory channel. Any failure in a memory component can be detect and corrected dynamically. This design takes the RAS of the memory subsystem to another level, making it essentially a fully fault tolerant “N+1” design.

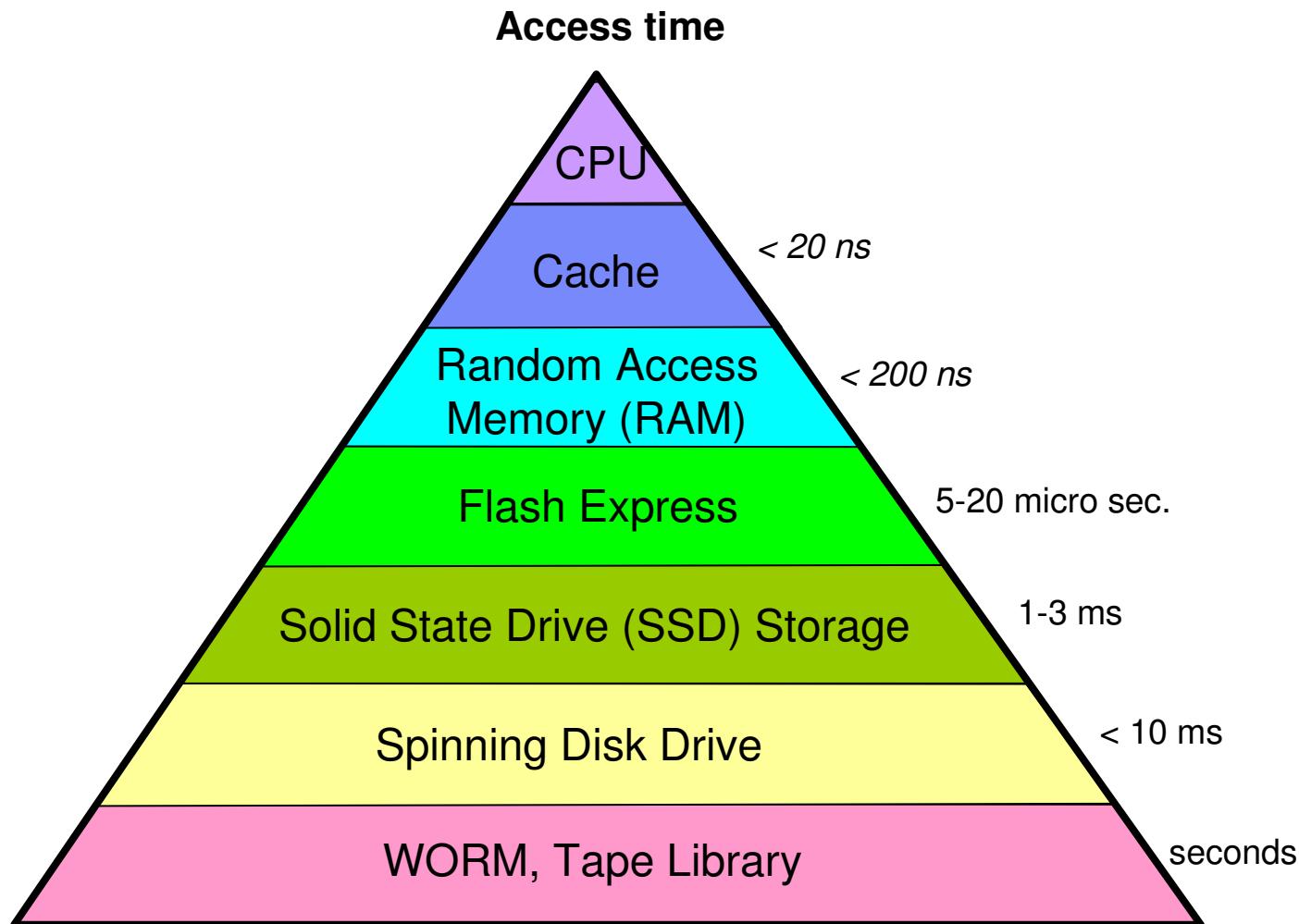


Introducing Flash Express

- Flash Express is intended to improve System z availability
 - Slash latency delays from paging
 - Flash Memory is much faster than spinning disk
 - Flash Memory is much slower than main memory
 - Flash Memory takes less power than either
 - Make your start of day processing fast
 - Designed to eliminate delays from SVC Dump processing
- zEC12 offers optional Flash Express memory cards
 - Supported in PCIe I/O drawer with other PCIe I/O cards
 - Installed in pairs for availability
 - No HCD/IOCP definitions required
- Assign Flash Memory to partitions like main memory
 - Assignment is by memory amount, not by feature
 - Each partition's Flash Memory is isolated like main memory
 - Dynamically increase the partition maximum amount of Flash
 - Dynamically configure Flash Memory into and out of the partition



Relative Access Times for different technologies

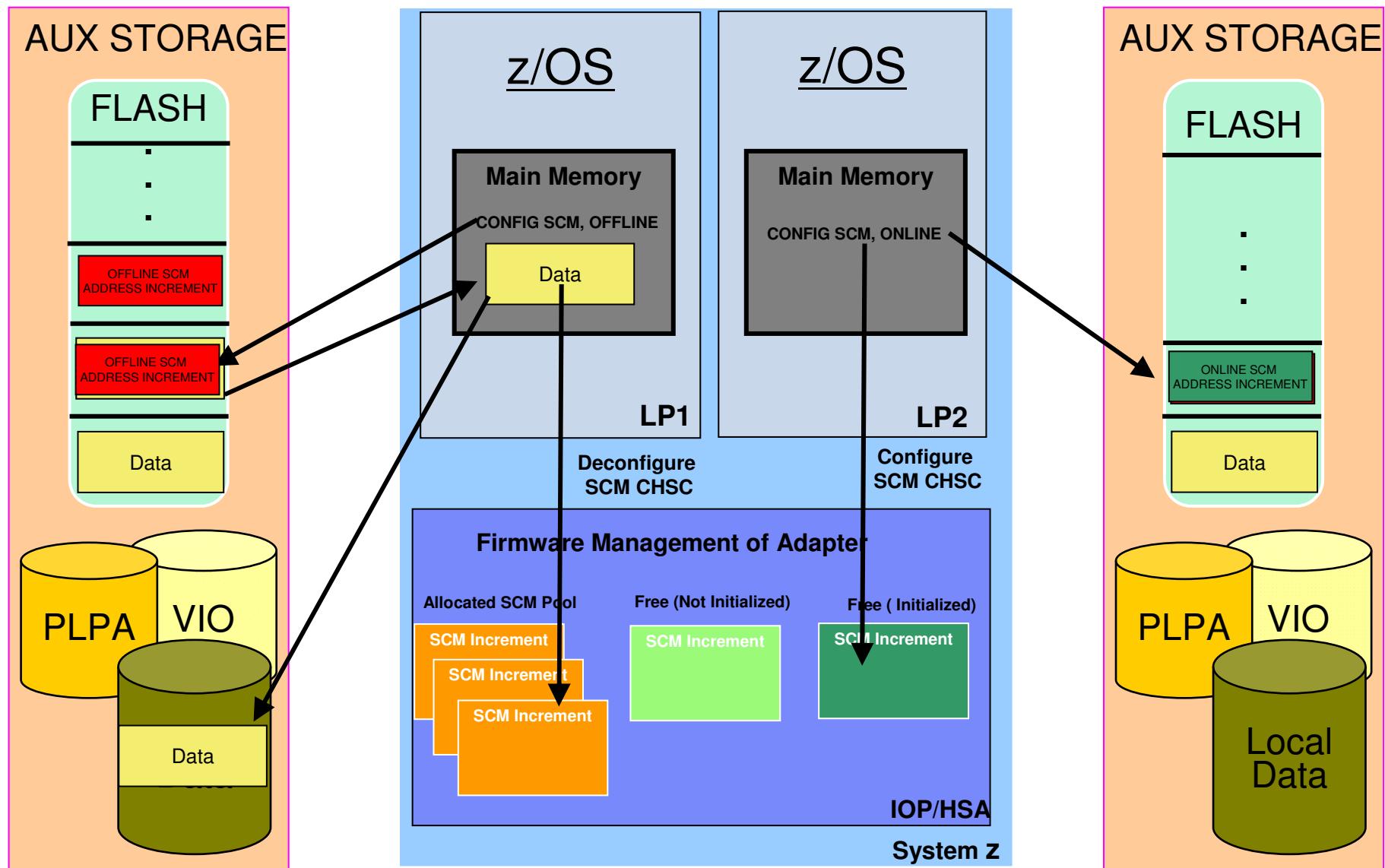


z/OS FLASH Use Cases

- **Paging**

- z/OS paging subsystem will work with mix of internal Flash and External Disk
 - Self Tuning based on measured performance
 - Improved Paging Performance, Simplified Configuration
- Begin Paging 1 MB Large Pages only to Flash
 - Exploit Flash's random I/O read rate to gain CPU performance by enabling additional use of Large Pages. Currently large pages are not pageable.
- Begin Speculative Page-In of 4K Pages
 - Exploit Flash's random I/O read rate to get Improved Resilience over Disruptions.
 - Market Open, Workload Failover,

A z/OS Flash Configuration



z196 Memory Offerings

- **Purchase Memory** – Memory available for assignment to LPARs
- **Hardware System Area** – Standard 16 GB outside customer memory for system use
- **Standard Memory** – Provides minimum physical memory required to hold base purchase memory plus 16 GB HSA
- **Flexible Memory** – Provides additional physical memory needed to support activation base customer memory and HSA on a multiple book z196 with one book out of service.
- **Plan Ahead Memory** – Provides additional physical memory needed for a concurrent upgrade (LIC CC change only) to a preplanned target customer memory

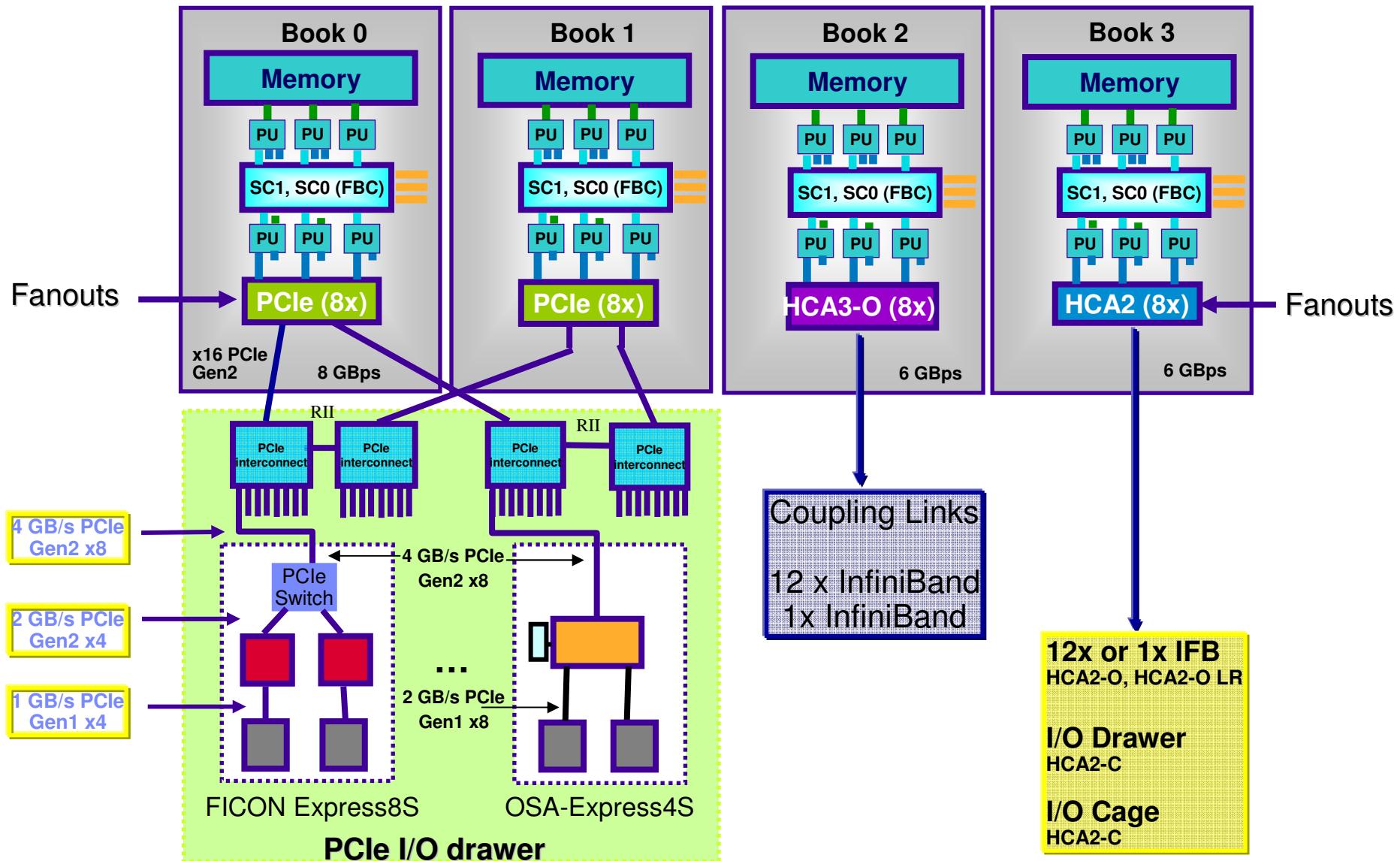
Model	Standard Memory GB	Flexible Memory GB
M15	32 - 704	NA
M32	32 - 1520	32 - 704
M49	32 - 2288	32 - 1520
M66	32 - 3056	32 - 2288
M80	32 - 3056	32 - 2288

zEC12

Connectivity



zEC12 I/O infrastructure



zEC12 Coupling Link connectivity summary

Features	Minimum # of features	Maximum # of features	Maximum connections	Increments per feature	Purchase increments
HCA3-O LR (1x)	0	16	64 links (H20: 32*)	4 links	4 links
HCA3-O (12x)	0	16	32 links (H20: 16*)	2 links	2 links
HCA2-O LR (1x) (carry forward only)	0	16 (H20-8*)	32 links (H20:16*)	2 links	2 links
HCA2-O (12x) (carry forward only)	0	16 (H20-8*)	32 links (H20:16*)	2 links	2 links
ISC-3 (carry forward only)	0	12	48 links	4 links	1 link

* Uses all available fanout slots. Allows no other I/O or coupling.

zEC12 I/O Feature Cards

Features	Offered As	Maximum # of features	Maximum channels	Increments per feature	Purchase increments
FICON					
FICON Express8S	NB	160	320 channels	2 channels	2 channels
FICON Express8	CF*	44	176 channels	4 channels	4 channels
FICON Express4 10km LX, SX	CF*	44	176 channels	4 channels	4 channels
ISC-3 Coupling	CF*	12	48 links	4 links	1 link
OSA-Express					
OSA-Express4S 10 GbE	NB	48	96 ports	1 port/1 channel	1 feature
OSA-Express4S 1 GbE OSA-Express4S 1000BASE-T**	NB	48	96 ports	2 ports/1 channel	1 feature
OSA-Express3	CF*	24	96 ports	2 (10 GbE) / 4 ports	1 feature
Crypto					
Crypto Express4S**	NB	16	16 PCIe adapters	1 PCIe adapter	1 feature ***
Crypto Express3	CF*	8	16 PCIe adapters	2 PCIe adapters	1 feature ***
Special Purpose					
Flash Express**	NB	8	8 PCIe adapters	1 PCIe adapter	2 features (shipped in pairs)

* Carry forward ONLY

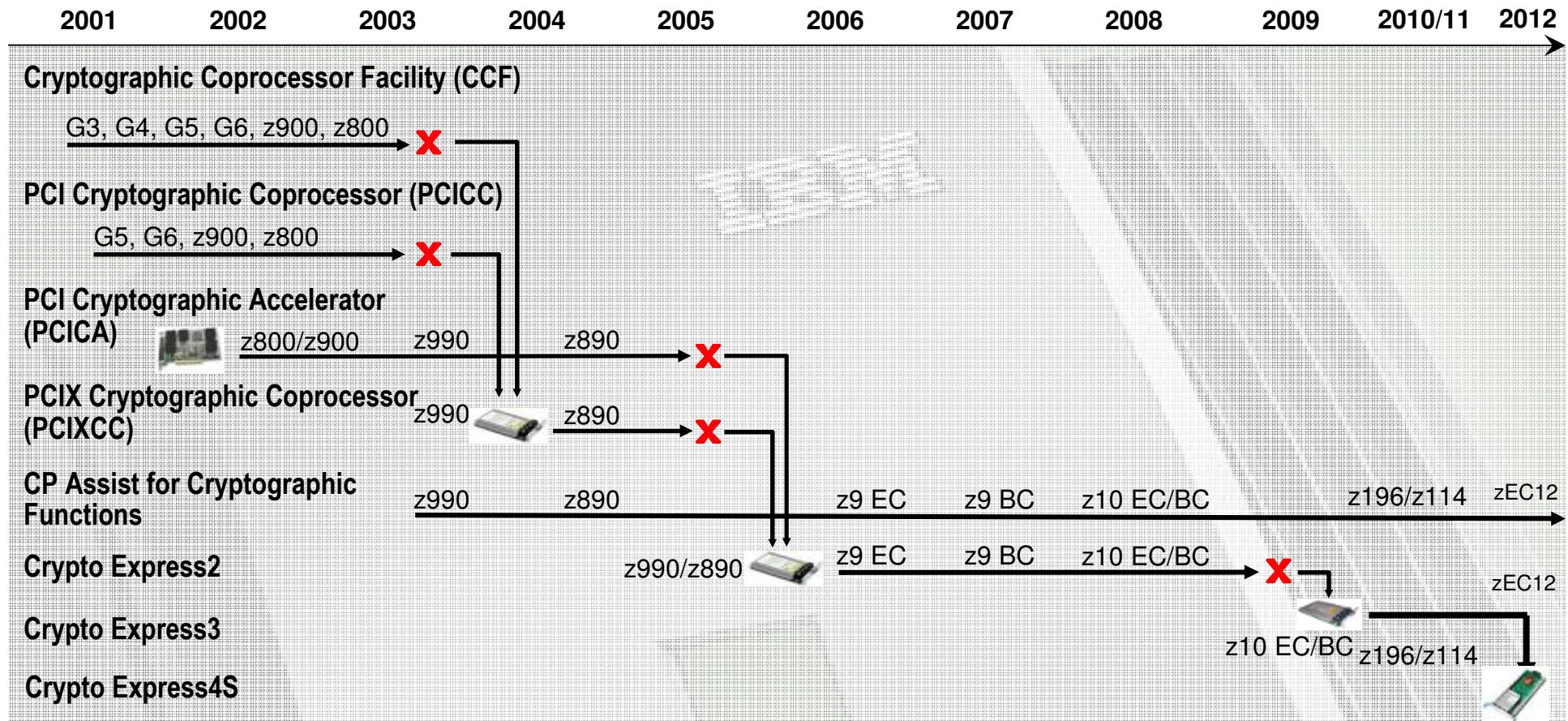
** New on zEC12

*** Two features initially, one thereafter

NB = New Build

CF = Carry Forward

System z Crypto History



- Cryptographic Coprocessor Facility – Supports “Secure key” cryptographic processing
- PCICC Feature – Supports “Secure key” cryptographic processing
- PCICA Feature – Supports “Clear key” SSL acceleration
- PCIXCC Feature – Supports “Secure key” cryptographic processing
- CP Assist for Cryptographic Function allows limited “Clear key” crypto functions from any CP/IFL
 - NOT equivalent to CCF on older machines in function or Crypto Express2 capability
- Crypto Express2 – Combines function and performance of PCICA and PCICC
- Crypto Express3 – PCIe Interface, additional processing capacity with improved RAS
- Crypto Express4S - IBM Standard PKCS #EP11

Crypto Express4S

- One PCIe adapter per feature
 - Initial order – two features
- FIPS 140-2 Level 4
- Installed in the PCIe I/O drawer
- Up to 16 features per server
- Prerequisite: CPACF (FC 3863)

- Three configuration options for the PCIe adapter
 - Only one configuration option can be chosen at any given time
 - Switching between configuration modes will erase all card secrets
 - Exception: Switching from CCA to accelerator or vice versa
- Accelerator
 - For SSL acceleration
 - Clear key RSA operations
- Enhanced: Secure IBM CCA coprocessor (default)
 - Optional: TKE workstation (FC 0841) for security-rich, flexible key entry or remote key management
- New: IBM Enterprise PKCS #11 (EP11) coprocessor
 - Designed for extended evaluations to meet public sector requirements
 - Both FIPS and Common Criteria certifications
 - **Required:** TKE workstation (FC 0841) for management of the Crypto Express4S when defined as an EP11 coprocessor
 - Supported on Crypto Express4S only



Introducing Crypto Express4S

- Latest cryptographic feature designed to complement the cryptographic functions of CPACF
- Provides state-of-the art tamper sensing and responding, programmable hardware to protect the cryptographic keys and sensitive custom applications
 - Unauthorized removal of the adapter zeroizes its content
- Suited to applications requiring high-speed security-sensitive cryptographic operations for data encryption and digital signing, and secure management and use of cryptographic keys
 - Functions targeted to Banking/Finance and Public sector
- FIPS 140-2 Level 4 hardware evaluation
- Performance of Crypto Express4S is similar to a single processor on Crypto Express3

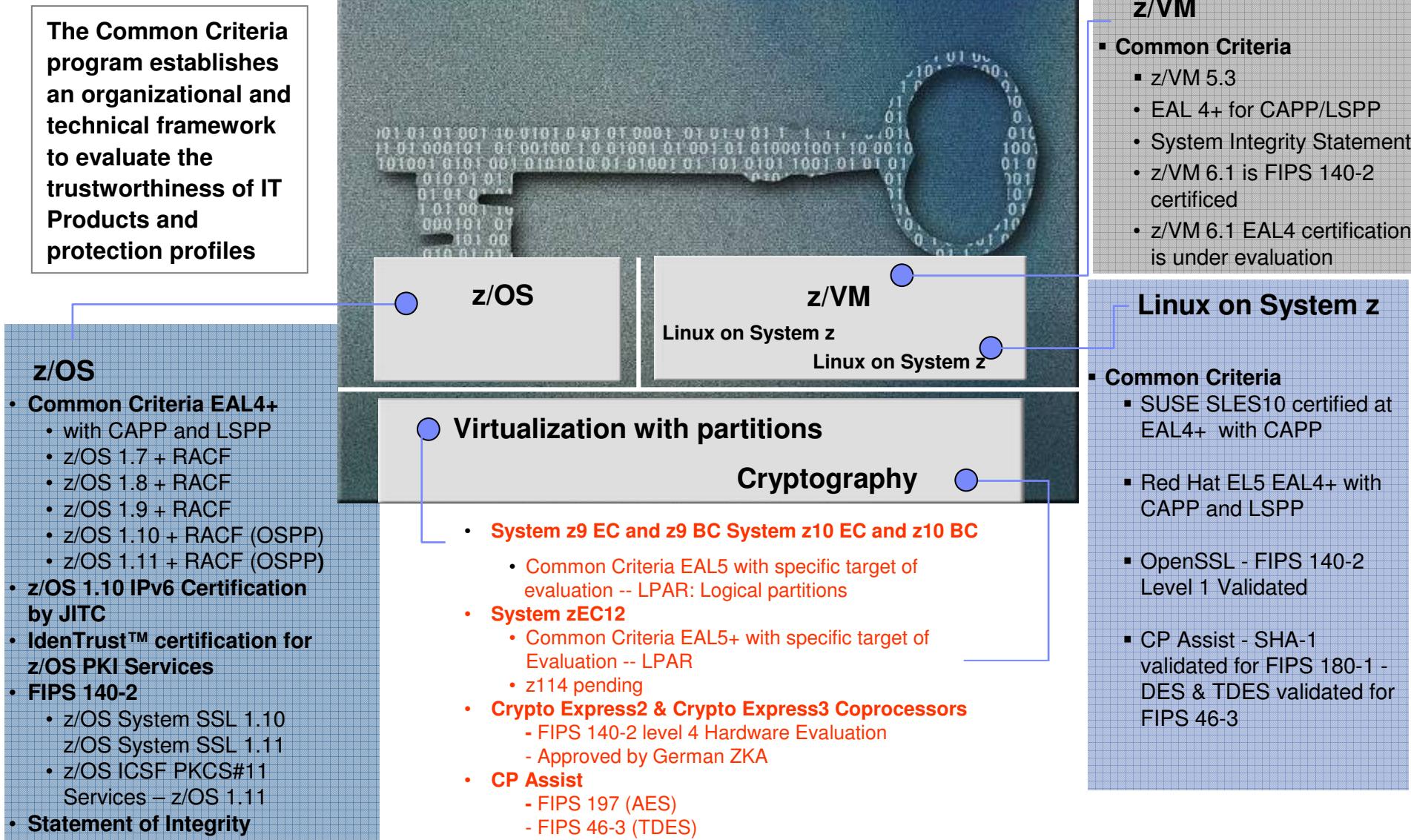
z196 New and exclusive cryptographic capabilities

- **Elliptic Curve Cryptography Digital Signature Algorithm (ECC)**, an emerging public key algorithm expected eventually to replace RSA cryptography in many applications. ECC is capable of providing digital signature functions and key agreement functions. The new CCA functions provide ECC key generation and key management and provide digital signature generation and verification functions compliance with the ECDSA method described in [ANSI X9.62 "Public Key Cryptography for the Financial Services Industry: The Elliptic Curve Digital Signature Algorithm \(ECDSA\)"](#). ECC uses keys that are shorter than RSA keys for equivalent strength-per-key-bit; RSA is impractical at key lengths with strength-per-key-bit equivalent to AES-192 and AES-256. So the strength-per-key-bit is substantially greater in an algorithm that uses elliptic curves.
- **ANSI X9.8 PIN security** which facilitates compliance with the processing requirements defined in the new version of the [ANSI X9.8 and ISO 9564 PIN Security Standards](#) and provides added security for transactions that require Personal Identification Numbers (PIN).
- **Enhanced Common Cryptographic Architecture (CCA)**, a Common Cryptographic Architecture (CCA) key token wrapping method using Cipher Block Chaining (CBC) mode in combination with other techniques to satisfy the key bundle compliance requirements in standards including [ANSI X9.24-1](#) and the recently published [Payment Card Industry Hardware Security Module \(PCI HSM\) standard](#).
- **Secure Keyed-Hash Message Authentication Code (HMAC)**, a method for computing a message authentication code using a secret key and a secure hash function. It is defined in the standard [FIPS 198, "The Keyed-Hash Message Authentication Code"](#). The new CCA functions support HMAC using SHA-1, SHA-224, SHA-256, SHA-384, and SHA-512 hash algorithms. The HMAC keys are variable-length and are securely encrypted so that their values are protected.
- **Modulus Exponent (ME) and Chinese Remainder Theorem (CRT)**, RSA encryption and decryption with key lengths greater than 2048-bits and up to 4096-bits.

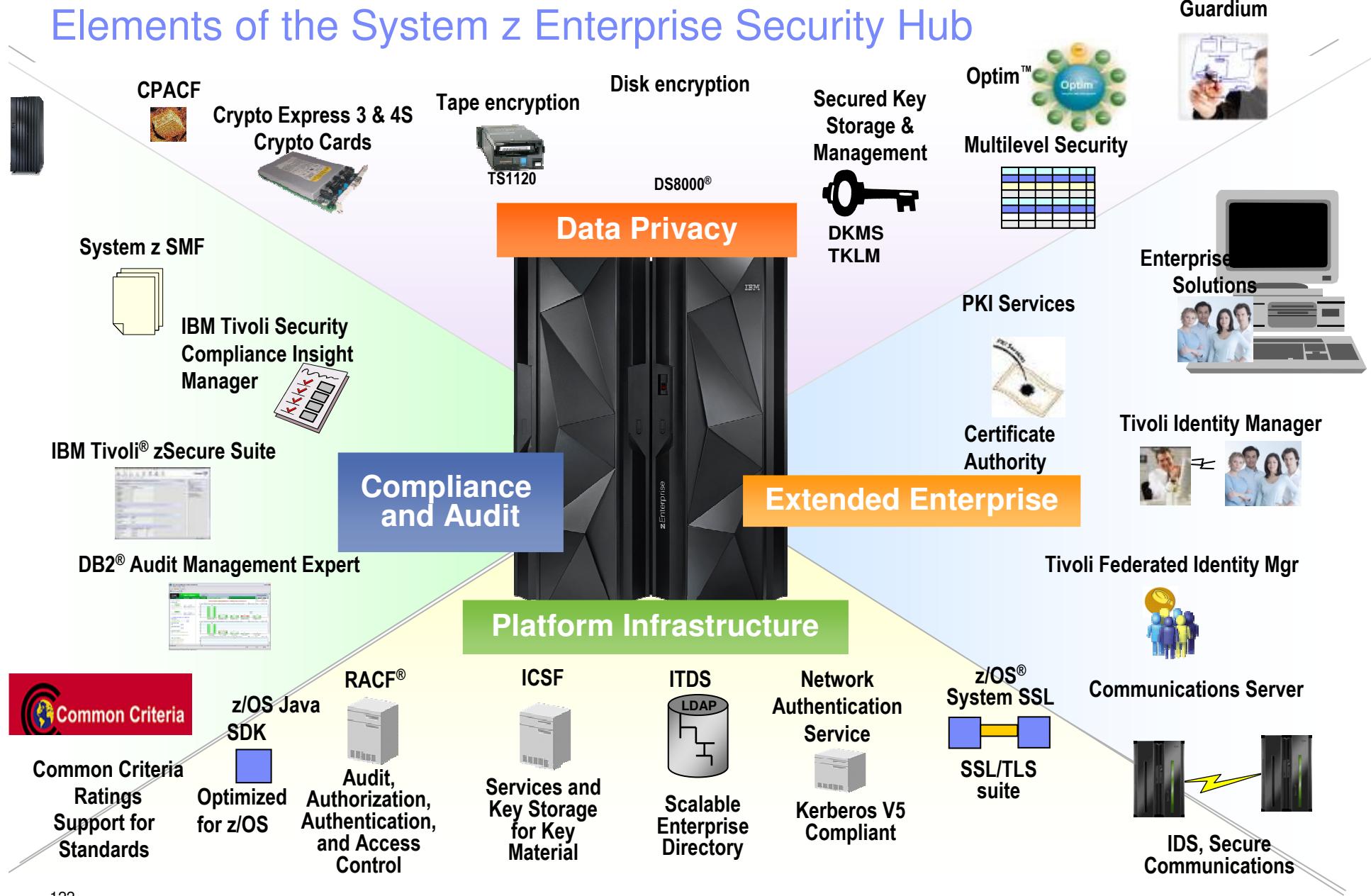
zEC12 Crypto Enhancements

- IBM Enterprise Public Key Cryptography Standards #11 (EP11)
 - Based on PKCS #11 specification v2.20 and more recent amendments
 - Designed to meet Common Criteria EAL 5+ and FIPS 140-2 Level 4
 - Conforms to Qualified Digital Signature (QDS) Technical Standards
- IBM Common Cryptographic Architecture (CCA)
 - Secure Cipher Text Translate
 - DUKPT for derivation of MAC and Encryption Keys
 - Wrap weaker keys with stronger keys for security and standards compliance
 - Compliance with new Random Number Generator standards
 - EMV enhancements for applications supporting American Express cards
- IBM Trusted Key Entry (TKE) 7.2 Licensed Internal Code (LIC)
 - Support for Crypto Express4S defined as a CCA coprocessor
 - Support for Crypto Express4S as a Enterprise PKCS #11 coprocessor
 - Support for new DES operational keys
 - New AES CIPHER key attribute
 - Allow creation of corresponding keys
 - New smart card part 74Y0551
 - Support for 4 smart card readers
 - Support for stronger key wrapping standards
 - Compatible with current TKE Workstation hardware

System z Evaluations & Certifications



Elements of the System z Enterprise Security Hub



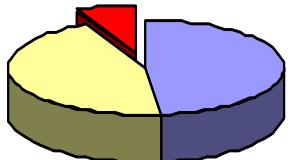
zEC12 RAS



System z overall RAS Strategy

.....Continuing our RAS focus helps avoid outages

Sources of Outages
Pre z9
-Hrs/Year/Syst-



- Scheduled (CIE+Disruptive Patches+ECs)
- Planned - (MES + Driver Upgrades)
- Unscheduled (UIRA)

Impact of Outage

	Prior Servers	z9 EC	z10 EC	z196	zEC12
Unscheduled Outages	✓	✓	✓	✓	✓
Scheduled Outages	✓	✓	✓	✓	✓
Planned Outages			✓	✓	✓
Preplanning requirements			✓	✓	✓
Power & Thermal Management		•Improved Silicon Reliability •Improved Mechanical Component Reliability		✓	✓

Redundancy in Mainframe Hardware

Power

2x Power Supply

2x Power feed

Internal Battery Feature

Optional internal battery in
cause of loss of external
power)

Cooling, air & water-cooling options

Dynamic oscillator switchover

Processors

Multiprocessors

Spare PUs

Memory

RAIM

Chip sparing

Error Correction and Checking

Enhanced book availability

- **The zEnterprise System continues to reduce customer down time by focusing on all sources of outages: unscheduled outages, scheduled outages and planned outages. Power and cooling requirements were reduced while still managing reliability.**

- Major new Memory design for preventing outages
- Introducing new IO drawers technologies designed for concurrent service
- Introducing Mainframe management to the mixed computing environment
- Delivering Green functions and RAS together

reduce SPOF
(Single Point of Failure)

Preventing All Outages

- Unscheduled Outages
 - ✓ **Advanced Memory RAIM (Redundant Array of Independent Memory) design**
 - ✓ Enhanced Reed-Solomon code (ECC) – 90B/64B
 - ✓ Protection against Channel/DIMM failures
 - ✓ Chip marking for fast DRAM replacements
 - ✓ **Mirrored Key cache**
 - ✓ **Improved chip packaging**
 - ✓ **Improved condensation management**
 - ✓ **Integrated TCP/IP checksum generation/checking**
 - ✓ **Integrated EPO switch cover (protecting the switch during repair actions)**
 - ✓ **Continued focus on Firmware**
- Scheduled Outages
 - ✓ **Double memory data bus lane sparing (reducing repair actions)**
 - ✓ **Single memory clock bus sparing**
 - ✓ **Field Repair of interface between processor chip and cache chip and between cache chips (fabric bus)**
 - ✓ **Fast bitline delete on L3/L4 cache (largest caches)**
 - ✓ **Power distribution using N+2 Voltage Transformation Modules (VTM)**
 - ✓ **Redundant (N+2) Humidity Sensors**
 - ✓ **Redundant (N+2) Altitude Sensors**
 - ✓ **Unified Resource Manager for zBX**

Improving Reliability

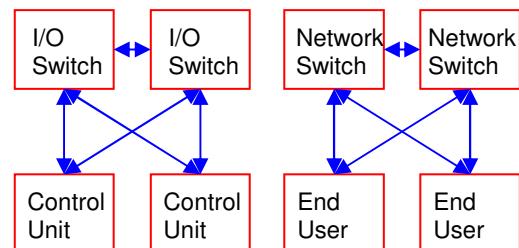
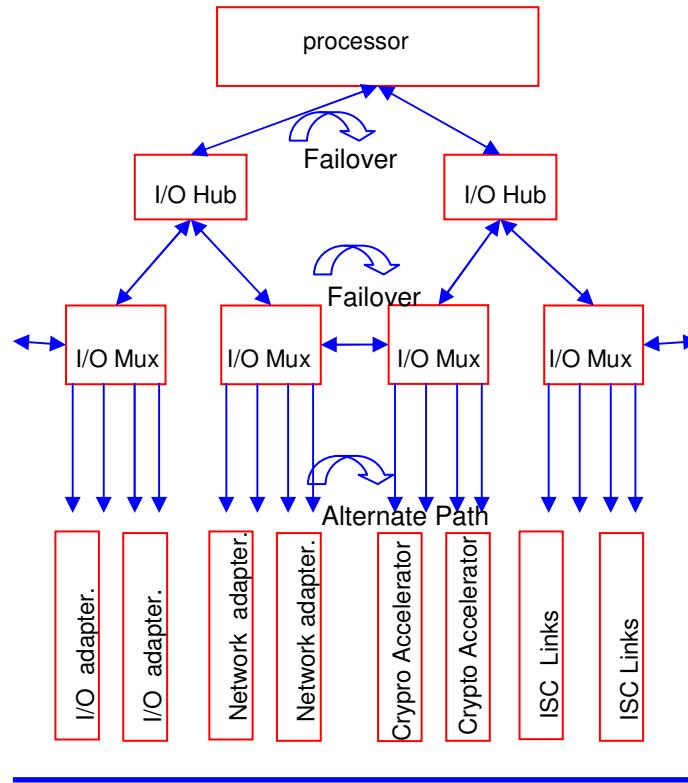
- **Power & Thermal Optimization and Management**

- ✓ Static Power Save Mode under z/OS control
- ✓ Smart blower management by sensing altitude and humidity
- ✓ Enhanced evaporator design to minimize temperature variations
- ✓ MCM cooling with N+1 design feature
- ✓ MCM backup cooling with Heat Exchanger
- ✓ Available air to water heat exchanger for customer water cooling

Concurrent Maintenance and Upgrades

- Duplex Units
 - Power Supplies,
- Concurrent Microcode (Firmware) updates
- Hot Pluggable I/O
- PU Conversion
- Permanent and Temporary Capacity Upgrades
 - Capacity Upgrade on Demand (CUoD)
 - Customer Initiated Upgrade (CIU)
 - On/Off Capacity on Demand (On/Off CoD)
- Capacity BackUp (CBU)
- Flexible & Plan Ahead Memory Options

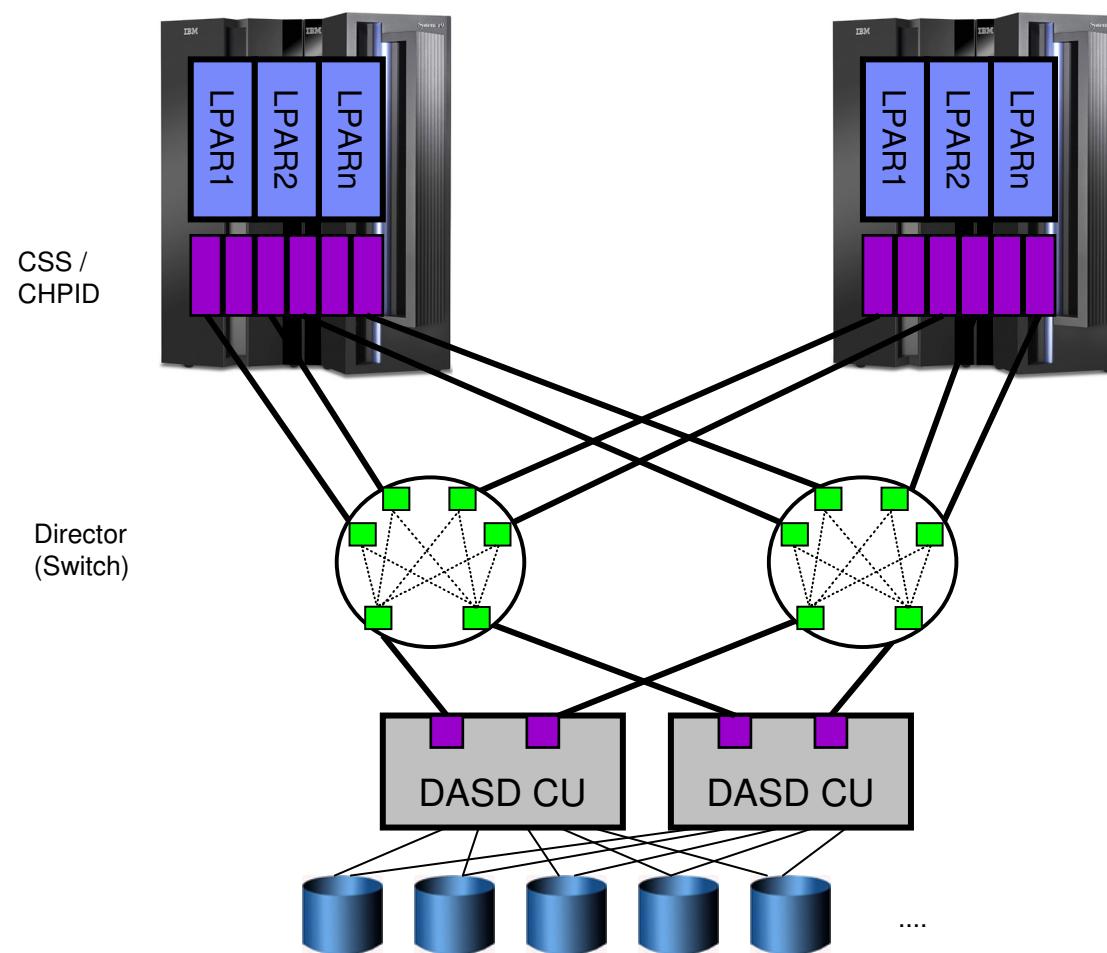
z196 RAS Design ofFully Redundant I/O Subsystem – of existing IO cage and drawers



Fully Redundant I/O Design

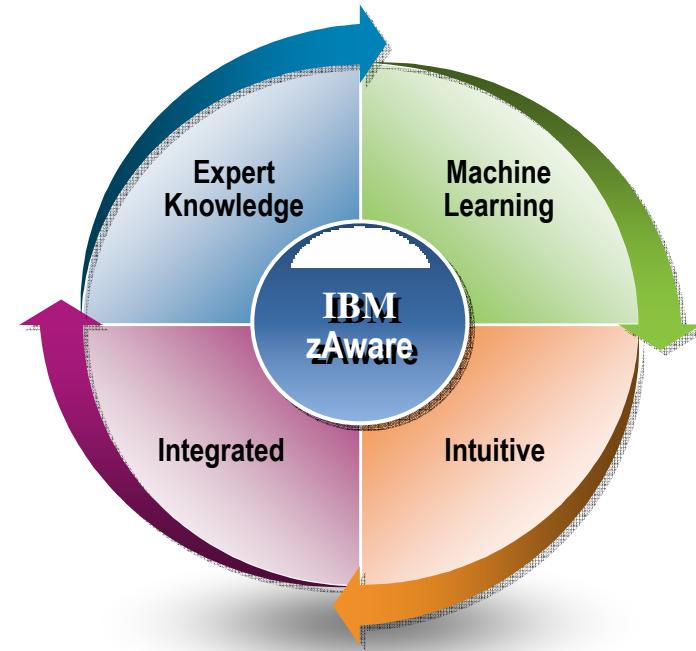
- SAP / CP sparing
- SAP Reassignment
- I/O Reset & Failover
- I/O Mux Reset / Failover
- Redundant I/O Adapter
- Redundant I/O interconnect
- Redundant Network Adapters
- Redundant ISC links
- Redundant Crypto processors
- I/O Switched Fabric
- Network Switched/Router Fabric
- High Availability Plugging Rules
- I/O and coupling fanout rebalancing on CBA
- Channel Initiated Retry
- High Data Integrity Infrastructure
- I/O Alternate Path
- Network Alternate Path
- Virtualization Technology

Create a redundant I/O configuration

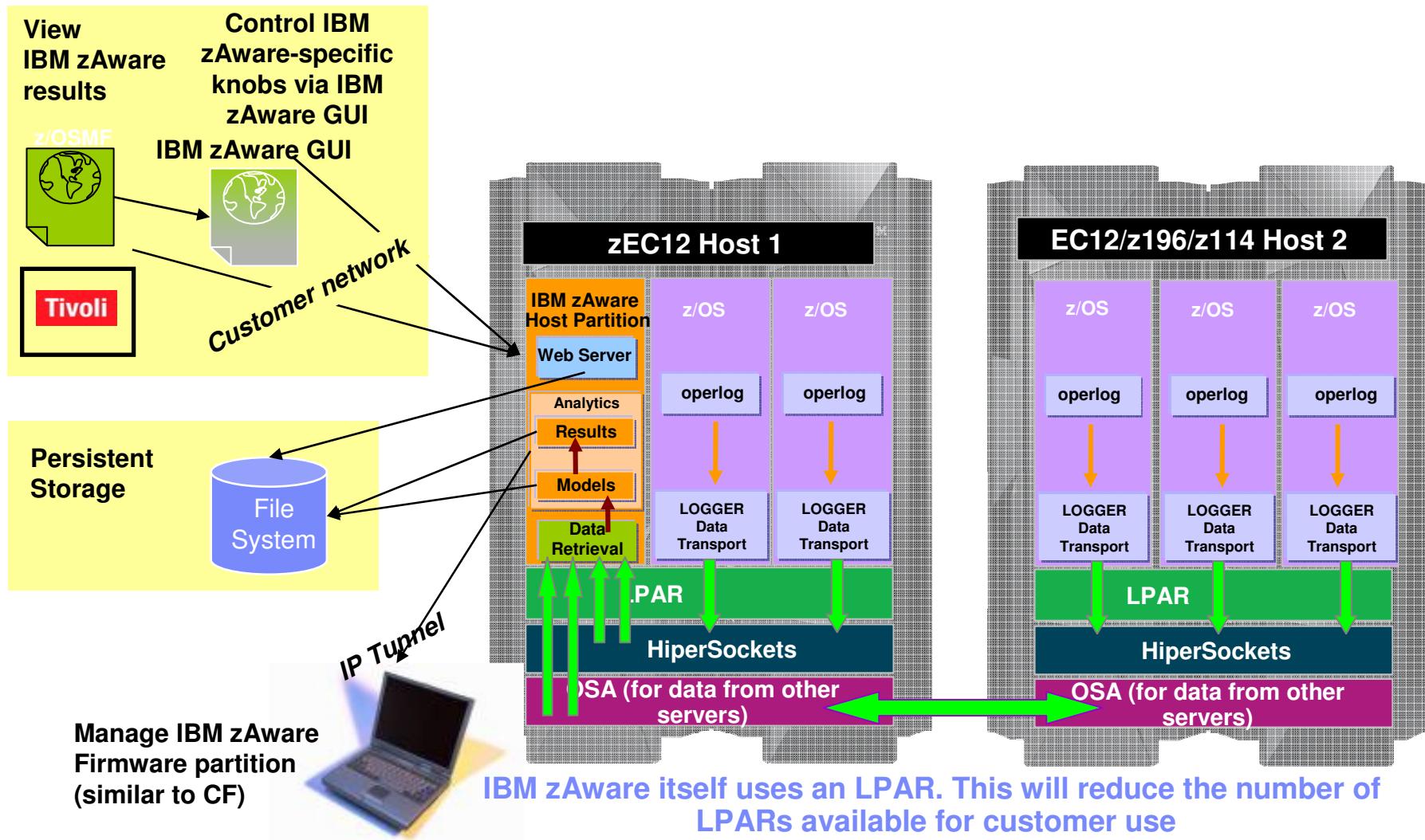


IBM zAware – IBM System z Advanced Workload Analysis Reporter

- Monitors z/OS OPERLOG messages including all z/OS console message, ISV and application generated messages
- Can monitor across a sysplex
- Samples every 2 minutes.
- Reports on 10 minute time slices.
- Uses a 90 day baseline created from SYSLOG
- Detects anomalies monitoring systems miss:
 - Messages may be suppressed or rare
 - Messages may indicate a trend
- Reports on unique messages, and a “score”
- Color-coded, browser-based (IE 8, Firefox)
- XML Output consumable through published API, can drive ISV products



A closer look inside IBM zAware



BACKUP

Slides



Did You Know...

Would you believe...

...that a massive multiplayer online gaming company selected an IBM mainframe, running Linux, as its platform of choice?

It's true!

Did you know...

...that customers can run most of the same applications on System z in 2008 that they could run on the 3033 in 1977?

Did you know?

- The "z" in System z stands for zero downtime.
- The "p" in System p stands for performance.
- The "i" in System i stands for integration.

Did you know...

...that mainframes run 70% of the world's major business operations?

Did you know...

...that a single mainframe system can scale up to process a billion transactions per day?

Did You Know...

Would you believe...

...that z/OS applications can be accessed from the Apple® iPhone™?

It's true! To learn more, click [Accessing z/OS Applications from an iPhone.](#)

Mainframes process roughly 30 billion business transactions per day, including most major credit card transactions and stock trades, money transfers, manufacturing processes, and ERP systems.

In 2004, an online marketplace where millions of items are sold each day lost \$1 million USD per hour due to an unplanned outage.

Did you know...

...that the z/OS Security Server has never been hacked or infected by a computer virus?

Did you know...

...that from July 2006 to July 2008, approximately 50,000 copies of Introduction to the New Mainframe: z/OS Basics were downloaded from IBM?

Did You Know...

Did you know...

...that System z is an ideal platform for consolidating and virtualizing hundreds or even thousands of servers?

Did you know...

...that System z can convert dispersed data into cohesive business intelligence and analytics?

Did you know...

...that Nationwide Insurance is saving an estimated \$15M by moving all new development to Linux on System z?

Did you know...

...that a typical System z mainframe can host more than 100,000 concurrent users?

Did you know...

...that in July 2007, analyst firm IDC ranked IBM as the worldwide revenue share leader in identity and access management software?

Did You Know...

Did you know...

...that the mainframe infrastructure enables standard, reliable communication between applications – dramatically reducing the need for connectivity-related coding?

Did you know...

...that, according to one analyst, System z requires a mere 1/12th the electricity of a distributed server farm with the equivalent processor capability?

Did you know...

...that turning on a new engine on a System z is the power equivalent of turning on a 75-watt light bulb?

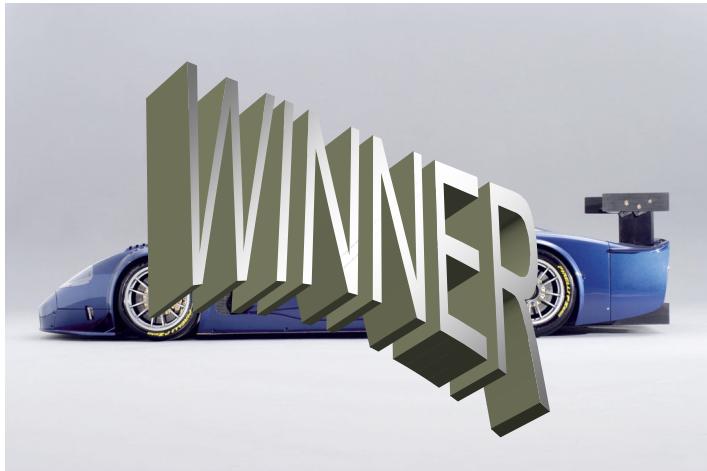
Did you know...

...that a Major Brazilian IT service provider used System z solutions to transform legacy systems into a modern development environment that enables them to process millions of online purchases per month?

Did you know...

...that IBM's own consolidation reduced energy consumption by 80% and footprint by 85% with a System z/Linux solution?

Quick Quiz: Which is the Better Vehicle?



Maserati MC12

VS.



Peterbilt Semi

The Race - ¼ Mile Dragstrip

Quick Quiz: Which is the Better Vehicle?



100 Maserati MC12

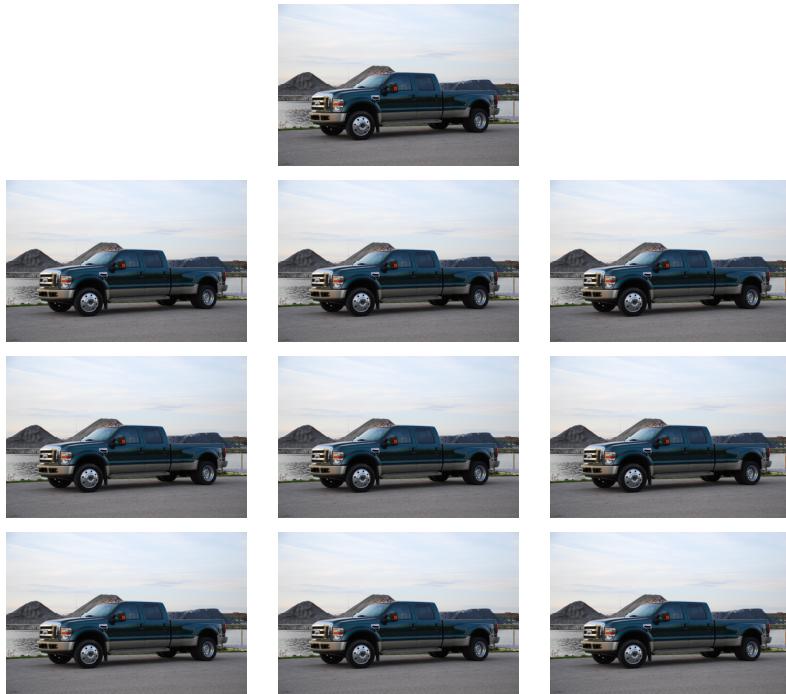
VS.



Peterbilt Semi

**The Race - $\frac{1}{4}$ Mile Dragstrip
Carrying 10 tons of crates**

Is this Better?



Peterbilt Semi

10 Ford F-450 1 ton Pickups

**The Race - $\frac{1}{4}$ Mile Dragstrip
Carrying 10 tons of crates**

Mainframe History - Myth vs. Truth

- <http://www-01.ibm.com/software/info/getztruth/index.jsp>
- ftp://public.dhe.ibm.com/s390/misc/bookoffer/download/360revolution_040704.pdf
- <http://www.vm.ibm.com/devpages/jelliott/pdfs/zhistory.pdf>
- <ftp://ftp.software.ibm.com/s390/audio/pdfs/zSeriesMainframeInnovations.pdf>
- <http://www.ca.com/us/bigiron.aspx>



Academic Initiative: Success Story

IBM Training Center for Mainframe opens at VIT, Vellore, India

- Students in Indian universities and colleges are generally taught about personal computers and small server technology. But mainframes run businesses, and students need exposure to this critical technology before they enter the workforce to maximize their effectiveness. The need was recognized by Chancellor G. Viswanathan of the Vellore Institute of Technology (VIT) in India – as well as by an IBM team looking for engineering institutes.
 - The opportunity opened in September 2010 for IBM to establish a partnership with VIT, a top-tier academic institute, which was ready to commit to nurturing and growing a System z ecosystem. Developed as part of the **IBM Academic Initiative System z Program**, this unique initiative builds partnerships with colleges and universities worldwide to add IBM enterprise systems education to curricula and put the mainframe back in computer science programs.
- The program kicked off with several training sessions that the India System z ISV team conducted at the VIT campus to educate professors and students on z/OS concepts. IBM helped the university explore enterprise system solutions as they built a long-term partnership with professors and the student community. In August, the “IBM Training Center for Mainframes” was officially launched at VIT. This is the second Training Center for Mainframe of its type in the world, and the first one in Asia. It has 60 dedicated high-end computers with 24/7 connectivity to the centralized System z in Dallas, Texas.
- VIT has added a course on “Introduction to Mainframe Computing” and offered it as an elective in its Master of Computer Applications curriculum.
- Chancellor Viswanathan has referred to IBM as a big role model and ensured that VIT will make use of IBM’s presence to foster innovation.
“India has the big advantage of producing the largest number of IT professionals in the world. The VIT will try to emerge as one of IBM’s best partners,” he said.

Master the Mainframe Contest

- **No experience** with mainframes is necessary. In fact, the contest is designed for students with little or no mainframe experience, increasing with difficulty as the contest progresses. Students just need to bring drive and competitive spirit and be ready to compete!

- **Experience!**

Today's mainframes are growing in popularity and require a new generation of mainframe experts. This contest is designed to equip you with basic skills to make you more competitive for jobs in the enterprise computing industry. Participation in the Master the Mainframe contest could give you the edge you need.



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- ABCs of z/OS System Programming Volume 3, [SG24-6983-03](#)
- ABCs of z/OS System Programming Volume 4, [SG24-6984-00](#)
- ABCs of z/OS System Programming Volume 5, [SG24-6985-01](#)
- ABCs of z/OS System Programming Volume 6, [SG24-6986-00](#)
- ABCs of z/OS System Programming Volume 7, [SG24-6987-01](#)
- ABCs of z/OS System Programming Volume 8, [SG24-6988-00](#)
- ABCs of z/OS System Programming Volume 9, [SG24-6989-04](#)
- ABCs of z/OS System Programming Volume 9, [SG24-6989-05](#)
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- IBM zEnterprise 196 Technical Guide, [SG24-7833-00](#)
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- IBM zEnterprise 114 Technical Guide, [SG24-7954-00](#)
- IBM System z Connectivity Handbook, [SG24-5444-12](#)
- z/Architecture Principles of Operation, [SA22-7832-08](#)
- z/Architecture Reference Summary, [SA22-7871-06](#)